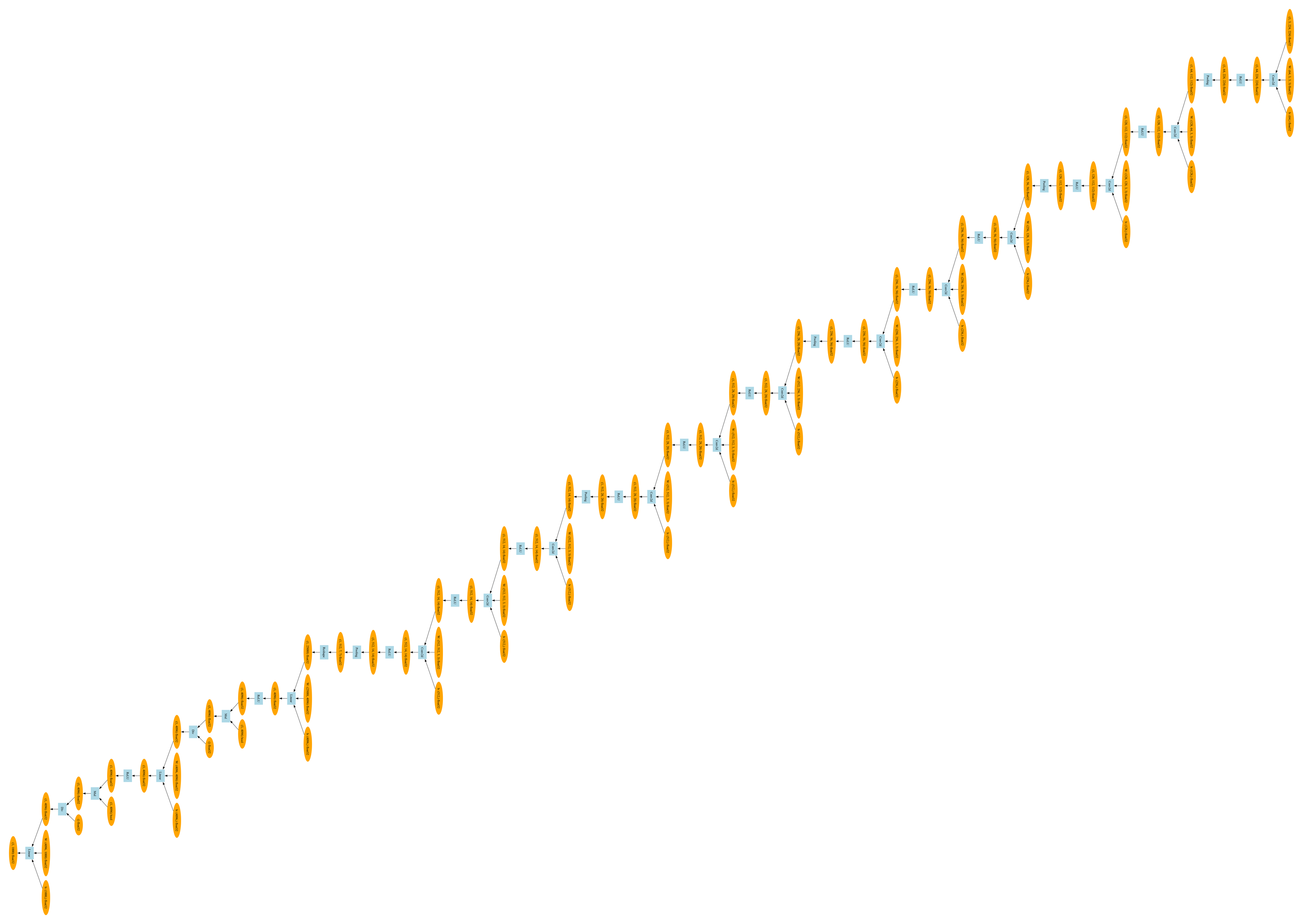
t: 1x1000 float32
I_Linear
W: 4096x1000 float32
b: 1x1000 x float32
t: 1x4096 float32
ReLU
t: 1x4096 float32
Mul
t: 1x4096 float32
t: 1x4096 float32
Div
t: 1x4096 float32
t: 1x1 float32
t: 1x4096 float32
t: 1x4096 float32
I_Linear
W: 4096x4096 float32
b: 1x4096 x float32
t: 1x4096 float32
Div
t: 1x4096 float32
t: 1x1 float32
t: 1x4096 float32
Mul
t: 1x4096 float32
t: 1x4096 float32
ReLU
t: 1x4096 float32
I_Linear
W: 25088x4096 float32
b: 1x4096 x float32
t: 1x25088 float32
Reshape
t: 1x512 x 7 x 7 float32
Pooling
t: 1x512 x 14 x 14 float32
ReLU
t: 1x512 x 14 x 14 float32
Conv2d
W: 512x512x3x3 float32
b: 1x512x1x1 float32
t: 1x512 x 14 x 14 float32
ReLU
t: 1x512 x 14 x 14 float32
Conv2d
W: 512x512x3x3 float32
b: 1x512x1x1 float32
t: 1x512 x 14 x 14 float32
Pooling
t: 1x512 x 28 x 28 float32
ReLU
t: 1x512 x 28 x 28 float32
Conv2d
W: 512x512x3x3 float32
b: 1x512x1x1 float32
t: 1x512 x 28 x 28 float32
ReLU
t: 1x512 x 28 x 28 float32
Conv2d
W: 512x256x3x3 float32
b: 1x256x1x1 float32
t: 1x256 x 28 x 28 float32
Pooling
t: 1x256 x 56 x 56 float32
ReLU
t: 1x256 x 56 x 56 float32
Conv2d
W: 256x256x3x3 float32
b: 1x256x1x1 float32
t: 1x256 x 56 x 56 float32
ReLU
t: 1x256 x 56 x 56 float32
Conv2d
W: 256x128x3x3 float32
b: 1x128x1x1 float32
t: 1x128 x 56 x 56 float32
Pooling
t: 1x128 x 112 x 112 float32
ReLU
t: 1x128 x 112 x 112 float32
Conv2d
W: 128x64x3x3 float32
b: 1x64x1x1 float32
t: 1x64 x 112 x 112 float32
Pooling
t: 1x64 x 224 x 224 float32
ReLU
t: 1x64 x 224 x 224 float32
Conv2d
W: 64x3x3x3 float32
b: 1x3x1x1 float32
t: 1x3 x 224 x 224 float32