ESP32-S3 Series

Hardware Design Guidelines

Introduction

Hardware design guidelines give advice on how to integrate ESP32-S3 into other products. ESP32-S3 is a series of high-performance Wi-Fi and Bluetooth® 5 (LE) SoCs.

These guidelines will help to ensure optimal performance of your product with respect to technical accuracy and conformity to Espressif's standards.

Version 1.1

Espressif Systems

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1 Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/documentation/esp32-s3_hardware_design_guidelines_en.pdf

ESP32-S3 is a highly-integrated, low-power, 2.4 GHz Wi-Fi + Bluetooth® LE (5) System-on-Chip (SoC) solution. It has the following features:

- Xtensa® 32-bit LX7 CPU operating at clock speeds up to 240 MHz
- Complete Wi-Fi + Bluetooth subsystem integrating radio and baseband, RF switch, RF balun, power amplifier, low noise amplifier (LNA), etc
- State-of-the-art power management unit
- Industry-leading RF performance
- Powerful AI computing ability
- Rich set of peripherals

ESP32-S3 also integrates advanced calibration circuitry that compensates for radio imperfections, and thus reduces the cost and time to the market for your product, and eliminates the need for specialized testing equipment.

The SoC is an ideal choice for a wide variety of application scenarios related to AI and Artificial Intelligence of Things (AIoT), such as:

- Wake word detection
- Speech commands recognition
- Face detection and recognition
- Smart home
- Smart appliances
- Smart control panel
- Smart speaker

For more information about ESP32-S3 series, please refer to *ESP32-S3 Series Datasheet*.

Note:

Unless otherwise specified, "ESP32-S3" used in this document refers to the series of chips, instead of a specific chip variant.

2 Schematic Checklist

The integrated circuitry of ESP32-S3 requires only 20 electrical components (resistors, capacitors, and inductors), one crystal and one SPI flash memory chip. The high integration of ESP32-S3 allows for simple peripheral circuit design. This chapter details ESP32-S3 schematics.

ESP32-S3 schematic is shown in Figure 1.

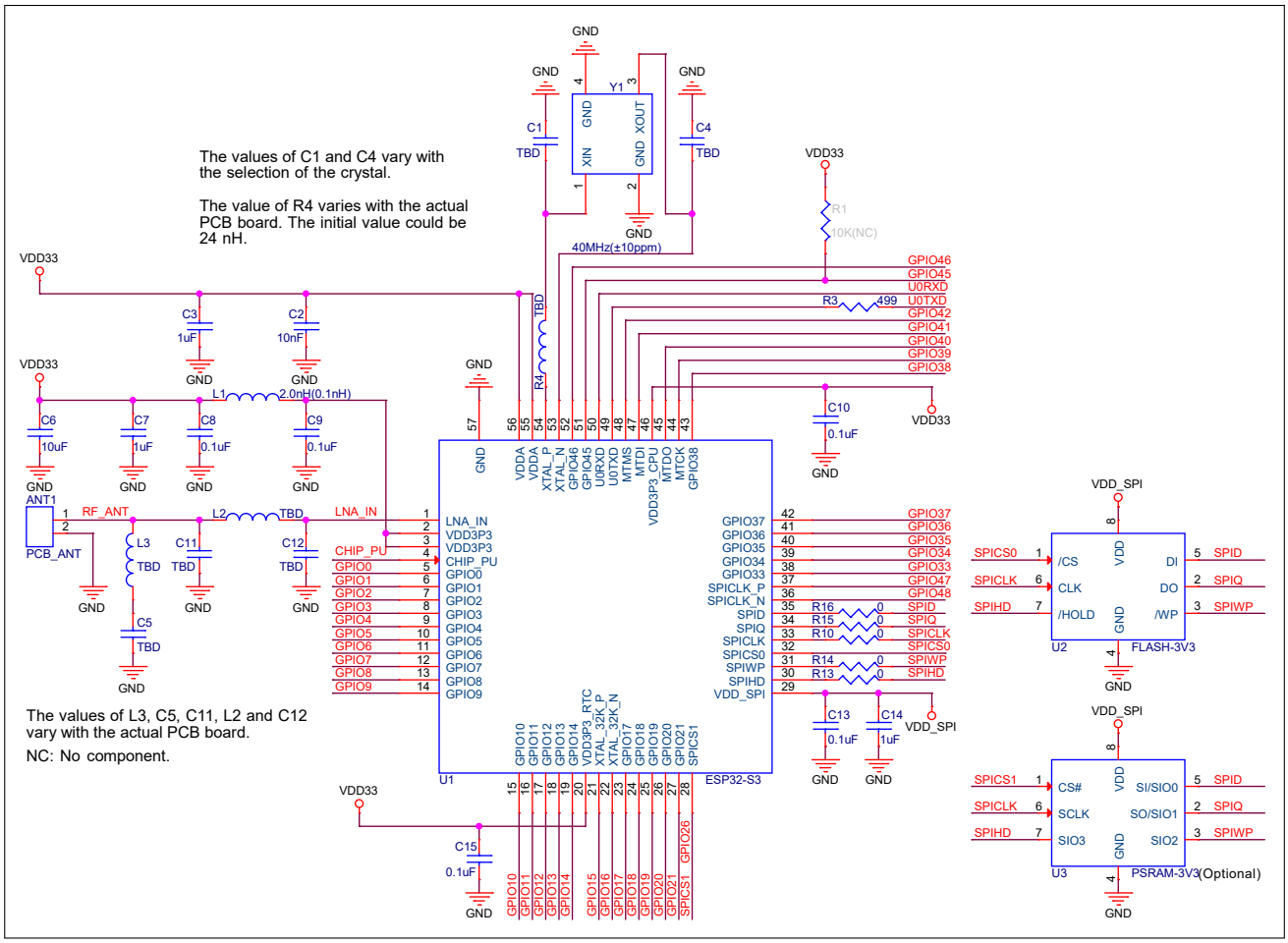

Figure 1: ESP32-S3 Schematic

Notice:

Figure 1 shows the connection for quad (SiP or external) SPI flash/PSRAM (3.3 V).

In cases when octal (SiP or external) SPI flash/PSRAM (3.3 V) is used, GPIO33 ~ GPIO37 are occupied and cannot be used for other functions.

In cases when octal (SiP or external) SPI flash/PSRAM (1.8 V) is used, GPIO33 ~ GPIO37 are occupied and R1 should be populated.

The core schematic for external octal flash/PSRAM (1.8 V) is as shown in Figure 2.

When there is only SiP flash, you do not need to populate the resistor on the SPI traces or care the SPI traces.

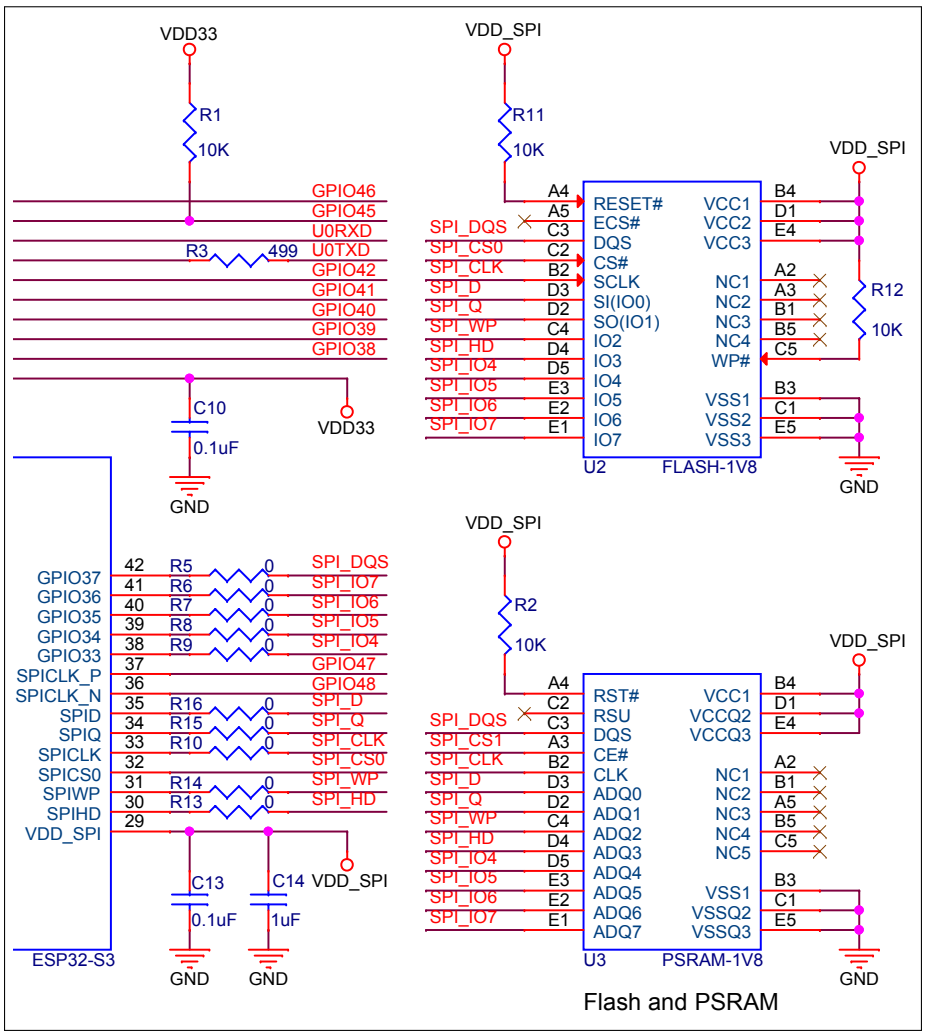

Figure 2: Schematic for the External Octal Flash/PSRAM (1.8 V)

Any basic ESP32-S3 circuit design may be broken down into 10 major sections:

- Power supply
- Power-on sequence and system reset
- Flash and SRAM
- Crystal
- RF
- UART
- ADC
- USB
- Touch Sensor
- Strapping pins

The rest of this document details the specifics of circuit design for each of these sections.

2.1 Power Supply

Details of using power supply pins can be found in Section *Power Scheme* in *ESP32-S3 Series Datasheet*.

2.1.1 Digital Power Supply

ESP32-S3 has pin46 VDD3P3_CPU that supplies power to CPU IO, in a voltage range of 3.0 V ~ 3.6 V. It is recommended to add an extra 0.1 μF decoupling capacitor close to each digital power supply pin.

Pin29 VDD_SPI can serve as the power supply for the external device at either 1.8 V if GPIO45 is pulled high during boot, or at 3.3 V if GPIO45 is pulled low during boot. It is recommended to add extra 0.1 μF and 1 μF decoupling capacitors close to VDD_SPI.

- When VDD_SPI operates at 1.8 V, it is powered by the internal Flash Voltage Regulator on the chip. The maximum current this Flash Voltage Regulator can offer is 40 mA.
- When VDD_SPI operates at 3.3 V, it is driven directly by VDD3P3_RTC through R_{SPI} resistor, therefore, there will be some voltage drop from VDD3P3_RTC.

VDD_SPI can also be driven by an external power supply.

Notice:
When using VDD_SPI as the power supply pin for the SiP or external 3.3 V flash/PSRAM, the supply voltage should be 3.0 V or above, so as to meet the requirements of flash/PSRAM's working voltage.

The schematic for the digital power supply pins is shown in Figure 3.

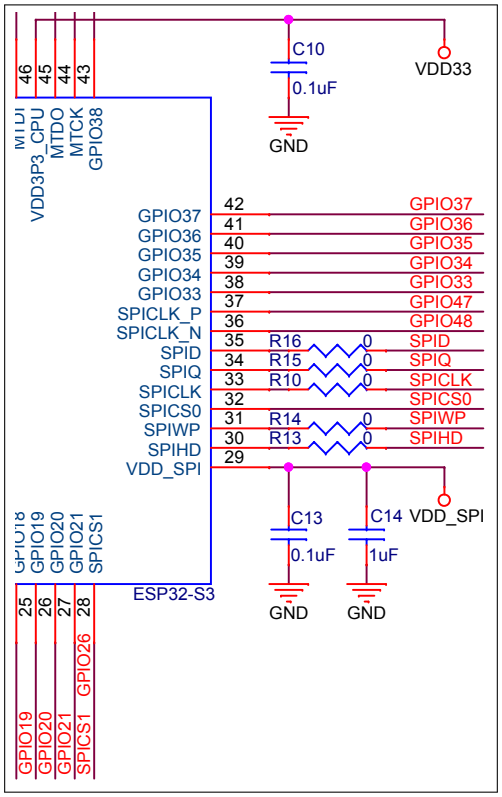

Figure 3: Schematic for the Digital Power Supply Pins

2.1.2 Analog Power Supply

Pin2 VDD3P3, pin3 VDD3P3, pin55 VDDA, and pin56 VDDA are the analog power supply pins, working at 3.0 V ~ 3.6 V.

It should be noted that the sudden increase in current draw, when ESP32-S3 is transmitting signals, may cause a power rail collapse. Therefore, it is highly recommended to add another 10 μF capacitor to the power trace, which can work in conjunction with the 0.1 μF capacitor. In addition, a LC filter circuit needs to be added near VDD3P3 pins so as to suppress high-frequency harmonics. The recommended rated current of the inductor is

500 mA or above. Refer to Figure 4 and place the appropriate decoupling capacitor near each analog power pin.

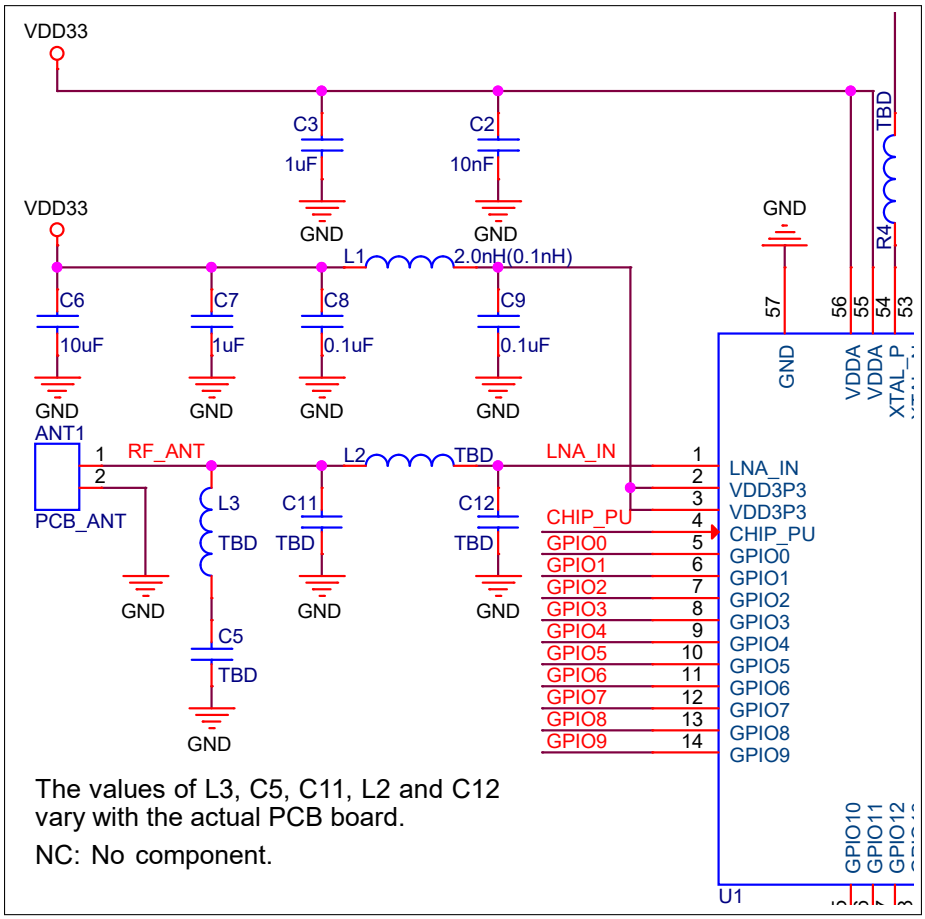

Figure 4: Schematic for the Analog Power Supply Pins

2.1.3 RTC Power Supply

Pin20 VDD3P3_RTC of ESP32-S3 series chips is RTC and analog power pin. It is recommended to place a 0.1 μf decoupling capacitor near this power pin in the circuit. This power supply cannot be used as backup power since it is not only for the RTC part.

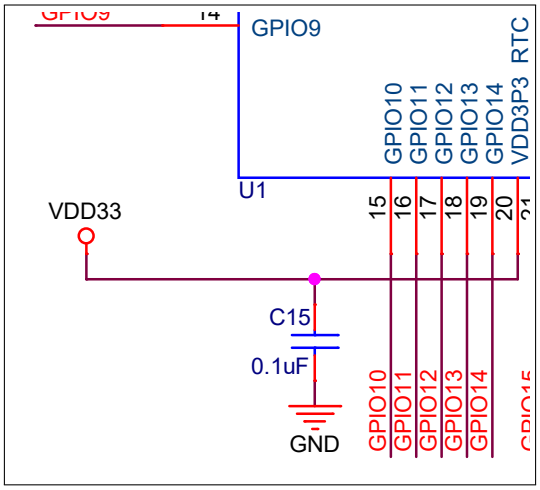

Figure 5: ESP32-S3 RTC Power Supply

Notice:

- When use the single power supply, the recommended power supply voltage for ESP32-S3 is 3.3 V and the output current should be no less than 500 mA.
- It is suggested to add an ESD protection diode at the power entrance.

2.2 Power-on Sequence and System Reset

2.2.1 Power-on Sequence

ESP32-S3 uses a 3.3 V system power supply. The chip should be activated after the power rails have stabilized. This is achieved by delaying the activation of CHIP_PU after the 3.3 V rails have been brought up.

Figure 6 shows the power-up and reset timing of ESP32-S3 series of SoCs. Details about the parameters are listed in Table 1.

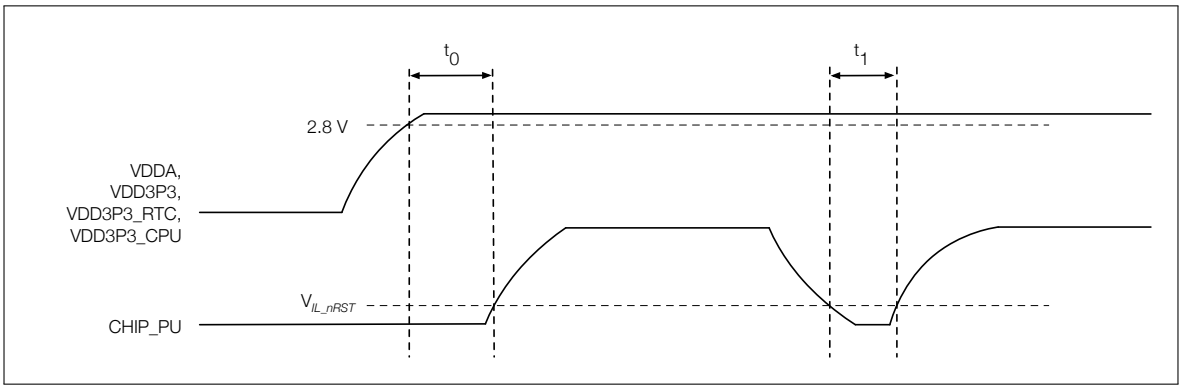

Figure 6: ESP32-S3 Power-up and Reset Timing

Table 1: Description of ESP32-S3 Power-up and Reset Timing Parameters

Parameter	Description	Min (μs)
t_0	Time between bringing up the power rails of VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU and activating CHIP_PU	50
t_1	Duration of CHIP_PU signal level < V_{IL_nRST} to reset the chip	50

Notice:

To ensure that stable power is supplied to the chip during power-up, it is advised to add an RC delay circuit at the CHIP_PU pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power supply features and the power-up and reset sequence timing of the chip.

2.2.2 System Reset

CHIP_PU serves as the reset pin of ESP32-S3. The reset voltage (V_{IL_nRST}) should be in the range of (–0.3 ~ 0.25 × VDD) V. VDD is the I/O voltage for a particular power domain of pins. To avoid reboots caused by external interferences, make the CHIP_PU trace as short as possible. Also, add a pull-up resistor as well as a capacitor to the ground whenever possible.

Notice:
CHIP_PU pin must not be left floating.

2.3 Flash and SRAM

ESP32-S3 requires SiP flash or external flash to store application firmware and data. SiP PSRAM or external RAM is optional.

2.3.1 SiP Flash and SiP PSRAM

SiP (System-in-Package) flash and SiP PSRAM refer to the flash and PSRAM that can be integrated into the package, depending on a chip variant. For the pin-to-pin mapping between the chip and SiP flash/PSRAM, please refer to Table 2. The chip pins listed here are not recommended for other usage.

Table 2: Pin-to-Pin Mapping Between Chip and SiP Flash/PSRAM

ESP32-S3FN8	SiP flash (8 MB, Quad SPI)
SPICLK	CLK
SPICS0	CS#
SPID	DI
SPIQ	DO
SPIWP	WP#
SPIHD	HOLD#
ESP32-S3R2	**SiP PSRAM (2 MB, Quad SPI)**
SPICLK	CLK
SPICS1	CE#
SPID	SI/SIO0
SPIQ	SO/SIO1
SPIWP	SIO2
SPIHD	SIO3
ESP32-S3R8 / ESP32-S3R8V	**SiP PSRAM (8 MB, Octal SPI)**
SPICLK	CLK
SPICS1	CE#
SPID	DQ0
SPIQ	DQ1
SPIWP	DQ2
SPIHD	DQ3
GPIO33	DQ4
GPIO34	DQ5
GPIO35	DQ6
GPIO36	DQ7
GPIO37	DQS/DM

2.3.2 External Flash and External RAM

ESP32-S3 supports up to 1 GB external flash and 1 GB external RAM. Make sure to select appropriate external flash and RAM according to the power voltage on VDD_SPI. It is recommended to add a zero-ohm series resistor on the SPI communication lines to lower the driving current, reduce interference to RF, adjust timing, and better shield from interference.

The ESP32-S3 schematics respectiavly for the external quad flash/PSRAM and external octal flash/PSRAM are shown in Figure 1 and Figure 2.

2.4 Clock Source

ESP32-S3 has two clock sources:

- External clock source
- RTC clock source

2.4.1 External Clock Source (compulsory)

Currently, the ESP32-S3 firmware only supports 40 MHz crystal or oscillator.

Crystal

The circuit for the crystal is shown in Figure 7. The specific capacitive values of C1 and C4 depend on further testing of, and adjustment to, the overall performance of the whole circuit. In order to reduce the drive strength of the crystal and minimize the impact of crystal harmonics on RF performance, a series component (a 20 nH inductor can be used initially) on the XTAL_P clock trace is required. Note that the accuracy of the selected crystal should be within ±10 ppm.

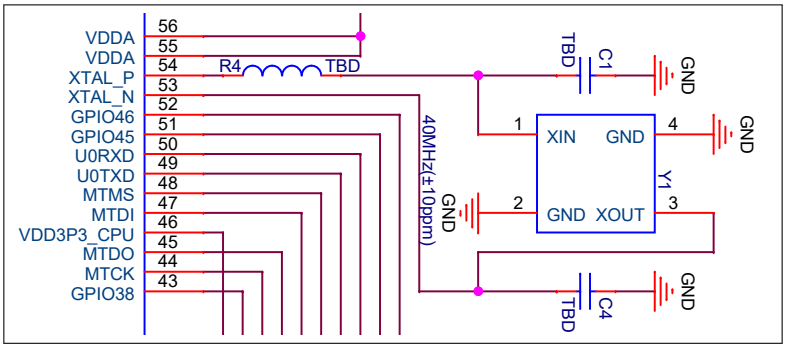

Figure 7: Schematic for the Crystal

Oscillator

If an oscillator is used, it is recommended to connect its output to XTAL_P on the chip through a component in series. XTAL_N can be floating. Make sure that the oscillator output is stable and its accuracy is within ±10 ppm. It is recommended to reserve a compatible design with crystal. In case of defects in the circuit design, you can still use the crystal.

Notice:

Defects in the manufacturing of crystal and oscillators (for example, large frequency deviation of more than ±10 ppm, unstable performance within operating temperature range, etc) may lead to the malfunction of ESP32-S3, resulting in a decrease of the RF performance.

2.4.2 RTC (optional)

ESP32-S3 supports an external 32.768 kHz crystal to act as the RTC clock. Figure 8 shows the schematic for the external 32.768 kHz crystal.

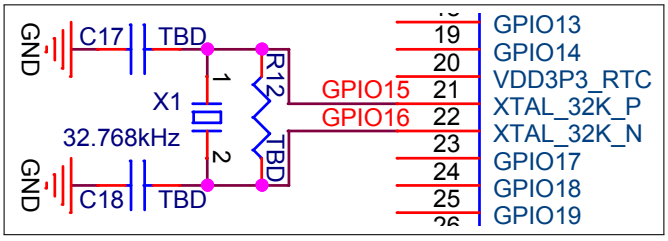

Figure 8: Schematic for the External Crystal (RTC)

Notice:

- Please note the requirements for the 32.768 kHz crystal.
  - Equivalent series resistance (ESR) $\leqslant 70\ k\Omega$.
  - Load capacitance at both ends should be configured according to the crystal's specification.
- The parallel resistor R is used for biasing the crystal circuit ($5\ M\Omega < R \leqslant 10\ M\Omega$). In general, you do not need to populate the resistor.
- If the RTC source is not required, then the pins for the external 32.768 kHz crystal can be used as other GPIOs.

2.5 RF

A π-type matching network is essential for antenna matching in the circuit design. CLC structure is recommended for the matching network. It is also recommended to add an LC filter circuit after the π-type matching network side to suppress secondary harmonics. The parameters of the components in the matching network are subject to the actual antenna and PCB layout. Figure 9 shows the RF matching schematic.

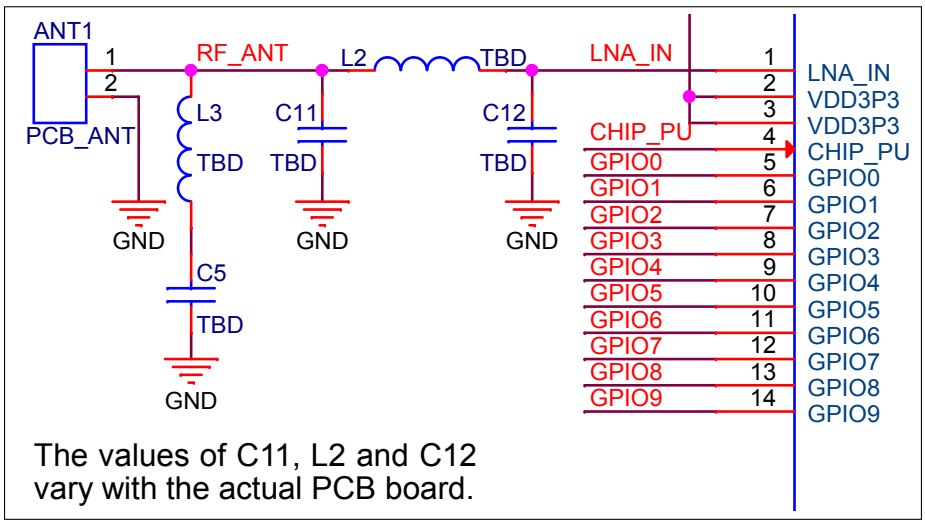

Figure 9: Schematic for RF Matching

2.6 UART

It is recommended to connect a 499 Ω series resistor to the U0TXD line in order to suppress the 80 MHz harmonics.

2.7 ADC

It is recommended to add a 0.1 μF filter capacitor to a pad when using the ADC function. ADC1 is recommended for use.

2.8 Strapping Pins

Note:
The content below is excerpted from Section Strapping Pins in *ESP32-S3 Series Datasheet*.

ESP32-S3 has four strapping pins:

- GPIO0
- GPIO45
- GPIO46
- GPIO3

Software can read the values of corresponding bits from register “GPIO_STRAPPING”.

During the chip’s system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of “0” or “1”, and hold these bits until the chip is powered down or shut down.

GPIO0, GPIO45 and GPIO46 are connected to the chip’s internal weak pull-up/pull-down during the chip reset. Consequently, if they are unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of these strapping pins.

GPIO3 is floating by default. Its strapping value can be configured to determine the source of the JTAG signal inside the CPU, as shown in Table 4. In this case, the strapping value is controlled by the external circuit that cannot be in a high impedance state. Table 3 shows more configuration combinations of EFUSE_DIS_USB_JTAG, EFUSE_DIS_PAD_JTAG, and EFUSE_STRAP_JTAG_SEL that determine the JTAG signal source.

Table 3: JTAG Signal Source Selection

EFUSE_STRAP_JTAG_SEL	EFUSE_DIS_USB_JTAG	EFUSE_DIS_PAD_JTAG	JTAG Signal Source
1	0	0	Refer to Table 4
0	0	0	USB Serial/JTAG controller
don't care	0	1	USB Serial/JTAG controller
don't care	1	0	On-chip JTAG pins
don't care	1	1	N/A

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-S3.

After reset, the strapping pins work as normal-function pins.

Refer to Table 4 for a detailed configuration of the strapping pins.

Table 4: Strapping Pins

VDD_SPI Voltage			
Pin	Default	3.3 V	1.8 V
GPIO45	Pull-down	0	1
Booting Mode [1]			
Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0
GPIO46	Pull-down	Don't care	0
Enabling/Disabling ROM Messages Print During Booting [2]			
Pin	Default	Enabled	Disabled
GPIO46	Pull-down	See the 2nd note	See the 2nd note
JTAG Signal Selection			
Pin	Default	EFUSE_DIS_USB_JTAG = 0, EFUSE_DIS_PAD_JTAG = 0, EFUSE_STRAP_JTAG_SEL=1	
GPIO3	N/A	0: JTAG signal from on-chip JTAG pins 1: JTAG signal from USB Serial/JTAG controller	

Note:

1. The strapping combination of GPIO46 = 1 and GPIO0 = 0 is invalid and will trigger unexpected behavior.
2. By default, the ROM boot messages are printed over UART0 (U0TXD pin) and USB Serial/JTAG controller together. The ROM code printing can be disabled through configuration register and eFuse. For detailed information, please refer to Chapter Chip Boot Control in *ESP32-S3 Technical Reference Manual*.

VDD_SPI voltage is determined either by the strapping value of GPIO45 or by EFUSE_VDD_SPI_TIEH. When EFUSE_VDD_SPI_FORCE is 0, VDD_SPI voltage is determined by the strapping value of GPIO45; when EFUSE_VDD_SPI_FORCE is 1, VDD_SPI voltage is determined by EFUSE_VDD_SPI_TIEH. Please refer to the following table for default configurations:

Table 5: The Default Value for VDD_SPI Voltage

Chip Variant	EFUSE_VDD_SPI_FORCE	EFUSE_VDD_SPI_TIEH	VDD_SPI Voltage
ESP32-S3	0	0	Determined by GPIO45
ESP32-S3R2	1	1	Force to 3.3 V
ESP32-S3R8	1	1	Force to 3.3 V
ESP32-S3R8V	1	0	Force to 1.8 V
ESP32-S3FN8	1	1	Force to 3.3 V
ESP32-S3FH4R2	1	1	Force to 3.3 V

Figure 10 shows the setup and hold times for the strapping pin before and after the CHIP_PU signal goes high. Details about the parameters are listed in Table 6.

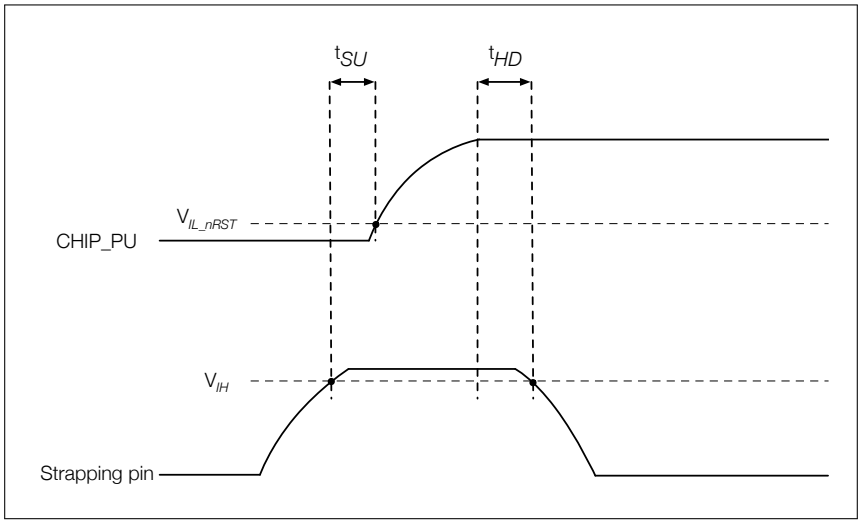

Figure 10: Setup and Hold Times for the Strapping Pin

Table 6: Parameter Descriptions of Setup and Hold Times for the Strapping Pin

Parameter	Description	Min (ms)
t_{SU}	Setup time before CHIP_PU goes from low to high	0
t_{HD}	Hold time after CHIP_PU goes high	3

2.9 USB

ESP32-S3 has a full-speed USB On-The-Go (OTG) peripheral with integrated transceivers. The USB peripheral is compliant with the USB 2.0 specification. GPIO19 and GPIO20 can be used as D- and D + of USB respectively. It is recommended to populate zero-ohm series resistors between the mentioned pins and the USB connector. Also reserve a footprint for a capacitor to ground on each trace.

ESP32-S3 also integrates a USB Serial/JTAG controller that supports USB 2.0 full-speed device.

2.10 Touch Sensor

When using the touch function, it is recommended to populate a zero-ohm series resistor at the chip side to reduce the coupling noise and interference on the line, and to strengthen the ESD protection. The recommended resistance is from 470 Ω to 2 kΩ, preferably 510 Ω. The specific value also depends on the actual test results of the product.

The ESP32-S3 touch sensor has a waterproof design and digital filtering function. Note that only GPIO14 (TOUCH14) can drive the shield electrode.

3 PCB Layout Design

This chapter introduces the key points of how to design an ESP32-S3 PCB layout using the ESP32-S3-WROOM-2 module as an example.

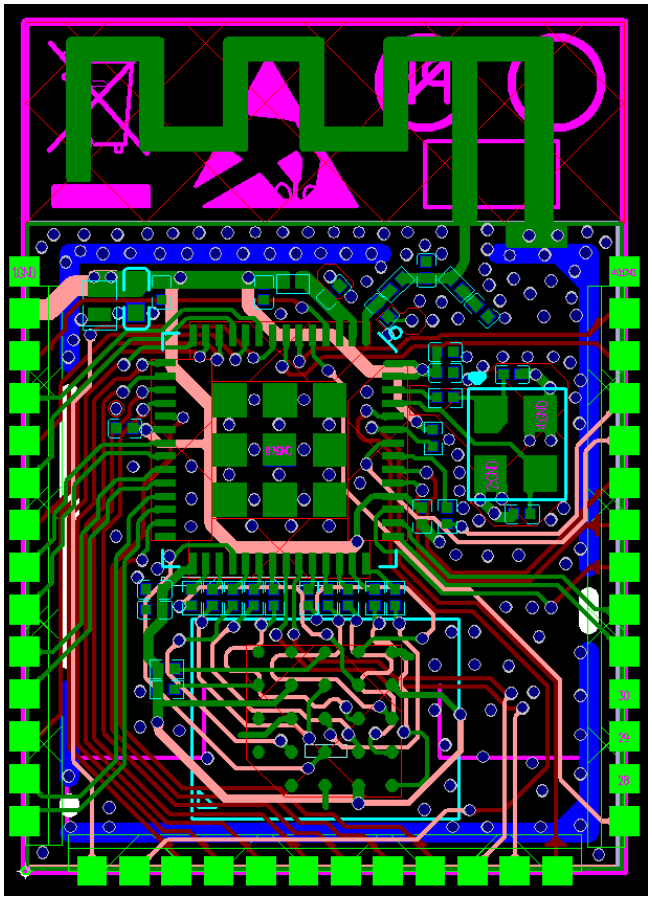

Figure 11: ESP32-S3 PCB Layout

3.1 General Principles of PCB Layout

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Signal traces and components
- Layer 2 (GND): No signal traces here to ensure a complete GND plane
- Layer 3 (POWER): GND plane should be applied. It is recommended to route power traces here.
- Layer 4 (BOTTOM): GND plane should be applied. It is not recommended to place any components on this layer. It is acceptable to route signal traces on this layer.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Signal traces and components
- Layer 2 (BOTTOM): Do not place any components on this layer and keep traces to a minimum. Please be noted that you should provide a complete GND plane for RF, crystal and ESP32-S3 chip.

3.2 Positioning a Module on a Base Board

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

The module should be placed as close to the edge of the base board as possible. On-board PCB antenna should be placed outside the base board whenever possible. In addition, the feed point of the antenna should be closest to the board. In the following example figures, positions with mark ✓are strongly recommended, while positions without a mark are not recommended.

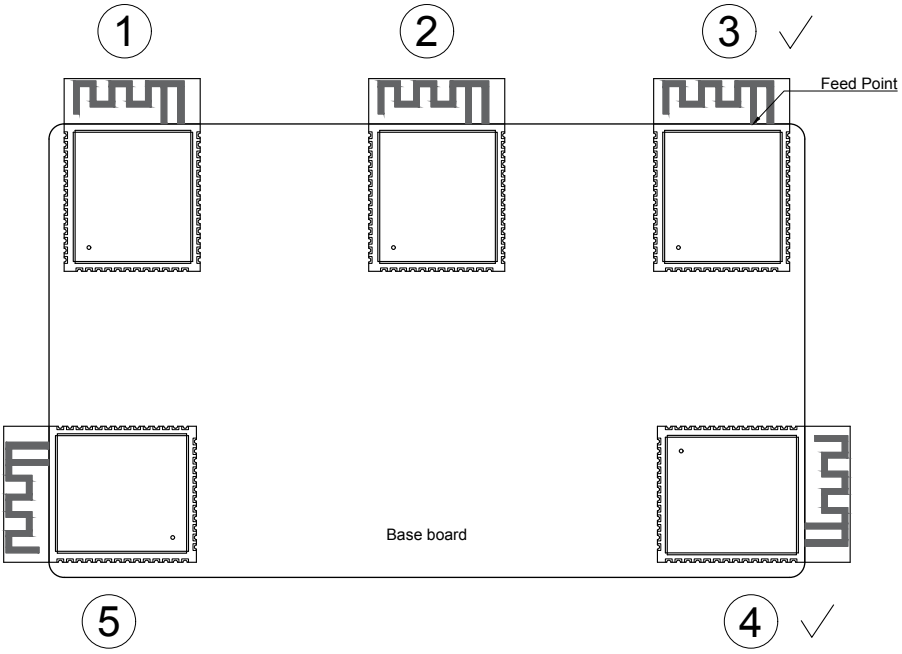

Figure 12: Placement of ESP32-S3 Modules on Base Board (antenna feed point on the right)

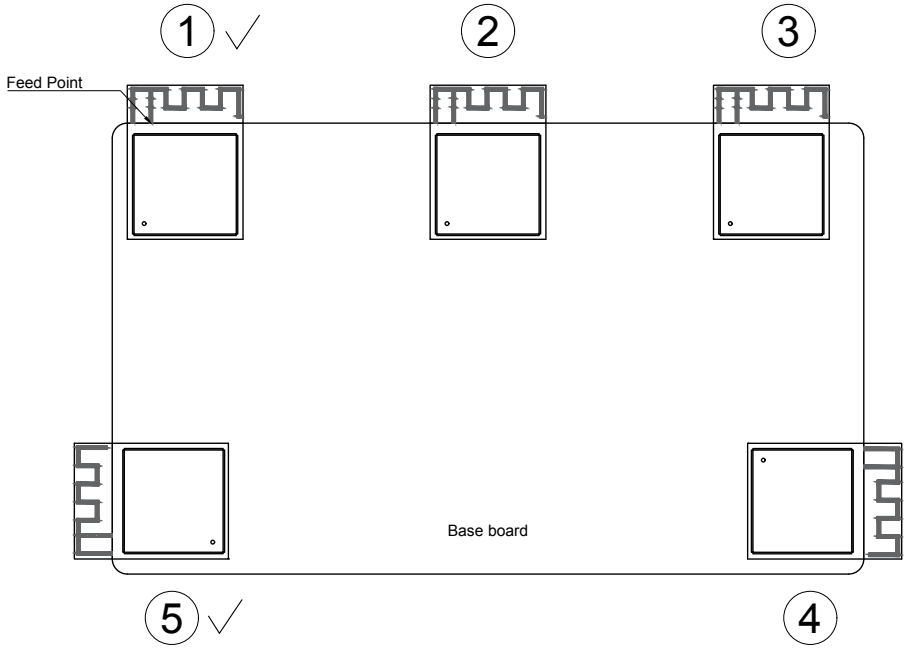

Figure 13: Placement of ESP32-S3 Modules on Base Board (antenna feed point on the left)

If PCB antenna could not be outside the board, please ensure a large clear region at least 15 mm around antenna area (no copper, routing, components on it), as shown in Figure 14. If there is base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna.

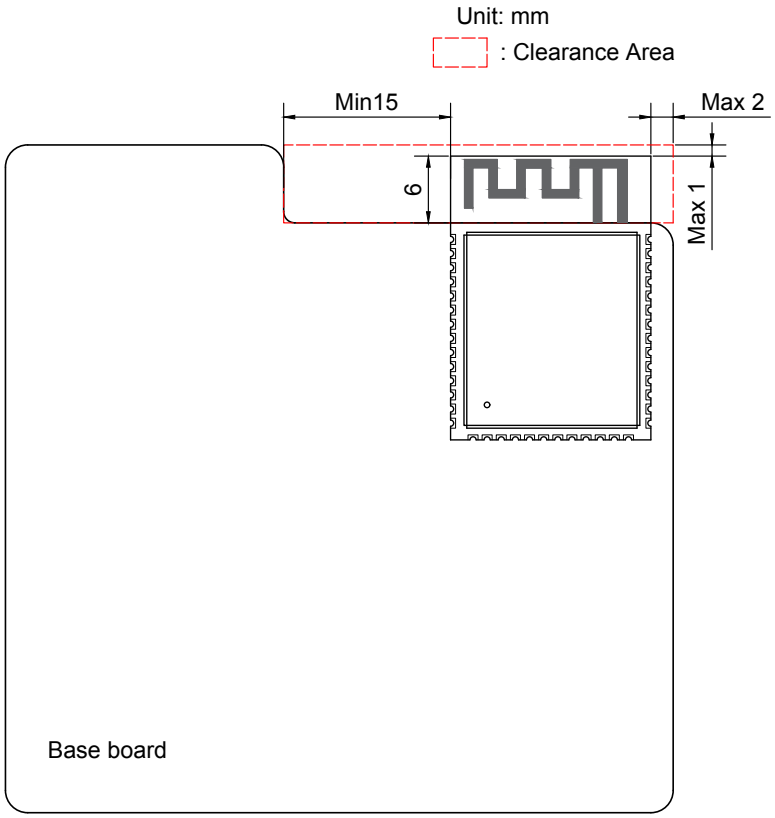

Figure 14: Keepout Zone for ESP32-S3 Module's Antenna on the Base Board

When designing an end product, attention should be paid to the interference caused by the housing of the antenna and it is recommended to carry out RF verification.

As a conclusion, please be noted it is necessary to test the throughput and communication signal range of the whole product to ensure real product performance.

3.3 Power Supply

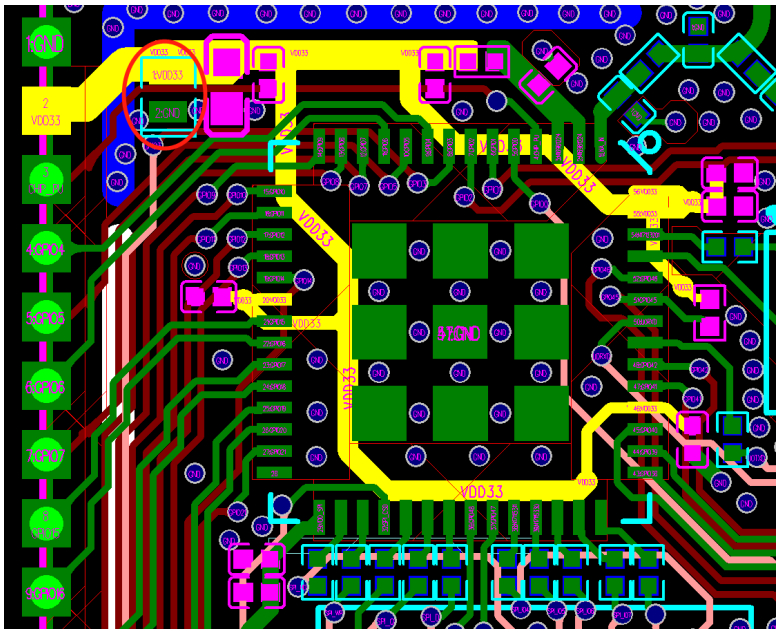

Figure 15: ESP32-S3 Power Traces in a Four-layer PCB Design

- Four-layer PCB design is preferred. The power traces should be routed on inner Layer 3 whenever possible. Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.
- The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure 15. The width of the main power traces should be no less than 25 mil. The width of the power traces for VDD3P3 pins should be no less than 20 mil. Recommended width of other power traces is 10 mil.
- The ESD protection diode is placed next to the power port (circled in red in the top left quarter of Figure 15). The power trace should have a 10 µF capacitor on its way to the chip, to be used in conjunction with a 0.1 µF capacitor. Then the power traces are divided into two ways from here and form a star-shape topology, thus reducing the coupling between different power pins. Note that all decoupling capacitors should be placed close to the power pin, and ground vias should be added close to the capacitor's ground pin to ensure a short return path.
- As shown in Figure 16, it is recommended to connect the capacitor to ground in the LC filter circuit near VDD3P3 pins to the fourth layer through a via, and maintain a keep-out area on other layers, so as to further restrain harmonic disturbance.
- The power trace begins at the power entrance and reaches VDD3P3. It is required to add GND isolation between this power trace and the GPIO traces on the left, and place vias whenever possible.
- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.

Note:
If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a

nine-grid on the EPAD, cover the gaps with ink, and place ground vias in the gaps, as shown in Figure 15. This can avoid tin leakage when soldering the module EPAD to the substrate.

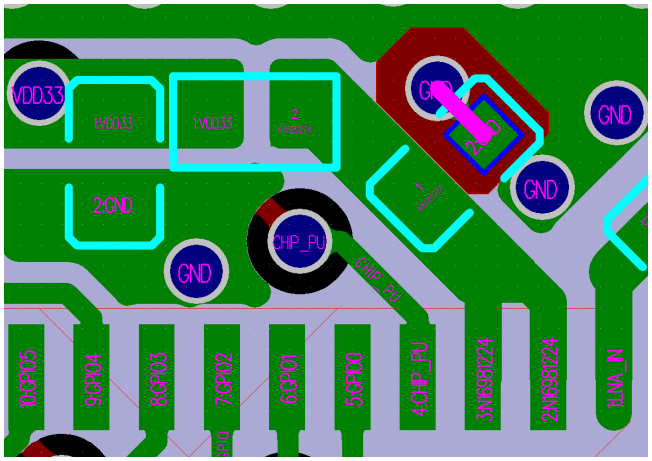

Figure 16: ESP32-S3 Analog Power Traces in a Four-layer PCB Design

3.4 Crystal

Figure 17 and Figure 18 show the reference design of the crystal. In addition, the following should be noted:

- The crystal should be placed far from the clock pin to avoid the interference on the chip. **The gap should be at least 2.0 mm**. It is good practice to add high-density ground via stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces, which means the traces cannot cross layers.
- The external loading capacitor should be placed on the near left or right side of the crystal, and at the end of the clock trace whenever possible, to make sure the ground pad of the capacitor is close to that of the crystal.
- Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper.
- As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

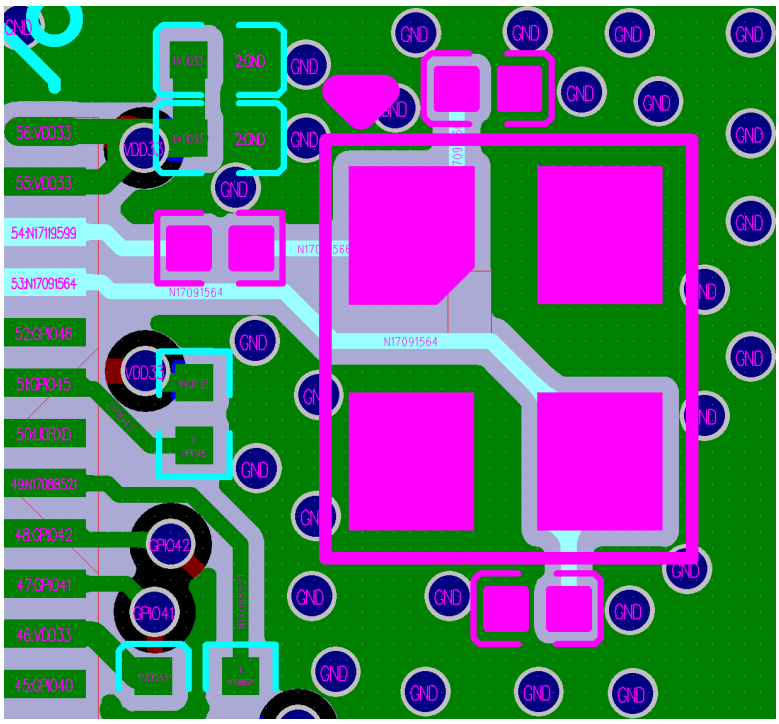

Figure 17: ESP32-S3 Crystal Layout (Connected to the Ground)

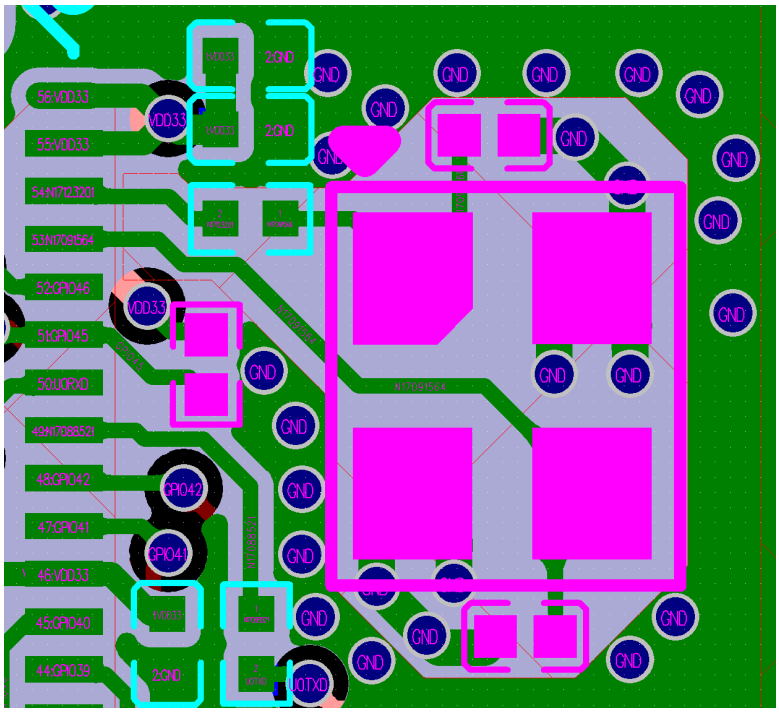

Figure 18: ESP32-S3 Crystal Layout (Not Connected to the Ground))

3.5 RF

The RF trace is routed as shown highlighted in pink in Figure 19.

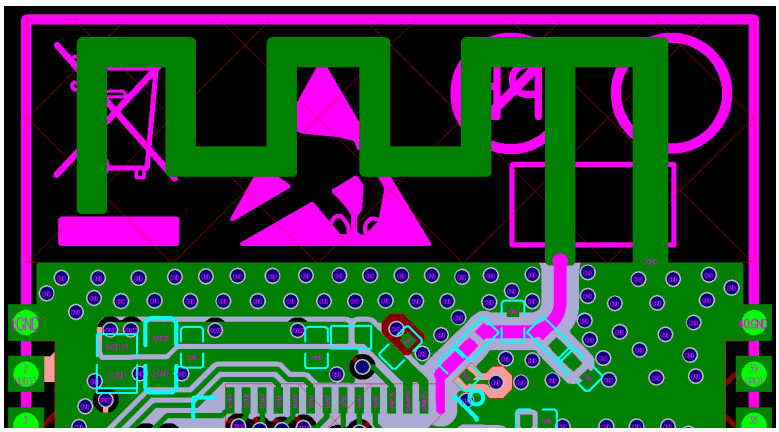

Figure 19: ESP32-S3 RF Layout in a Four-layer PCB Design

- The RF trace should have 50 Ω single-ended characteristic impedance. The reference plane is the second layer. A π-type matching circuit and an LC filter circuit should be added on the RF trace and placed close to the chip, in a zigzag.
- For designing the RF trace at 50 Ω single-ended impedance, please refer to the PCB stack-up design shown in Figure 20.
- The RF trace should have consistent width and not branch out. It should be as short as possible with dense ground vias around for inteference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- Please add a stub between the ground and the capacitors near the chip to suppress second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the number of PCB layers, so that the characteristic impedance of the stub is 100 Ω ± 10%. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. The trace highlighted in Figure 21 is the stub. Note that a stub is not required for package types above 0201.
- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	12.2	12.6	12.2

Stack up	Material	Base copper (oz)	Thickness (mil)	DK
SM			0.4	4
L1_Top	Finished copper 1 oz	0.33	0.8	
PP	7628 TG150 RC50%		8	4.39
L2_Gnd		1	1.2	
Core	Core		Adjustable	4.43
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8	4.39
L4_Bottom	Finished copper 1 oz	0.33	0.8	
SM			0.4	4

Figure 20: ESP32-S3 PCB Stack up Design

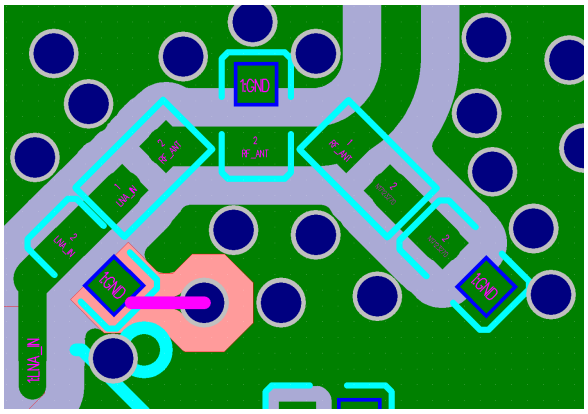

Figure 21: ESP32-S3 Stub in a Four-layer PCB Design

3.6 Flash and PSRAM

Place the zero-ohm series resistors on the SPI lines closer to the chip. Route the SPI traces on the inner layer (e.g., the third layer) whenever possible. Add ground copper and ground vias around the clock and data traces of SPI separately. Octal SPI traces should have matching lengths.

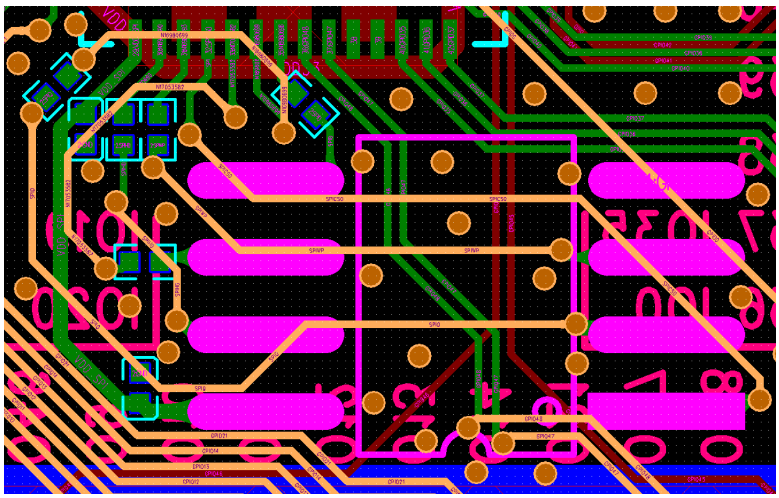

Figure 22: ESP32-S3 Quad Flash Layout

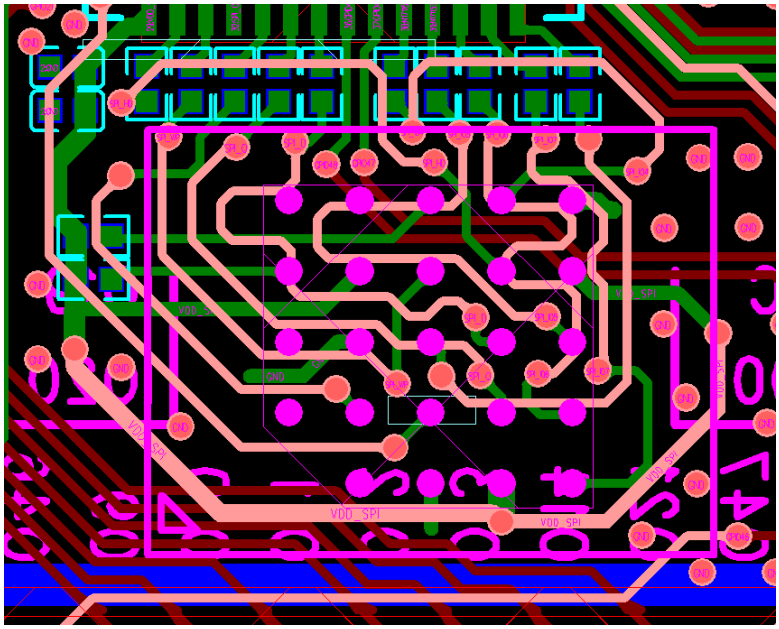

Figure 23: ESP32-S3 Octal Flash Layout

3.7 UART

The series resistor on the U0TXD trace needs to be placed close to the chip and away from the crystal. The U0TXD and U0RXD traces on the top layer should be as short as possible, surrounded by ground copper and ground vias.

3.8 USB

Place the RC circuit on the USB traces closer to the chip. Please use differential pairs and route them in parallel at equal lengths. Make sure there is a complete reference ground plane and surround the USB traces with ground copper.

3.9 Touch Sensor

ESP32-S3 offers up to 14 capacitive IOs that detect changes in capacitance on touch sensors due to finger contact or proximity. The chip's internal capacitance detection circuit features low noise and high sensitivity. It allows to use touch pads with smaller area to implement the touch detection function. You can also use the touch panel array to detect a larger area or more test points.

Figure 24 depicts a typical touch sensor application.

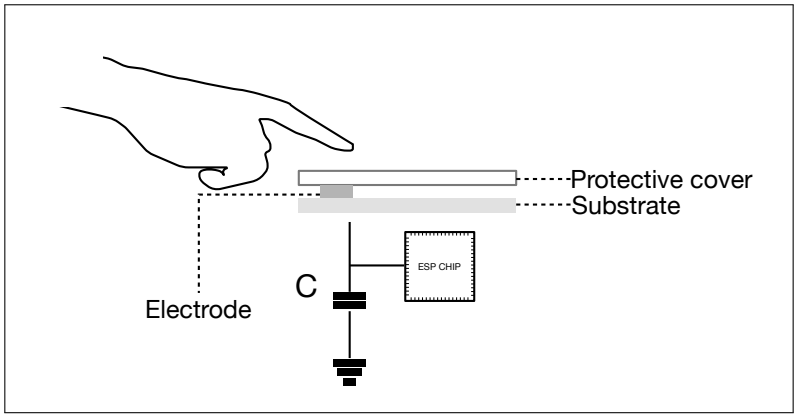

Figure 24: A Typical Touch Sensor Application

In order to prevent capacitive coupling and other electrical interference to the sensitivity of the touch sensor system, the following factors should be taken into account.

3.9.1 Electrode Pattern

The proper size and shape of an electrode improves system sensitivity. Round, oval, or shapes similar to a human fingertip are commonly applied. Large size or irregular shape might lead to incorrect responses from nearby electrodes.

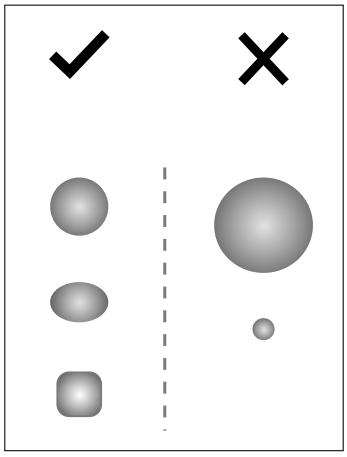

Figure 25: Electrode Pattern Requirements

Note:
The examples illustrated in Figure 25 are not of actual scale. It is suggested to use a human fingertip as reference.

3.9.2 PCB Layout

Figure 26 illustrates the general guidelines to routing traces. Specifically,

- The trace should be as short as possible and no longer than 300 mm.
- The trace width (W) can not be larger than 0.18 mm (7 mil).
- The alignment angle (R) should not be less than 90°.
- The trace-to-ground gap (S) should be in the range of 0.5 mm to 1 mm.
- The electrode diameter (D) should be in the range of 8 mm to 15 mm.
- Hatched ground should be added around the electrodes and traces.
- The traces should be isolated well and routed away from that of the antenna.

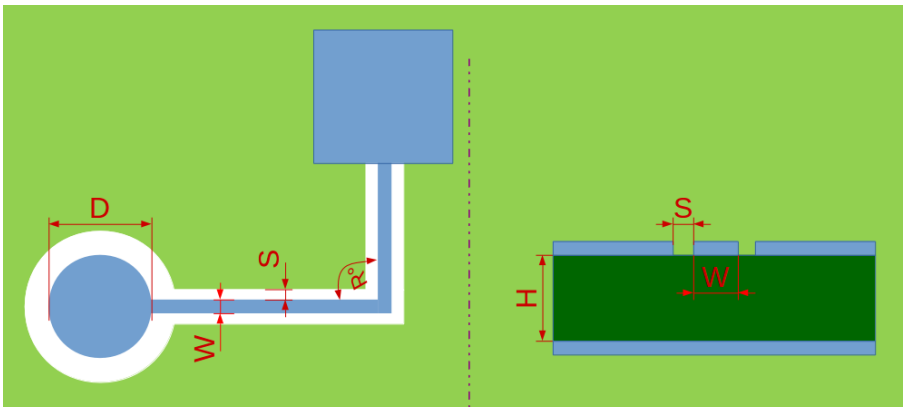

Figure 26: Sensor Track Routing Requirements

3.9.3 Waterproof and Proximity Sensing Design

ESP32-S3 touch sensor has a waterproof design and features proximity sensor function. Figure 27 shows an example layout of a waterproof and proximity sensing design.

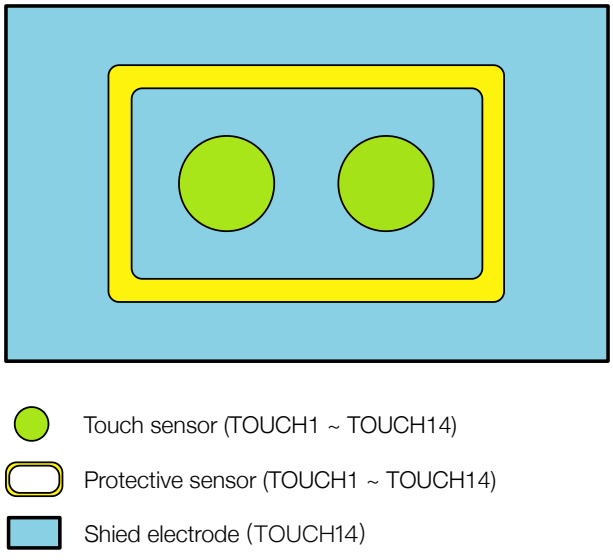

Figure 27: Shield Electrode and Protective Sensor

Note the following guidelines to better implement the waterproof and proximity sensing design:

- The recommended width of the shield electrode width is 2 cm.
- Employ a grid on the top layer with a trace width of 7 mil and a grid width of 45 mil (25% fill). The filled grid is connected to the driver shield signal.
- Employ a grid on the bottom layer with a trace width of 7 mil and a grid width of 70 mil (17% fill). The filled grid is connected to the driver shield signal.
- The protective sensor should be in a rectangle shape with curved edges and surround all other sensors.
- The recommended width of the protective sensor is 2 mm.
- The recommended gap between the protective sensor and shield sensor is 1 mm.
- The sensing distance of the proximity sensor is directly proportional to the area of the proximity sensor. However, increasing the sensing area will introduce more noise. Actual testing is needed for optimized performance.
- It is recommended that the shape of the proximity sensor is a closed loop. The recommended width is 1.5 mm.

Note:
For more details on the hardware design of ESP32-S3 touch sensor, please refer to *ESP32-S3 Touch Sensor Application Note*.

3.10 Typical Layout Problems and Solutions

3.10.1 Q: The current ripple is not large, but the TX performance of RF is rather poor.

Analysis:

The current ripple has a strong impact on the RF TX performance. It should be noted that the ripple must be tested when ESP32-S3 is in the normal working mode. The ripple increases when the power gets high in a different mode.

Generally, the peak-to-peak value of the ripple should be <80 mV when ESP32-S3 sends MCS7@11n packets, and <120 mV when ESP32-S3 sends 11m@11b packets.

Solution:

Add a 10 μF filter capacitor to the branch of the power trace (the branch powering the chip's analog power pin). The 10 μF capacitor should be as close to the analog power pin as possible for small and stable current ripples.

3.10.2 Q: The power ripple is small, but RF TX performance is poor.

Analysis:

The RF TX performance can be affected not only by power ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces,

such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiation components, such as inductors and antennas, may also decrease the RF performance.

Solution:

This problem is caused by improper layout and can be solved by re-layout. Please see Section 3.4 for details.

3.10.3 Q: When ESP32-S3 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis:

The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution:

Match the antenna's impedance with the π-type circuit on the RF trace, so that impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

3.10.4 Q: TX performance is not bad, but the RX sensitivity is low.

Analysis:

Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution:

Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please see Section 3.5 for details.

4 Hardware Development

4.1 ESP32-S3 Modules

For a list of ESP32-S3 modules please check Modules section of Espressif website.

To review module reference designs please check Documentation section of Espressif website.

Notes on Using Modules

- The module uses one single pin as the power supply pin. You can connect the module to a 3.3 V power supply that can drive at least 500 mA output current. The 3.3 V power supply works both for the analog circuit and the digital circuit.
- The EN pin is used for enabling the module. Set the EN pin high for normal working mode. There is no RC delay circuit on the module. It is recommended to add an external RC delay circuit to the module. For details please refer to Section 2.2.
- Lead the GND, RXD, TXD pins out and connect them to a USB-to-UART converter for firmware download, log-printing and communication.

By default, the initial firmware has already been downloaded in the flash. If you need to download different firmware, please follow the steps below:

1. Set the module to UART Download mode by pulling IO0 (pulled up by default) and IO46 (pulled down by default) low.
2. Power on the module and check whether the module has entered UART Download mode via serial port.
3. Download your firmware into flash using Flash Download Tool.
4. After firmware has been downloaded, pull IO0 high to enter SPI Boot mode.
5. Power on the module again. The chip will read and execute the new firmware during initialization.

Notice:

- During the whole process, you can check the status of the chip with the log printed through UART. If the firmware cannot be downloaded or executed, you can check if the working mode is normal during the chip initialization by looking at the log.
- The serial port cannot be used for both the log-print and flash-download tools simultaneously.

4.2 ESP32-S3 Development Boards

For a list of the latest designs of ESP32-S3 boards please check Development Boards section of Espressif website.

5 Related Documentation and Resources

Related Documentation

- ESP32-S3 Series Datasheet – Specifications of the ESP32-S3 hardware.
- ESP32-S3 Technical Reference Manual – Detailed information on how to use the ESP32-S3 memory and peripherals.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S3 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S3 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S3 Series SoCs* – Browse through all ESP32-S3 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S3
- *ESP32-S3 Series Modules* – Browse through all ESP32-S3-based modules.
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- *ESP32-S3 Series DevKits* – Browse through all ESP32-S3-based devkits.
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Glossary

CLC	Capacitor-Inductor-Capacitor
DDR	Double-Data Rate
ESD	Electrostatic Discharge
GND	Ground
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
RX	Receive
SiP	System-in-Package
TX	Transmit
Zero-ohm resistor	A zero-ohm resistor is a placeholder on the circuit so that another higher ohm resistor can replace it, depending on design cases.

Revision History

Date	Version	Release Notes
2022-06-02	v1.1	• Added Section 2.1.3 *RTC Power Supply* • Updated the following sections: – Section 2.1 *Power Supply* – Section 2.2 *Power-on Sequence and System Reset* – Section 2.3 *Flash and SRAM* – Section 2.4.1 *External Clock Source (compulsory)* – Section 2.8 *Strapping Pins* – Section 3.1 *General Principles of PCB Layout* – Section 3.4 *Crystal* – Section 3.6 *Flash and PSRAM* • Updated the following figures: – Figure 1 *ESP32-S3 Schematic* (including the note) – Figure 2 *Schematic for the External Octal Flash/PSRAM (1.8 V)* – Figure 11 *ESP32-S3 PCB Layout* – Figure 15 *ESP32-S3 Power Traces in a Four-layer PCB Design* – Figure 16 *ESP32-S3 Analog Power Traces in a Four-layer PCB Design* – Figure 19 *ESP32-S3 RF Layout in a Four-layer PCB Design* – Figure 21 *ESP32-S3 Stub in a Four-layer PCB Design* • Other minor updates
2021-09-30	v1.0	First release

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