

Synthesis Report

Testbench	Pass
Clock Cycle	10 (ns)
Cell Area	237349.274729
Total Time	10840 (ns)
Area*Time	2572866138.06

Synthesis No-latch (screenshot)

Inferred memory devices in process
in routine IOTDF line 306 in file
'/home/raid7_2/userb10/b10163/ICD2024/ICD_HW3/02_SYN/IOTDF.v'.

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
o_data_reg	Flip-flop	128	Y	N	N	N	N	N	N
o_busy_reg	Flip-flop	1	N	N	N	N	N	N	N
state_reg	Flip-flop	2	Y	N	N	N	N	N	N
whole_data_reg	Flip-flop	128	Y	N	N	N	N	N	N
o_valid_reg	Flip-flop	1	N	N	N	N	N	N	N
counter_reg	Flip-flop	4	Y	N	N	N	N	N	N

Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb10/b10163/ICD2024/ICD_HW3/02_SYN/IOTDF.db:IOTDF'
Loaded 1 design.
Current design is 'IOTDF'.
design_vision>
Current design is 'IOTDF'.

Log History

design_vision>

Ready

Synthesis slack (screenshot)

clock clk (rise edge) 10.00 10.00
clock network delay (ideal) 1.00 11.00
clock uncertainty -0.10 10.90
o_data_reg[2]/CK (DFFQXL) 0.00 10.90 r
library setup time -0.09 10.81
data required time 10.81

data required time 10.81
data arrival time -10.81

slack (MET) 0.00

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Log History

design_vision>

Ready