Digital Standard Cell Library

SAED_EDK90_CORE

DATABOOK

Document #: SAED_EDK90_CORE
Revision : 1.11
Technology : SAED90nm
Process : SAED90nm 1P9M 1.2v / 2.5v / 3.3v

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1. Introduction

This Databook describes possibilities, peculiarities of SAED_EDK90_CORE Digital Standard Cell Library and technical parameters of separate cells included in it. The library is free from intellectual property restrictions. It is one of the components of SAED_EDK90 Educational Design Kit (EDK). SAED_EDK90 EDK is anticipated for the use of educational purposes aimed at training highly qualified specialists in the area of microelectronics in:

- SYNOPSYS Customer Education Services
- SYNOPSYS Global Technical Services
- Universities included in SYNOPSYS University Program

SAED_EDK90 is foreseen to support the trainees to better master:

- Advanced design methodologies
- Capabilities of SYNOPSYS tools.

For the use of EDK it is assumed that European or North American bundle of SYNOPSYS EDA tools is available to trainees.

SAED_EDK90_CORE Digital Standard Cell Library is anticipated for designing different integrated circuits (ICs) by the application of 90nm technology and SYNOPSYS EDA tools.

The SAED_EDK90_CORE Digital Standard Cell Library has been built using SAED90nm 1P9M 1.2V/2.5V/3.3V design rules. The library has been created aimed at optimizing the main characteristics of designed ICs by its help. The library includes typical miscellaneous combinational and sequential logic cells for different drive strengths. Besides, the library contains all the cells which are required for different styles of low power (multi-voltage, multi-threshold) designs (www.synopsys.com/products/power/multivoltage_bkgrd.pdf, www.synopsys.com/sps/pdf/optimum_sleep_transistor_vlsi_dat06.pdf). Those are the following: Isolation Cells, Level Shifters, Retention Flip-Flops, Always-on Buffers and Power Gating Cells. The presence of all these cells provides the support of IC design with different core voltages to minimize dynamic and leakage power.
In order to implement multi-threshold low power techniques High-Vt (HVT), Low-Vt (LVT) and Standart-Vt (SVT) versions of the Library exist. The rest of this document covers only SVT cells.

2. General Information

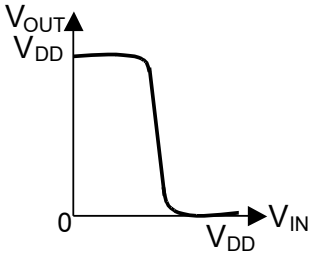
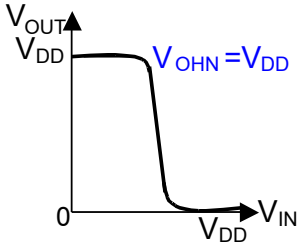
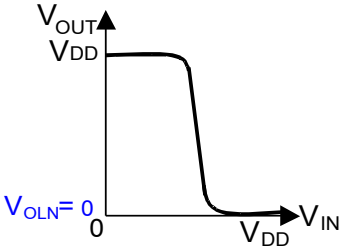
The used symbols of logic elements' states are shown in Table 2.1.

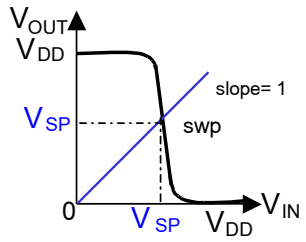
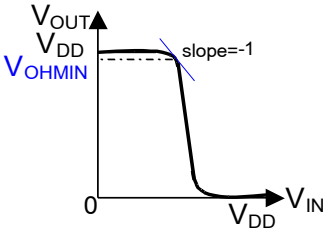
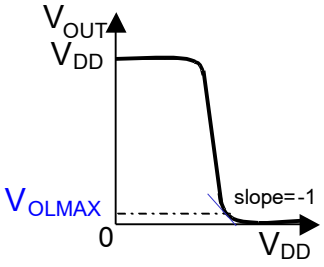
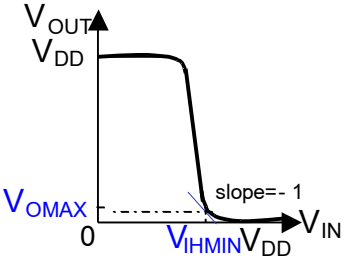
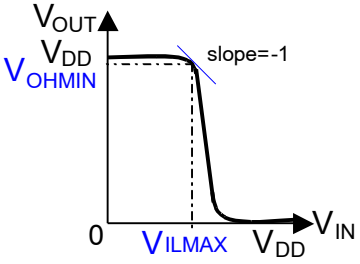
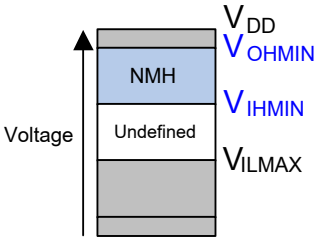
Table 2.1. Symbols of logic elements' states

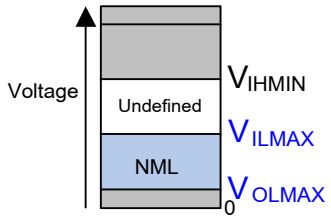
Symbol	State
L ("0")	LOW Logic Level
H ("1")	HIGH Logic Level
Z	High-impedance State
LH ("0"→"1")	LOW to HIGH Transition
HL ("1"→"0")	HIGH to LOW Transition
X	Either HIGH or LOW Logic Level

DC parameters and measurement conditions of the elements included in SAED_EDK90_CORE Digital Standard Cell Library are shown in Table 2.2.

Table 2.2. DC Parameters and measurement conditions of digital cells

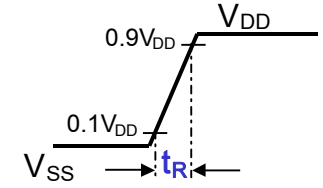
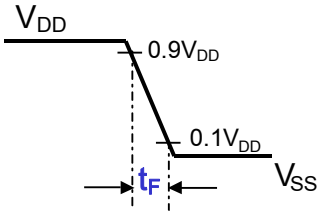
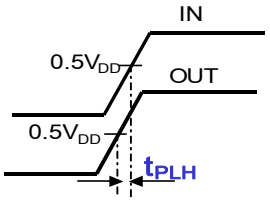
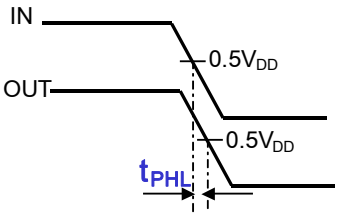
No	Parameter	Unit	Symbol	Figure	Definition
1	Voltage Transfer Characteristic	-	VTC		DC functional dependence between input and output voltages.
2	Output high level voltage (nominal)	V	$V_{OHN}=V_{DD}$		Output high voltage at nominal condition, usually equals to V_{DD}
3	Output low level voltage (nominal)	V	$V_{OLN}=0$ ($V_{OLN}=V_{SS}$)		Output low voltage at nominal condition, usually $V_{OLN}=0$

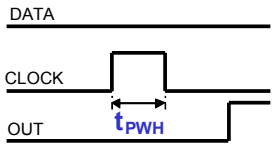
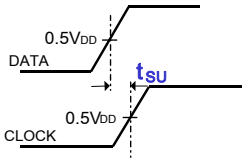
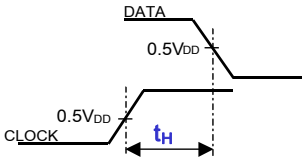
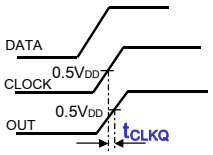
No	Parameter	Unit	Symbol	Figure	Definition
4	Switching point voltage	V	V_{SP}		Point on VTC where $V_{OUT}=V_{IN}$
5	Output high level minimum voltage	V	V_{OHMIN}		Highest output voltage at slope= -1.
6	Output low level maximum voltage	V	V_{OLMAX}		Lowest output voltage at slope= -1
7	Input minimum high voltage	V	V_{IHMIN}		Highest input voltage at slope = -1
8	Input maximum low voltage	V	V_{ILMAX}		Lowest input voltage at slope = -1
9	High state noise margin	V	NMH= =V_{OHMIN}- V_{IHMIN}		The maximum input noise voltage which does not change the output state when its value is subtracted from the input high level voltage

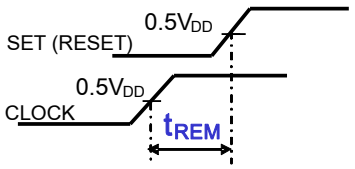
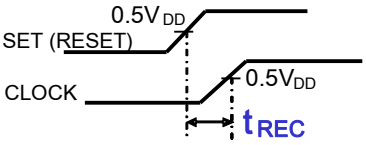
No	Parameter	Unit	Symbol	Figure	Definition
10	Low state noise margin	V	NML= =V_{ILMAX}- V_{OLMAX}		The maximum input noise voltage which does not change the output state when added to the input low level voltage
11	Static leakage current consumption at output on high state	uA	I_{LEAKH}	None	The current consumed when the output is high
		uA	I_{LEAKL}	None	The current consumed when the output is low
12	Leakage power consumption (dissipation) at output	pW	P_{LEAKH}= =V_{DD} x I_{LEAKH}	None	The power consumed when the output is high
		pW	P_{LEAKL}= =V_{DD} x I_{LEAKL}	None	The power consumed when the output is low

AC parameters and measurement conditions of the elements included in SAED_EDK90_CORE Digital Standard Cell Library are shown in Table 2.3.

Table 2.3. AC Parameters and measurement conditions of digital cells

No	Parameter	Unit	Symbol	Figure	Definition
1	Rise transition time	ns	t_R		The time it takes a driving pin to make a transition from kV_{DD} to $(1-k)V_{DD}$ value. Usually k=0.1 (also possible k=0.2, 0.3, etc)
2	Fall transition time	ns	t_F		The time it takes a driving pin to make a transition from $(1-k)V_{DD}$ to kV_{DD} value. Usually k=0.1 (also possible k=0.2, 0.3, etc)
3	Propagation delay low-to-high (Rise propagation)	ns	t_{PLH} (t_{PR})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from low to high
4	Propagation delay high-to-low (Fall propagation)	ns	t_{PHL} (t_{PF})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from high to low

No	Parameter	Unit	Symbol	Figure	Definition
5	Average supply current	uA	$I_{V_{DD}AVG} = \int_0^T I_{V_{DD}}(t)dt$	None	The power supply current average value for a period (T)
6	Supply peak current	uA	$I_{VDDPEAK}$= =max(I_{VDD}(t)) t∈[0;T]	None	The peak value of power supply current within one period (T)
7	Dynamic power dissipation	pW	P_{DISDYN}= =I_{VDDAVG} x V_{DD}	None	The average power consumed from the power supply
8	Power-delay product	nJ	PD=P_{DISDYN} x x max (t_{PHL},t_{PLH})	None	The product of consumed power and the largest propagation delay
9	Energy-delay product	nJs	ED=PD x x max(t_{PHL},t_{PLH})	None	The product of PD and the largest propagation delay
10	Switching fall power	nJ	P_{SWF} = =(C_{LOAD}+C_{OUTF}) x x V_{DD}^2/2	None	The energy dissipated on a fall transition. (C_{OUTF} is the output fall capacitance)
11	Switching rise power	nJ	P_{SWR}= =(C_{LOAD}+C_{OUTR}) x x V_{DD}^2/2	None	The energy dissipated on a rise transition. (C_{OUTR} is the output rise capacitance)
12	Minimum clock pulse (only for flip-flops or latches)	ns	t_{PWH} (t_{PWL})		The time interval during which the clock signal is high or low, so that it ensures proper operation of a flip-flop or a latch
13	Setup time (only for flip-flops or latches)	ns	t_{SU}		The minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs
14	Hold time (only for flip-flops or latches)	ns	t_H		The minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred
15	Clock-to-output time (only for flip-flops or latches)	ns	t_{CLKQ}		The amount of time that takes the output signal to change after clock's active edge is applied

No	Parameter	Unit	Symbol	Figure	Definition
16	Removal time (only for flip-flops or latches with asynchronous Set or Reset).	ns	t_{REM}		The minimum time in which the asynchronous Set or Reset pin to a flip-flop or latch must remain enabled after the active edge of the clock has occurred
17	Recovery time (only for flip-flops and latches with asynchronous Set or Reset)	ns	t_{REC}		The minimum time in which Set or Reset must be held stable after being deasserted before next active edge of the clock occurs
18	From high to Z-state entry time, (only for tri-state output cells)	ns	t_{HZ}	None	The amount of time that takes the output to change from high to Z-state after control signal is applied
19	From low to Z-state entry time, (only for tri-state output cells)	ns	t_{LZ}	None	The amount of time that takes the output to change from low to Z-state after control signal is applied
20	From Z to high-state exit time (only for tri-state output cells)	ns	t_{ZH}	None	The amount of time that takes the output to change from Z to high-state after control signal is applied
21	From Z to low-state exit time (only for tri-state output cells)	ns	t_{ZL}	None	The amount of time that takes the output to change from Z to low-state after control signal is applied
22	Input pin capacitance	pF	C_{IN}	None	Defines the load of an output pin
23	Maximum capacitance	pF	C_{MAX}	None	Defines the maximum total capacitive load that an output pin can drive

3. Operating conditions

SAED_EDK90_CORE Digital Standard Cell Library is anticipated for 1.2V operation. The used process technology is SAED90nm 1P9M 1.2V/2.5V/3.3V, but only the 1P1M option is used.

The operating conditions of SAED_EDK90_CORE Digital Standard Cell Library are shown in

Table 3.1. Operating conditions

Parameter	Min	Typ	Max	Units
Power Supply (VDD) range	0.7	1.2	1.32	V
Operating Temperature range	-40	+25	+125	°C
Operating Frequency (F)	-	300	-	MHz

4. Input signal slope, standard load and drive strengths

Standard load (C_{sl}) has been selected as the input pin capacitance of INVX1 cell. The INVX1 cell itself is tuned to drive 4 loads.

Table 4.1. Definition of drive strength

Drive Strength	Cell Load
X0	0.5x C_{sl}
X1	1x C_{sl}
X2	2x C_{sl}
X3	3x C_{sl}
X4	4x C_{sl}
X8	8x C_{sl}
X12	12x C_{sl}
X16	16x C_{sl}
X24	24x C_{sl}
X32	32x C_{sl}

5. AC Characteristics

5.1. Characterization corners

Composite Current Source (CCS) modeling technology has been applied for characterization to meet the contemporary methods of low power design. The application of that technology supports timing, noise, and power analyses simultaneously with consideration of the relevant nanometer dependencies. It allows meeting the requirements of variation-aware analysis.
The characterization results are given for 27 process/voltage/temperature (PVT) conditions shown in Table 5.1 and 45 process/voltage/temperature conditions for multi voltage cells.

Table 5.1. Base Characterization Corners

Corner Name	Process (NMOS proc. – PMOS proc.)	Temperature (^{0}C)	Power Supply (V)	Notes	Library Name Prefix
TTNT1p20v	Typical - Typical	25	1.2	Typical corner	Typ
TTHT1p20v	Typical - Typical	125	1.2	Typical corner	typ_ht
TTLT1p20v	Typical - Typical	-40	1.2	Typical corner	typ_ltl
SSNT1p08v	Slow - Slow	25	1.08	Slow corner	max_nth
SSHT1p08v	Slow - Slow	125	1.08	Slow corner	max_hth
SSLT1p08v	Slow - Slow	-40	1.08	Slow corner	max_lth
FFNT1p32v	Fast - Fast	25	1.32	Fast corner	min_nt
FFHT1p32v	Fast - Fast	125	1.32	Fast corner	min_ht
FFLT1p32v	Fast - Fast	-40	1.32	Fast corner	min
Middle Voltage Operating Conditions					
TTNT0p75v	Typical - Typical	25	0.75	Typical corner	typ_tm
TTHT0p75v	Typical - Typical	125	0.75	Typical corner	typ_htm
TTLT0p75v	Typical - Typical	-40	0.75	Typical corner	typ_ltm
SSNT0p65v	Slow - Slow	25	0.65	Slow corner	max_tm
SSHT0p65v	Slow - Slow	125	0.65	Slow corner	max_htm
SSLT0p65v	Slow - Slow	-40	0.65	Slow corner	max_ltm
FFNT0p85v	Fast - Fast	25	0.85	Fast corner	min_tm
FFHT0p85v	Fast - Fast	125	0.85	Fast corner	min_htm
FFLT0p85v	Fast - Fast	-40	0.85	Fast corner	min_ltm
Low Voltage Operating Conditions					
TTNT0p08v	Typical - Typical	25	0.8	Typical corner	typ_ntl
TTHT0p08v	Typical - Typical	125	0.8	Typical corner	typ_htl
TTLT0p08v	Typical - Typical	-40	0.8	Typical corner	typ_ltl
SSNT0p07v	Slow - Slow	25	0.7	Slow corner	max_nt
SSHT0p07v	Slow - Slow	125	0.7	Slow corner	max
SSLT0p07v	Slow - Slow	-40	0.7	Slow corner	max_lt
FFNT0p09v	Fast - Fast	25	0.9	Fast corner	min_ntl
FFHT0p09v	Fast - Fast	125	0.9	Fast corner	min_htl
FFLT0p09v	Fast - Fast	-40	0.9	Fast corner	min_ltl

The Level Shifters were characterized for the foloving corners:

Table 5.2. Multi-VDD characterization corners

Corner Name	Process (NMOS proc. – PMOS proc.)	Temperature (^{0}C)	Power Supply1 (V)	Power Supply2 (V)	Notes	Library Name
FFHT1p32v1p32v	Fast-Fast	125	1.32	1.32	Fast corner	min_hthh
FFHT1p32v0p90v	Fast-Fast	125	1.32	0.9	Fast corner	min_hthn
FFHT0p90v0p90v	Fast-Fast	125	0.9	0.9	Fast corner	min_htln
FFNT1p32v1p32v	Fast-Fast	25	1.32	1.32	Fast corner	min_nthh
FFNT1p32v0p90v	Fast-Fast	25	1.32	0.9	Fast corner	min_nthn
FFNT0p90v0p90v	Fast-Fast	25	0.9	0.9	Fast corner	min_ntln
FFLT1p32v1p32v	Fast-Fast	-40	1.32	1.32	Fast corner	min_lthh
FFLT1p32v0p90v	Fast-Fast	-40	1.32	0.9	Fast corner	min_lthn
FFLT0p90v0p90v	Fast-Fast	-40	0.9	0.9	Fast corner	min_ltln
TTHT1p20v1p20v	Typical-Typical	125	1.2	1.2	Typical corner	typ_hthh
TTHT1p20v0p80v	Typical-Typical	125	1.2	0.8	Typical corner	typ_hthn
TTHT0p80v0p80v	Typical-Typical	125	0.8	0.8	Typical corner	typ_htln
TTNT1p20v1p20v	Typical-Typical	25	1.2	1.2	Typical corner	typ_nthh
TTNT1p20v0p80v	Typical-Typical	25	1.2	0.8	Typical corner	typ_nthn
TTNT0p80v0p80v	Typical-Typical	25	0.8	0.8	Typical corner	typ_ntln
TTLT1p20v1p20v	Typical-Typical	-40	1.2	1.2	Typical corner	typ_lthh
TTLT1p20v0p80v	Typical-Typical	-40	1.2	0.8	Typical corner	typ_lthn
TTLT0p80v0p80v	Typical-Typical	-40	0.8	0.8	Typical corner	typ_ltln
SSHT1p08v1p08v	Slow-Slow	125	1.08	1.08	Slow corner	max_hthh
SSHT1p08v0p70v	Slow-Slow	125	1.08	0.7	Slow corner	max_hthn
SSHT0p70v0p70v	Slow-Slow	125	0.7	0.7	Slow corner	max_htln
SSNT1p08v1p08v	Slow-Slow	25	1.08	1.08	Slow corner	max_nthh
SSNT1p08v0p70v	Slow-Slow	25	1.08	0.7	Slow corner	max_nthn
SSNT0p70v0p70v	Slow-Slow	25	0.7	0.7	Slow corner	max_ntln
SSLT1p08v1p08v	Slow-Slow	-40	1.08	1.08	Slow corner	max_lthh
SSLT1p08v0p70v	Slow-Slow	-40	1.08	0.7	Slow corner	max_lthn
SSLT0p70v0p70v	Slow-Slow	-40	0.7	0.7	Slow corner	max_ltln
FFHT1p32v0p85v	Fast-Fast	125	1.32	0.85	Fast corner	min_thm
FFHT0p85v0p85v	Fast-Fast	125	0.85	0.85	Fast corner	min_htmm
FFNT1p32v0p85v	Fast-Fast	25	1.32	0.85	Fast corner	min_nthm
FFNT0p85v0p85v	Fast-Fast	25	0.85	0.85	Fast corner	min_ntmm
FFLT1p32v0p85v	Fast-Fast	-40	1.32	0.85	Fast corner	min_lthm
FFLT0p85v0p85v	Fast-Fast	-40	0.85	0.85	Fast corner	min_ltmm
TTHT1p20v0p75v	Typical-Typical	125	1.2	0.75	Typical corner	typ_hthm
TTHT0p75v0p75v	Typical-Typical	125	0.75	0.75	Typical corner	typ_htmm
TTNT1p20v0p75v	Typical-Typical	25	1.2	0.75	Typical corner	typ_nthm
TTNT0p75v0p75v	Typical-Typical	25	0.75	0.75	Typical corner	typ_ntmm
TTLT1p20v0p75v	Typical-Typical	-40	1.2	0.75	Typical corner	typ_lthm
TTLT0p75v0p75v	Typical-Typical	-40	0.75	0.75	Typical corner	typ_ltmm
SSHT1p08v0p65v	Slow-Slow	125	1.08	0.65	Slow corner	max_hthm
SSHT0p65v0p65v	Slow-Slow	125	0.65	0.65	Slow corner	max_htmm
SSNT1p08v0p65v	Slow-Slow	25	1.08	0.65	Slow corner	max_nthm
SSNT0p65v0p65v	Slow-Slow	25	0.65	0.65	Slow corner	max_ntmm
SSLT1p08v0p65v	Slow-Slow	-40	1.08	0.65	Slow corner	max_lthm
SSNT0p65v0p65v	Slow-Slow	-40	0.65	0.65	Slow corner	max_ltmm

5.2. The values of Output Load and Input Slope

Characterization has been realized for 7 different values of Output Load and 7 different values of Input Slope shown in Table 5.3.

Table 5.3 The values used for characterization

Parameter	Value						
Output Load	0	$0.5*C_{sl}$	$1*C_{sl}$	$2*C_{sl}$	$4*C_{sl}$	$8*C_{sl}$	$16*C_{sl}$
Input Slope (ns)	$0.2*T_{isl}$	$0.4*T_{isl}$	$0.8*T_{isl}$	$1.6*T_{isl}$	$3.2*T_{isl}$	$6.4*T_{isl}$	$12.8*T_{isl}$

The calculation of Setup/Hold times has been realized for 3 different values of Data and Input Slopes shown in Table 5.4.

Table 5.4 The used values for calculating Setup/Hold Times

Parameter	Slope Values (ns)						
Data Input Slope	$0.2*T_{isl}$	$0.4*T_{isl}$	$0.8*T_{isl}$	$1.6*T_{isl}$	$3.2*T_{isl}$	$6.4*T_{isl}$	$12.8*T_{isl}$
Clock Input Slope	$0.2*T_{isl}$	$0.4*T_{isl}$	$0.8*T_{isl}$	$1.6*T_{isl}$	$3.2*T_{isl}$	$6.4*T_{isl}$	$12.8*T_{isl}$

6. Digital Standard Library Cell List

SAED_EDK90_CORE Digital Standard Cell Library contains 340 cells in total, the list of which is shown in Table 6.1.

Table 6.1. Digital Standard Library Cell List

No	Cell Description	Cell Name
	Inverters, Buffers	
1	Inverter	INVX0
2	Inverter	INVX1
3	Inverter	INVX2
4	Inverter	INVX4
5	Inverter	INVX8
6	Inverter	INVX16
7	Inverter	INVX32
8	Inverting Buffer	IBUFFX2
9	Inverting Buffer	IBUFFX4
10	Inverting Buffer	IBUFFX8
11	Inverting Buffer	IBUFFX16
12	Inverting Buffer	IBUFFX32
13	Non-inverting Buffer	NBUFFX2
14	Non-inverting Buffer	NBUFFX4
15	Non-inverting Buffer	NBUFFX8
16	Non-inverting Buffer	NBUFFX16
17	Non-inverting Buffer	NBUFFX32
18	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX1
19	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX2
20	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX4
21	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX8
22	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX16
23	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX32
	Logic Gates	
24	AND 2-input	AND2X1
25	AND 2-input	AND2X2
26	AND 2-input	AND2X4
27	AND 3-input	AND3X1
28	AND 3-input	AND3X2
29	AND 3-input	AND3X4
30	AND 4-input	AND4X1
31	AND 4-input	AND4X2
32	AND 4-input	AND4X4
33	NAND 2-input	NAND2X0
34	NAND 2-input	NAND2X1
35	NAND 2-input	NAND2X2

No	Cell Description	Cell Name
36	NAND 2-input	NAND2X4
37	NAND 3-input	NAND3X0
38	NAND 3-input	NAND3X1
39	NAND 3-input	NAND3X2
40	NAND 3-input	NAND3X4
41	NAND 4-input	NAND4X0
42	NAND 4-input	NAND4X1
43	OR 2-input	OR2X1
44	OR 2-input	OR2X2
45	OR 2-input	OR2X4
46	OR 3-input	OR3X1
47	OR 3-input	OR3X2
48	OR 3-input	OR3X4
49	OR 4-input	OR4X1
50	OR 4-input	OR4X2
51	OR 4-input	OR4X4
52	NOR 2-input	NOR2X0
53	NOR 2-input	NOR2X1
54	NOR 2-input	NOR2X2
55	NOR 2-input	NOR2X4
56	NOR 3-input	NOR3X0
57	NOR 3-input	NOR3X1
58	NOR 3-input	NOR3X2
59	NOR 3-input	NOR3X4
60	NOR 4-input	NOR4X0
61	NOR 4-input	NOR4X1
62	XOR 2-input	XOR2X1
63	XOR 2-input	XOR2X2
64	XOR 3-input	XOR3X1
65	XOR 3-input	XOR3X2
66	XNOR 2-input	XNOR2X1
67	XNOR 2-input	XNOR2X2
68	XNOR 3-input	XNOR3X1
69	XNOR 3-input	XNOR3X2
	Complex Logic Gates	
70	AND-OR 2/1	AO21X1
71	AND-OR 2/1	AO21X2
72	AND-OR 2/2	AO22X1
73	AND-OR 2/2	AO22X2
74	AND-OR 2/2/1	AO221X1

No	Cell Description	Cell Name
75	AND-OR 2/2/1	AO221X2
76	AND-OR 2/2/2	AO222X1
77	AND-OR 2/2/2	AO222X2
78	AND-OR-Invert 2/1	AOI21X1
79	AND-OR Invert 2/1	AOI21X2
80	AND-OR-Invert 2/2	AOI22X1
81	AND-OR-Invert 2/2	AOI22X2
82	AND-OR-Invert 2/2/1	AOI221X1
83	AND-OR-Invert 2/2/1	AOI221X2
84	AND-OR-Invert 2/2/2	AOI222X1
85	AND-OR-Invert 2/2/2	AOI222X2
86	OR-AND 2/1	OA21X1
87	OR-AND 2/1	OA21X2
88	OR-AND 2/2	OA22X1
89	OR-AND 2/2	OA22X2
90	OR-AND 2/2/1	OA221X1
91	OR-AND 2/2/1	OA221X2
92	OR-AND 2/2/2	OA222X1
93	OR-AND 2/2/2	OA222X2
94	OR-AND-Invert 2/1	OAI21X1
95	OR-AND-Invert 2/1	OAI21X2
96	OR-AND-Invert 2/2	OAI22X1
97	OR-AND-Invert 2/2	OAI22X2
98	OR-AND-Invert 2/2/1	OAI221X1
99	OR-AND-Invert 2/2/1	OAI221X2
100	OR-AND-Invert 2/2/2	OAI222X1
101	OR-AND-Invert 2/2/2	OAI222X2
	Multiplexers	
102	Multiplexer 2 to 1	MUX21X1
103	Multiplexer 2 to 1	MUX21X2
104	Multiplexer 4 to 1	MUX41X1
105	Multiplexer 4 to 1	MUX41X2
	Decoders	
106	Decoder 2 to 4	DEC24X1
107	Decoder 2 to 4	DEC24X2
	Adders and Subtractors	
108	Half Adder 1 bit	HADDX1
109	Half Adder 1 bit	HADDX2
110	Full Adder 1 bit	FADDX1
111	Full Adder 1 bit	FADDX2

No	Cell Description	Cell Name
	D Flip-Flops	
112	Pos Edge DFF	DFFX1
113	Pos Edge DFF	DFFX2
114	Pos Edge DFF, w/ Async Low-Active Set	DFFASX1
115	Pos Edge DFF, w/ Async Low-Active Set	DFFASX2
116	Pos Edge DFF, w/ Async Low-Active Reset	DFFARX1
117	Pos Edge DFF, w/ Async Low-Active Reset	DFFARX2
118	Pos Edge DFF, w/ Async Low-Active Set & Reset	DFFASRX1
119	Pos Edge DFF, w/ Async Low-Active Set & Reset	DFFASRX2
120	Pos Edge DFF, w/ Sync Low-Active Set & Reset	DFFSSRX1
121	Pos Edge DFF, w/ Sync Low-Active Set & Reset	DFFSSRX2
122	Neg Edge DFF	DFFNX1
123	Neg Edge DFF	DFFNX2
124	Neg Edge DFF, w/ Async Low-Active Set	DFFNASX1
125	Neg Edge DFF, w/ Async Low-Active Set	DFFNASX2
126	Neg Edge DFF, w/ Async Low-Active Reset	DFFNARX1
127	Neg Edge DFF, w/ Async Low-Active Reset	DFFNARX2
128	Neg Edge DFF, w/ Async Low-Active Set & Reset	DFFNASRX1
129	Neg Edge DFF, w/ Async Low-Active Set & Reset	DFFNASRX2
130	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out	DFFNASRQX1
131	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out	DFFNASRQX2
132	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out	DFFNASRNX1
133	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out	DFFNASRNX2
	Scan D Flip-Flops	
134	Scan Pos Edge DFF	SDFFX1
135	Scan Pos Edge DFF	SDFFX2
136	Scan Pos Edge DFF, w/ Async Low-Active Set	SDFFASX1
137	Scan Pos Edge DFF, w/ Async Low-Active Set	SDFFASX2
138	Scan Pos Edge DFF, w/ Async Low-Active Reset	SDFFARX1
139	Scan Pos Edge DFF, w/ Async Low-Active Reset	SDFFARX2
140	Scan Pos Edge DFF, w/ Async Low-Active Set & Reset	SDFFASRX1
141	Scan Pos Edge DFF, w/ Async Low-Active Set & Reset	SDFFASRX2
142	Scan Pos Edge DFF, w/ Async Low-Active Set & Reset, Q, QN, & S0 outs	SDFFASRSX1
143	Scan Pos Edge DFF, w/ Async Low-Active Set & Reset, Q, QN, & S0 outs	SDFFASRSX2
144	Scan Pos Edge DFF, w/ Sync Low-Active Set & Reset	SDFFSSRX1
145	Scan Pos Edge DFF, w/ Sync Low-Active Set & Reset	SDFFSSRX2
146	Scan Neg Edge DFF	SDFFNX1
147	Scan Neg Edge DFF	SDFFNX2
148	Scan Neg Edge DFF, w/ Async Low-Active Set	SDFFNASX1
149	Scan Neg Edge DFF, w/ Async Low-Active Set	SDFFNASX2
150	Scan Neg Edge DFF, w/ Async Low-Active Reset	SDFFNARX1

No	Cell Description	Cell Name
151	Scan Neg Edge DFF, w/ Async Low-Active Reset	SDFFNARX2
152	Scan Neg Edge DFF, w/ Async Low-Active Set & Reset	SDFFNASRX1
153	Scan Neg Edge DFF, w/ Async Low-Active Set & Reset	SDFFNASRX2
	Latches	
154	RS NAND Latch	LNANDX1
155	RS NAND Latch	LNANDX2
156	High-Active Latch	LATCHX1
157	High-Active Latch	LATCHX2
158	High-Active Latch, w/ Async Low-Active Set	LASX1
159	High-Active Latch, w/ Async Low-Active Set	LASX2
160	High-Active Latch, w/ Async Low-Active Reset	LARX1
161	High-Active Latch, w/ Async Low-Active Reset	LARX2
162	High-Active Latch, w/ Async Low-Active Set & Reset	LASRX1
163	High-Active Latch, w/ Async Low-Active Set & Reset	LASRX2
164	High-Active Latch ,w/ Async Low-Active Set & Reset only Q out	LASRQX1
165	High-Active Latch, w/ Async Low-Active Set & Reset only Q out	LASRQX2
166	High-Active Latch, w/ Async Low-Active Set & Reset only QN out	LASRNX1
167	High-Active Latch, w/ Async Low-Active Set & Reset only QN out	LASRNX2
	Clocked Gates	
168	Clock Gating cell, w/ Latched Pos Edge Control Post	CGLPPSX2
169	Clock Gating cell, w/ Latched Pos Edge Control Post	CGLPPSX4
170	Clock Gating cell, w/ Latched Pos Edge Control Post	CGLPPSX8
171	Clock Gating cell, w/ Latched Pos Edge Control Post	CGLPPSX16
172	Clock Gating cell, w/ Latched Neg Edge Control Post	CGLNPSX2
173	Clock Gating cell, w/ Latched Neg Edge Control Post	CGLNPSX4
174	Clock Gating cell, w/ Latched Neg Edge Control Post	CGLNPSX8
175	Clock Gating cell, w/ Latched Neg Edge Control Post	CGLNPSX16
176	Clock Gating cell ,w/ Latched Pos Edge Control Pre	CGLPPRX2
177	Clock Gating cell ,w/ Latched Pos Edge Control Pre	CGLPPRX8
178	Clock Gating cell ,w/ Latched Neg Edge Control Pre	CGLNPRX2
179	Clock Gating cell, w/ Latched Neg Edge Control Pre	CGLNPRX8
	Delay Lines	
180	Non-inverting Delay Line, 250 ps	DELLN1X2
181	Non-inverting Delay Line, 500 ps	DELLN2X2
182	Non-inverting Delay Line, 750 ps	DELLN3X2
	Pass Gates	
183	Pass Gate	PGX1
184	Pass Gate	PGX2
185	Pass Gate	PGX4
	Bi-directional Switches	
186	Bi-directional Switch w/ Low-Active Enable	BSLEX1
187	Bi-directional Switch w/ Low-Active Enable	BSLEX2

No	Cell Description	Cell Name
188	Bi-directional Switch w/ Low-Active Enable	BSLEX4
	Isolation Cells	
189	Hold 0 Isolation Cell (Logic AND)	ISOLANDX1
190	Hold 0 Isolation Cell (Logic AND)	ISOLANDX2
191	Hold 0 Isolation Cell (Logic AND)	ISOLANDX4
192	Hold 0 Isolation Cell (Logic AND)	ISOLANDX8
193	Hold 0 Isolation Cell (Logic AND),Always On	ISOLANDAOX1
194	Hold 0 Isolation Cell (Logic AND),Always On	ISOLANDAOX2
195	Hold 0 Isolation Cell (Logic AND),Always On	ISOLANDAOX4
196	Hold 0 Isolation Cell (Logic AND),Always On	ISOLANDAOX8
197	Hold 1 Isolation Cell (Logic OR)	ISOLORX1
198	Hold 1 Isolation Cell (Logic OR)	ISOLORX2
199	Hold 1 Isolation Cell (Logic OR)	ISOLORX4
200	Hold 1 Isolation Cell (Logic OR),	ISOLORX8
201	Hold 1 Isolation Cell (Logic OR),Always On	ISOLORAOX1
202	Hold 1 Isolation Cell (Logic OR),Always On	ISOLORAOX2
203	Hold 1 Isolation Cell (Logic OR),Always On	ISOLORAOX4
204	Hold 1 Isolation Cell (Logic OR),Always On	ISOLORAOX8
	Level Shifters	
205	Low to High Level Shifter	LSUPX1
206	Low to High Level Shifter	LSUPX2
207	Low to High Level Shifter	LSUPX4
208	Low to High Level Shifter	LSUPX8
209	High to Low Level Shifter	LSDNX1
210	High to Low Level Shifter	LSDNX2
211	High to Low Level Shifter	LSDNX4
212	High to Low Level Shifter	LSDNX8
213	Low to High Level Shifter/ High-Active Enable, Clamp High	LSUPENX1
214	Low to High Level Shifter/ High-Active Enable, Clamp High	LSUPENX2
215	Low to High Level Shifter/ High-Active Enable, Clamp High	LSUPENX4
216	Low to High Level Shifter/ High-Active Enable, Clamp High	LSUPENX8
217	High to Low Level Shifter/ High-Active Enable, Clamp High	LSDNENX1
218	High to Low Level Shifter/ High-Active Enable, Clamp High	LSDNENX2
219	High to Low Level Shifter/ High-Active Enable, Clamp High	LSDNENX4
220	High to Low Level Shifter/ High-Active Enable, Clamp High	LSDNENX8
221	Low to High Level Shifter/ High-Active Enable, Clamp Low	LSUPENCLX1
222	Low to High Level Shifter/ High-Active Enable, Clamp Low	LSUPENCLX2
223	Low to High Level Shifter/ High-Active Enable, Clamp Low	LSUPENCLX4
224	Low to High Level Shifter/ High-Active Enable, Clamp Low	LSUPENCLX8
225	High to Low Level Shifter/ High-Active Enable, Clamp Low	LSDNENCLX1
226	High to Low Level Shifter/ High-Active Enable, Clamp Low	LSDNENCLX2
227	High to Low Level Shifter/ High-Active Enable, Clamp Low	LSDNENCLX4

No	Cell Description	Cell Name
228	High to Low Level Shifter/ High-Active Enable, Clamp Low	LSDNENCLX8
229	High to Low Level Shifter/Single Supply	LSDNSSX1
230	High to Low Level Shifter/Single Supply	LSDNSSX2
231	High to Low Level Shifter/Single Supply	LSDNSSX3
232	High to Low Level Shifter/Single Supply	LSDNSSX4
233	High to Low Level Shifter/High-Active Enable,Single Supply	LSDNENSSX1
234	High to Low Level Shifter/High-Active Enable,Single Supply	LSDNENSSX2
235	High to Low Level Shifter/High-Active Enable,Single Supply	LSDNENSSX4
236	High to Low Level Shifter/High-Active Enable,Single Supply	LSDNENSSX8
237	High to Low Level Shifter/High-Active Enable, Clamp Low, Single Supply	LSDNENCLSSX1
238	High to Low Level Shifter/High-Active Enable, Clamp Low, Single Supply	LSDNENCLSSX2
239	High to Low Level Shifter/High-Active Enable, Clamp Low, Single Supply	LSDNENCLSSX4
240	High to Low Level Shifter/High-Active Enable, Clamp Low, Single Supply	LSDNENCLSSX8
	Retention Flip-Flops and scan Flip-Flops	
241	Pos Edge Retention DFF	RDFFX1
242	Pos Edge Retention DFF	RDFFX2
243	Scan Pos Edge Retention DFF	RSDFFX1
244	Scan Pos Edge Retention DFF	RSDFFX2
245	Neg Edge Retention DFF	RDFFNX1
246	Neg Edge Retention DFF	RDFFNX2
247	Scan Neg Edge Retention DFF	RSDFFNX1
248	Scan Neg Edge Retention DFF	RSDFFNX2
249	Scan Pos Edge Retention DFF ,w/ Async Low-Active Reset	RSDFFARX1
250	Scan Pos Edge Retention DFF ,w/ Async Low-Active Reset	RSDFFARX2
251	Scan Neg Edge Retention DFF,w/ Async Low-Active Reset	RSDFFNARX1
252	Scan Neg Edge Retention DFF,w/ Async Low-Active Reset	RSDFFNARX2
253	Pos Edge Retention DFF, w/ Async Low-Active Reset	RDFFARX1
254	Pos Edge Retention DFF, w/ Async Low-Active Reset	RDFFARX2
255	Neg Edge Retention DFF, w/ Async Low-Active Reset	RDFFNARX1
256	Neg Edge Retention DFF, w/ Async Low-Active Reset	RDFFNARX2
	Retention D Flip-Flops with Save and Restore pins	
257	Pos Edge DFF SR	RDFFSRX1
258	Pos Edge DFF SR	RDFFSRX2
259	Pos Edge DFF SR, w/ Async Low-Active Set	RDFFSRASX1
260	Pos Edge DFF SR, w/ Async Low-Active Set	RDFFSRASX2
261	Pos Edge DFF SR, w/ Async Low-Active Reset	RDFFSRARX1
262	Pos Edge DFF SR, w/ Async Low-Active Reset	RDFFSRARX2
263	Pos Edge DFF SR, w/ Async Low-Active Set & Reset	RDFFSRASRX1
264	Pos Edge DFF SR, w/ Async Low-Active Set & Reset	RDFFSRASRX2

No	Cell Description	Cell Name
265	Pos Edge DFF SR, w/ Sync Low-Active Set & Reset	RDFFSRSSRX1
266	Pos Edge DFF SR, w/ Sync Low-Active Set & Reset	RDFFSRSSRX2
267	Neg Edge DFF SR	RDFFNSRX1
268	Neg Edge DFF SR	RDFFNSRX2
269	Neg Edge DFF SR, w/ Async Low-Active Set	RDFFNSRASX1
270	Neg Edge DFF SR, w/ Async Low-Active Set	RDFFNSRASX2
271	Pos Edge DFF SR, w/ Async Low-Active Reset	RDFFNSRARX1
272	Pos Edge DFF SR, w/ Async Low-Active Reset	RDFFNSRARX2
273	Neg Edge DFF SR, w/ Async Low-Active Set & Reset	RDFFNSRASRX1
274	Neg Edge DFF SR, w/ Async Low-Active Set & Reset	RDFFNSRASRX2
275	Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out	RDFFNSRASRQX1
276	Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out	RDFFNSRASRQX2
277	Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out	RDFFNSRASRNX1
278	Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out	RDFFNSRASRNX2
	Scan Retention D Flip-Flops with Save and Restore pins	
279	Scan Pos Edge DFF SR	RSDFFSRX1
280	Scan Pos Edge DFF SR	RSDFFSRX2
281	Scan Pos Edge DFF SR, w/ Async Low-Active Set	RSDFFSRASX1
282	Scan Pos Edge DFF SR, w/ Async Low-Active Set	RSDFFSRASX2
283	Scan Pos Edge DFF SR, w/ Async Low-Active Reset	RSDFFSRARX1
284	Scan Pos Edge DFF SR, w/ Async Low-Active Reset	RSDFFSRARX2
285	Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset	RSDFFSRASRX1
286	Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset	RSDFFSRASRX2
287	Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset	RSDFFSRSSRX1
288	Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset	RSDFFSRSSRX2
289	Scan Neg Edge DFF SR	RSDFFNSRX1
290	Scan Neg Edge DFF SR	RSDFFNSRX2
291	Scan Neg Edge DFF SR, w/ Async Low-Active Set	RSDFFNSRASX1
292	Scan Neg Edge DFF SR, w/ Async Low-Active Set	RSDFFNSRASX2
293	Scan Pos Edge DFF SR , w/ Async Low-Active Reset	RSDFFNSRARX1
294	Scan Pos Edge DFF SR, w/ Async Low-Active Reset	RSDFFNSRARX2
295	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset	RSDFFNSRASRX1
296	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset	RSDFFNSRASRX2
297	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out	RSDFFNSRASRQX1
298	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out	RSDFFNSRASRQX2
299	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out	RSDFFNSRASRNX1
300	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out	RSDFFNSRASRNX2
	Power Gating Cells	
301	Header Cell	HEADX2

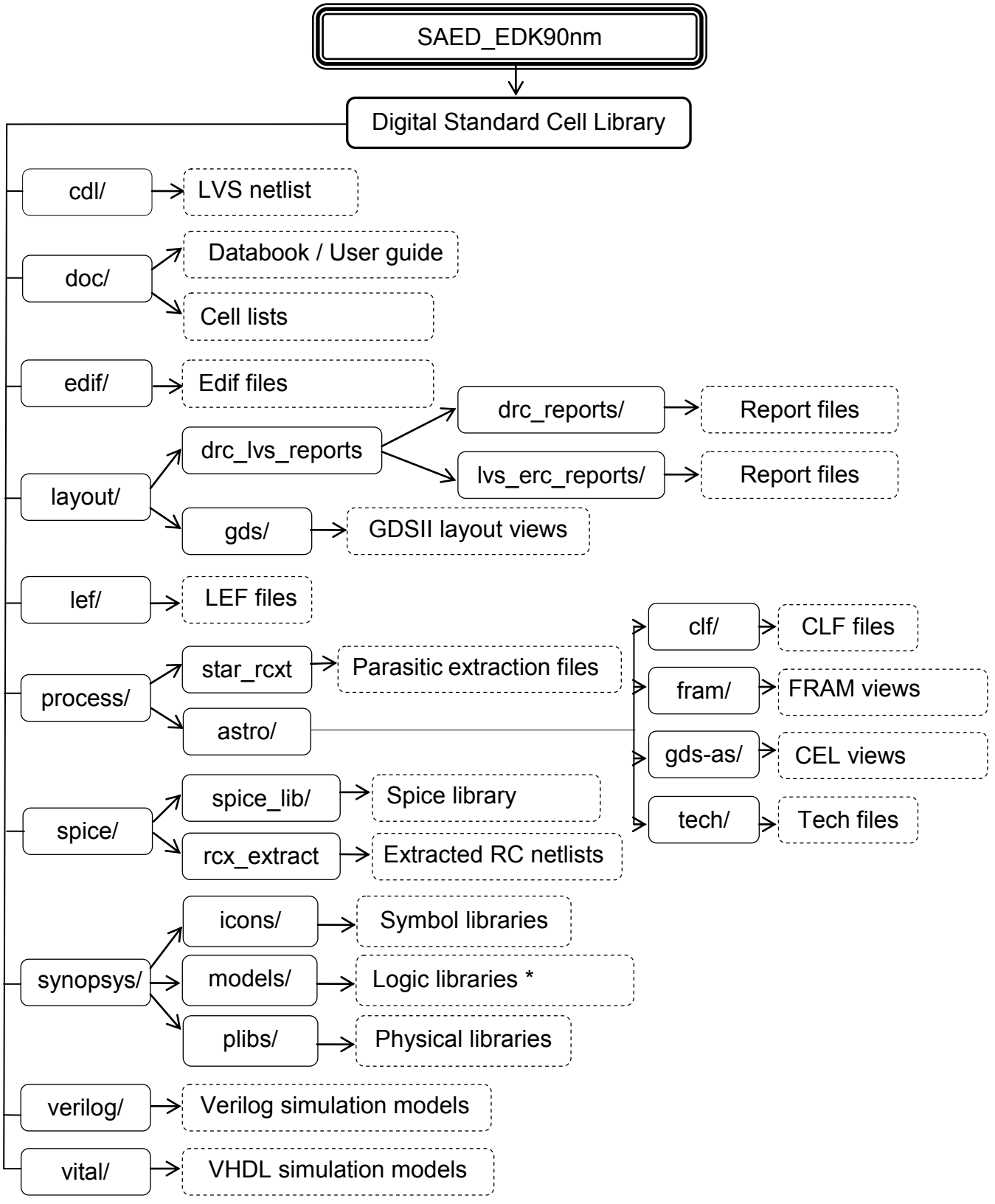
No	Cell Description	Cell Name
302	Header Cell	HEADX4
303	Header Cell	HEADX8
304	Header Cell	HEADX16
305	Header Cell	HEADX32
306	Header Cell (with SLEEPOUT output)	HEAD2X2
307	Header Cell (with SLEEPOUT output)	HEAD2X4
308	Header Cell (with SLEEPOUT output)	HEAD2X8
309	Header Cell (with SLEEPOUT output)	HEAD2X16
310	Header Cell (with SLEEPOUT output)	HEAD2X32
	Always on Cells	
311	Always on Inverter	AOINVX1
312	Always on Inverter	AOINVX2
313	Always on Inverter	AOINVX4
314	Always on Non-inverting Buffer	AOBUFX1
315	Always on Non-inverting Buffer	AOBUFX2
316	Always on Non-inverting Buffer	AOBUFX4
317	Always on Pos Edge DFF, w/ Async Low-Active Reset	AODFFARX1
318	Always on Pos Edge DFF, w/ Async Low-Active Reset	AODFFARX2
319	Always on Neg Edge DFF, w/ Async Low-Active Reset	AODFFNARX1
320	Always on Neg Edge DFF, w/ Async Low-Active Reset	AODFFNARX2
	Additional Cells	
321	Bus Keeper	BUSKP
322	P-MOSFET (w=1.12 um, l=0.1um)	PMT1
323	P-MOSFET (w=2.24 um, l=0.1um)	PMT2
324	P-MOSFET (w=4.48 um, l=0.1um)	PMT3
325	N-MOSFET (w=0.48 um, l=0.1um)	NMT1
326	N-MOSFET (w=0.96 um, l=0.1um)	NMT2
327	N-MOSFET (w=1.92 um, l=0.1um)	NMT3
328	Tie High	TIEH
329	Tie Low	TIEL
330	Antenna Diode	ANTENNA
331	Decoupling Capacitance	DCAP
332	Capacitive Load	CLOAD1
	Fillers	
333	Single Height Filler Cell 1 grid width	SHFILL1
334	Single Height Filler Cell 2 grid width	SHFILL2
335	Single Height Filler Cell 3 grid width	SHFILL3
336	Single Height Filler Cell 64 grid width	SHFILL64
337	Single Height Filler Cell 128 grid width	SHFILL128
338	Double Height (high-low-high) Filler Cell 2 grid width	DHFILLHLH2
339	Double Height (low-high-low) Filler Cell 2 grid width	DHFILLLHL2
340	Double Height (high-low-high) Level Shifter Filler Cell 11 grid width	DHFILLHLHLS11

7. Digital Standard Cell Library deliverables

Table 7.1. Digital Standard Cell Library deliverables

N	Type	Description
1	.doc, .txt	Databook / User guide, Layer usage file
2	.sdb, .slib	Symbols
3	.db, .lib	Synthesis
4	.v	Verilog simulation models
5	.vhd	VHDL / Vital simulation models
6	.sp	HSPICE netlists
7	.rcx	Extracted RC netlists for different corners
8	.gds	GDSII layout views
9	.drc, .lvs, .erc	Report files
10	.lef	LEF files
11	.fram, .cel	Fram views, layout views and runset files
12	.plib	Physical compiler views

8. Directory structure and file naming conventions



** See Table 8.2 for details*

Figure 8.1. Digital standard cell library directory structure

The Digital Standard Cell Library file naming conventions are shown in Table 8.1 and 8.2, words in parentheses are placeholders for cell types, threshold groups, etc. The interpretation can be found in the notes below the tables.

Table 8.1 Digital Standard Cell Library file naming conventions

N	Filenames	Extn	Example	Description
1	saed90nm(**a**)	.cdl	saed90nm_hvt.cdl	LVS netlists
3	saed90nm(**a**)	.edif	saed90nm_hvt.edif	Edif files
4	saed90nm(**a**)	.gds	saed90nm_hvt.gds	GDSII views
5	**cell name**(**a**)	_drcreports _lvsreports	INVX0_drcreports	Report Files
6	saed90nm(**a**)	.lef	saed90nm_hvt.lef	LEF files
7	saed90nm(**a**)	.spf	saed90nm_hvt.spf	Extracted RC netlists
8	saed90nm(**a**)	.v, .tv	saed90nm_hvt.v	Verilog simulation Models
9	saed90nm(**a**)	.vhd	saed90nm_hvt.vhd	VHDL simulation Models
10	saed90nm(**a**)	_fr, _dv	saed90nm_fr	MW reference Libraries
11	saed90nm	.sdb, .slib	saed90nm.sdb	Symbol libraries
12	saed90nm(**a**)	.pdb,.plib	saed90nm.pdb	Physical libraries

Notes: (**a**) –> *_hvt or _lvt* or empty (threshold voltage group*)*
cell name the same as Cell Name in the Table 6.1

Table 8.2 Logic libraries paths and file naming conventions

Cell type	Path	Library name
Isolation cells with Backup power	DSCL/isoao/	saed90nm_(**proc**)_(**tg**)_iso.db
Level shifters	DSCL/level_shiers/	saed90nm_(**proc**)_(**tg**)_lsh.db
Level shifters (single supply)	DSCL/level_shifters_ss/	saed90nm_(**proc**)_(**tg**)_lshss.db
Clock gating	DSCL/clock_gating/	saed90nm_(**proc**)_cg_(**tg**).db
Retention cells (single control)	DSCL/retention/	saed90nm_(**proc**)_rd_(**tg**).db
Retention cells (single control, asynchronous reset)	DSCL/retention/with_asynchron_reset/	saed90nm_(**proc**)_rdr_(**tg**).db
Retention cells with (SAVE/RESTORE control)	DSCL/retention_sr/	saed90nm_(**proc**)_(**tg**)_rdsr.db

*Notes: (**proc**) - library name prefix from the Tables 5.1 and 5.2*
*(**tg**) - _hvt or _lvt* or empty for denoting svt (threshold voltage group*)*
DSCL - Digital Standard Cell Library/synopsys/models

9. Physical structure of digital cell

The selection of physical structure of digital cell is aimed at providing maximum cell density in digital designs. It is more important to provide minimal area for the most frequently used cells. In general, these are usually NAND cells with two inputs, and D flip-flops. The width of the power rails has been selected on the basis of acceptable current density given by the design rules, and electromigration. Physical structures, shown in Fig.9.1-9.5, have been used for different cells.

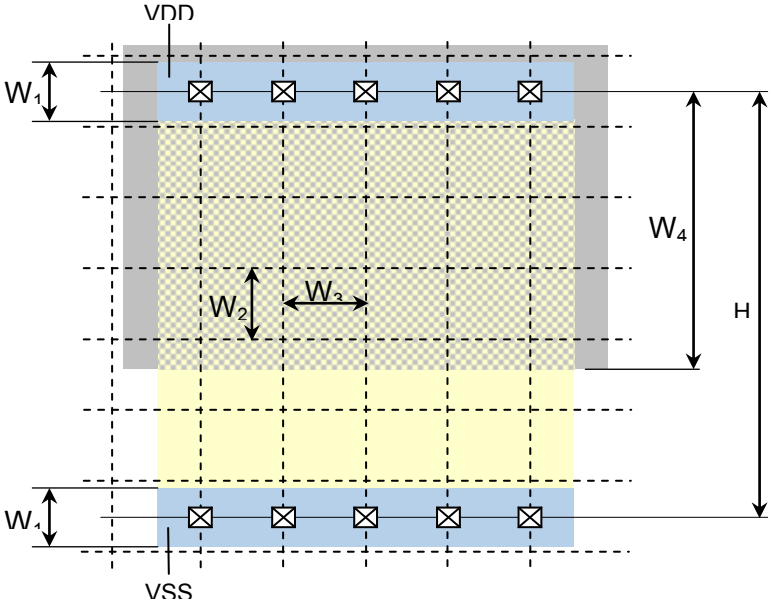


Figure 9.1. Physical structure of single height digital standard cells

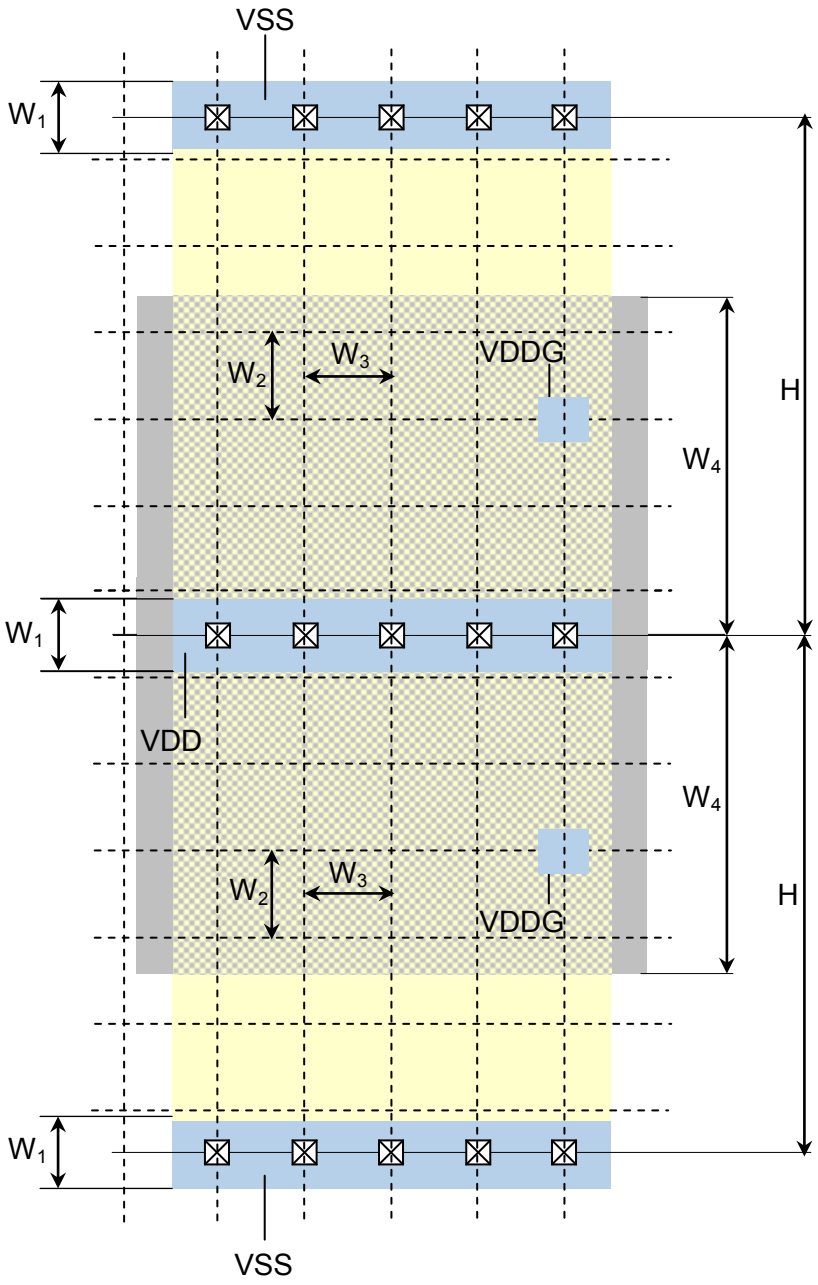


Figure 9.2. Physical structure of double height (low-high-low) digital standard cells (for Always on Cells)

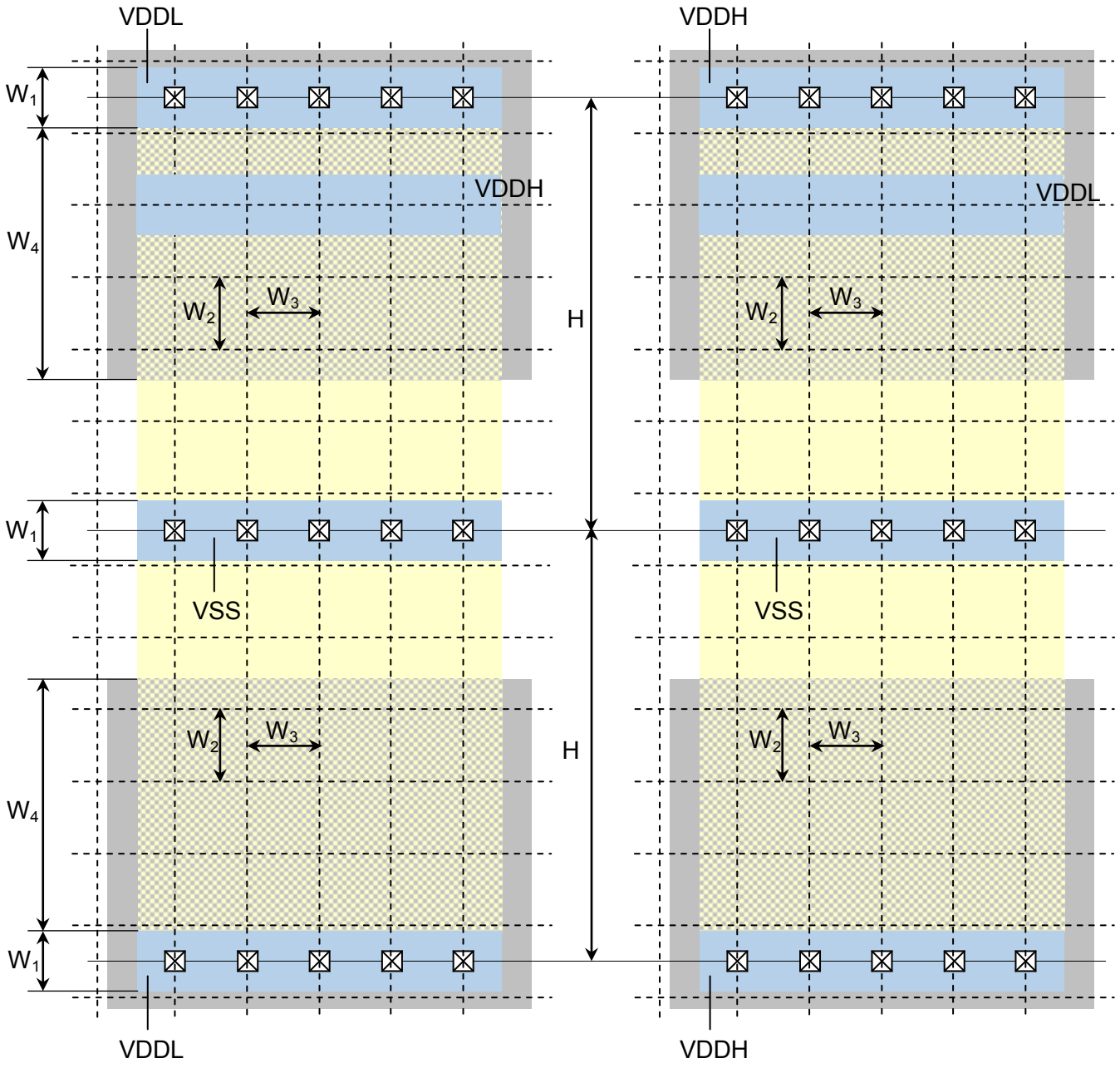


Figure 9.3. Physical structure of Level-shifter cells:
a. High-to-Low, b.Low-to-High

Table 9.1. Physical structure dimensions

Parameter	Symbol	Value
Cell height	H	2.88 um
Power rail width	W_1	0.16 um
Vertical grid	W_2	0.32 um
Horizontal grid	W_3	0.32 um
NWell height	W_4	1.68 um
VDDH to VDDL height (Fig. 8.3)	W_5	0.72 um

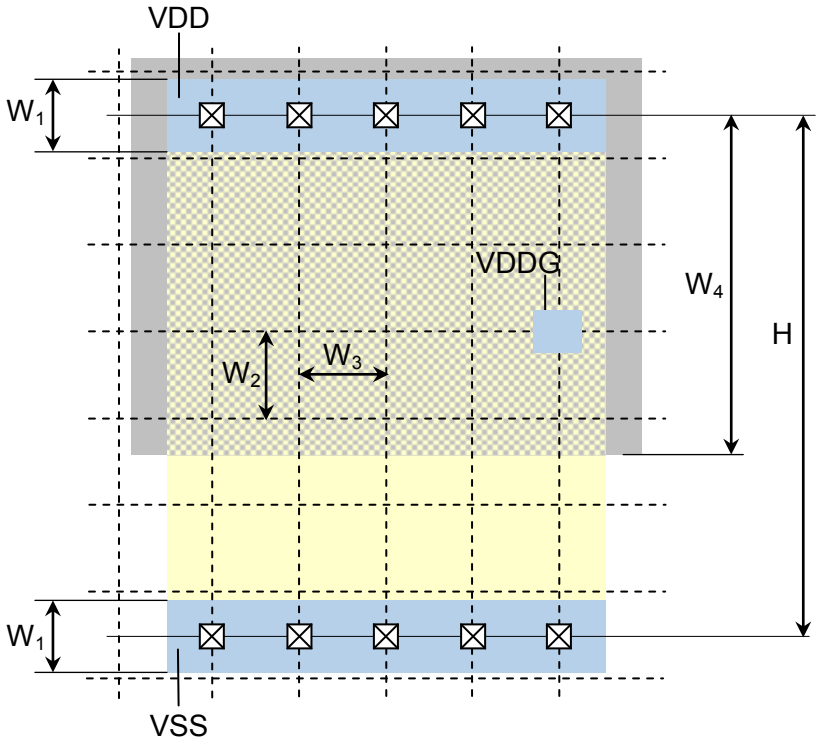


Figure 9.4. Physical structure of single height digital standard cells (for Retention Flip-Flops and scan Flip-Flops)

d_{track} is the minimum center-to-center distance for metal2 layers (with VIA12)

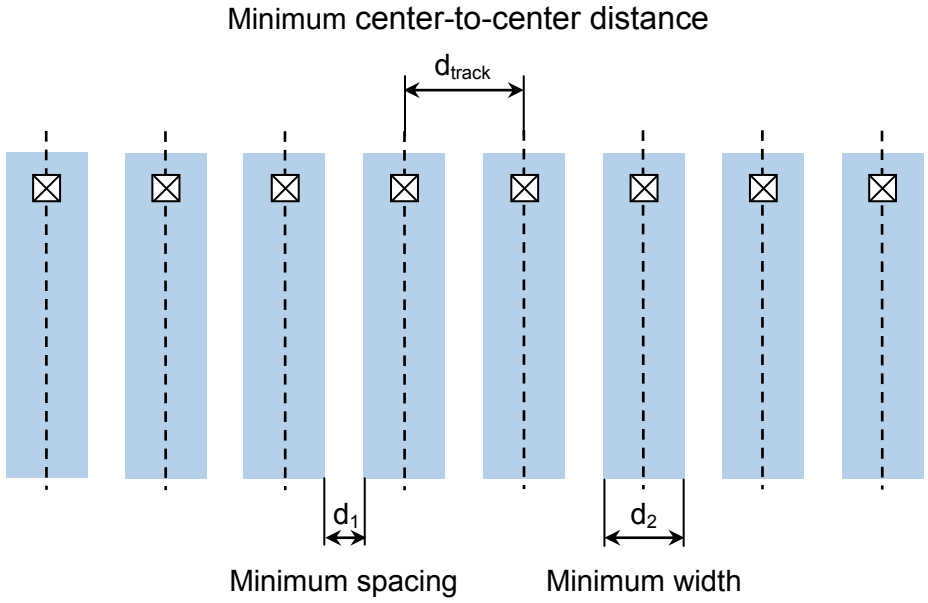


Figure 9.5. Definition of d_{track}

10. Descriptions of Digital Standard Cells

10.1. Inverters

INVX0, INVX1, INVX2, INVX4, INVX8, INVX16, INVX32

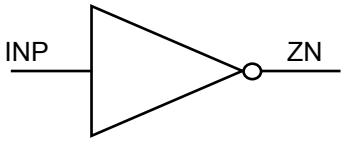


Figure 10.1. Logic Symbol of Inverting Buffer

Table 10.1. Inverter Truth Table

INP	ZN
0	1
1	0

Table 10.2. Inverter Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
INVX0	0.5 x Csl	103	25	10	5.5296
INVX1	1 x Csl	100	52	8	6.4512
INVX2	2 x Csl	100	104	30	6.4512
INVX4	4 x Csl	99	209	27	9.216
INVX8	8 x Csl	98	418	14	14.7456
INVX16	16 x Csl	83	837	81	25.8048
INVX32	32 x Csl	98	1674	157	47.0016

10.2. Inverting Buffers

IBUFFX2, IBUFFX4, IBUFFX8, IBUFFX16, IBUFFX32

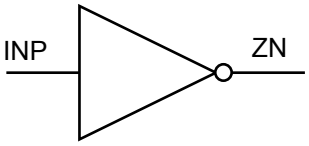


Figure 10.2. Logic Symbol of Inverting Buffer

Table 10.3. Inverting Buffer Truth Table

INP	ZN
0	1
1	0

Table 10.4. Inverting Buffer Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
IBUFFX2	2 x Csl	135	131	618	10.1376
IBUFFX4	4 x Csl	162	235	964	12.9024
IBUFFX8	8 x Csl	189	441	3170	18.4320
IBUFFX16	16 x Csl	226	861	6066	31.3344
IBUFFX32	32 x Csl	310	170	14748	56.2176

10.3. Non-inverting Buffers

NBUFFX2, NBUFFX4, NBUFFX8, NBUFFX16, NBUFFX32

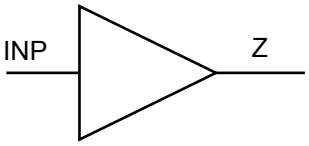


Figure 10.3. Logic Symbol of Non-inverting Buffer

Table 10.5. Non-inverting Buffer Truth Table

INP	Z
0	0
1	1

Table 10.6. Non-inverting Buffer Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		Ps	nW	nW/MHz	(um^2)
NBUFFX2	2 x Csl	188	106	582	5.5296
NBUFFX4	4 x Csl	242	209	1502	10.1376
NBUFFX8	8 x Csl	246	418	2877	14.7456
NBUFFX16	16 x Csl	244	835	5191	26.7264
NBUFFX32	32 x Csl	255	173	9719	55.2960

10.4. Tri-state Non-inverting Buffer w/ High-Active Enable

TNBUFFX1, TNBUFFX2, TNBUFFX4, TNBUFFX8, TNBUFFX16, TNBUFFX32

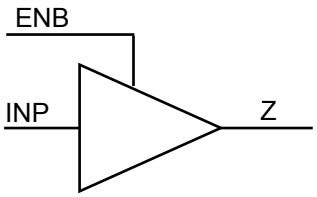


Figure 10.4. Logic Symbol of Tri-state Non-inverting Buffer w/ High-Active Enable

Table 10.7. Tri-state Non-inverting Buffer w/ High-Active Enable Truth Table

ENB	INP	Z
0	0	Z
0	1	Z
1	0	0
1	1	1

Table 10.8. Tri-state Non-inverting Buffer w/ High-Active Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
TNBUFFX1	1 x Csl	208	897	8295	13.8240
TNBUFFX2	2 x Csl	227	135	12846	15.6672
TNBUFFX4	4 x Csl	240	244	30411	18.432
TNBUFFX8	8 x Csl	293	455	48947	23.9616
TNBUFFX16	16 x Csl	288	888	94350	37.7856
TNBUFFX32	32 x Csl	288	175	181834	68.1984

10.5. AND

AND2X1, AND2X2, AND2X4, AND3X1, AND3X2, AND3X4, AND4X1, AND4X2, AND4X4

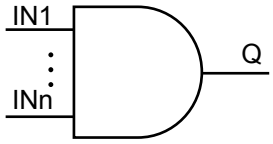


Figure 10.5. Logic Symbol of AND

Table 10.9. AND Truth Table (n=2,3,4)

IN1	IN2	. . .	INn	Q
0	X	. . .	X	0
X	0	. . .	X	0
. . .	. . .	. . .	. . .	0
X	X	. . .	0	0
1	1	1	1	1

Table 10.10. AND Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AND2X1	1 x Csl	180	56	6545	7.3728
AND2X2	2 x Csl	214	108	13906	8.2944
AND2X4	4 x Csl	277	210	40254	11.0592
AND3X1	1 x Csl	206	59	8222	8.2944
AND3X2	2 x Csl	247	109	17706	10.1376
AND3X4	4 x Csl	319	211	50401	12.9024
AND4X1	1 x Csl	214	63	8557	10.1376
AND4X2	2 x Csl	244	115	19124	11.9808
AND4X4	4 x Csl	323	220	52530	14.7456

10.6. NAND

NAND2X0, NAND2X1, NAND2X2, NAND2X4, NAND3X0, NAND3X1, NAND3X2, NAND3X4, NAND4X0, NAND4X1

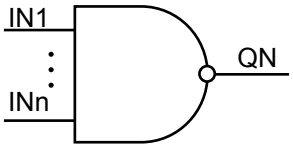


Figure 10.6. Logic Symbol of NAND

Table 10.11. NAND Truth Table (n=2,3,4)

IN1	IN2	. . .	INn	QN
0	X	. . .	X	1
X	0	. . .	X	1
. . .	. . .	. . .	. . .	1
X	X	. . .	0	1
1	1	1	1	0

Table 10.12. NAND Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
NAND2X0	0.5 x Csl	140	38	3583	5.5296
NAND2X1	1 x Csl	132	78	5208	5.5296
NAND2X2	2 x Csl	126	157	9191	9.2160
NAND2X4	4 x Csl	125	314	17902	14.7456
NAND3X0	0.5 x Csl	128	91	5331	7.3728
NAND3X1	1 x Csl	192	102	12200	11.9808
NAND3X2	2 x Csl	212	155	19526	12.9024
NAND3X4	4 x Csl	241	260	44937	15.6672
NAND4X0	0.5 x Csl	147	106	5357	8.2944
NAND4X1	1 x Csl	178	161	15214	12.9024

10.7. OR

OR2X1, OR2X2, OR2X4, OR3X1, OR3X2, OR3X4, OR4X1, OR4X2, OR4X4

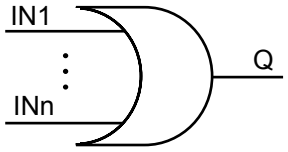


Figure 10.7. Logic Symbol of OR

Table 10.13. OR Truth Table (n=2,3,4)

IN1	IN2	. . .	INn	Q
0	0	. . .	0	0
1	X	. . .	X	1
. . .	. . .	. . .	. . .	1
X	1	. . .	X	1
X	X	X	1	1

Table 10.14. OR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OR2X1	1 x Csl	171	58	6859	7.3728
OR2X2	2 x Csl	204	110	12934	9.2160
OR2X4	4 x Csl	251	216	34515	11.9808
OR3X1	1 x Csl	184	62	7396	9.2160
OR3X2	2 x Csl	210	115	14574	11.0592
OR3X4	4 x Csl	271	227	40937	13.824
OR4X1	1 x Csl	199	64	7698	10.1376
OR4X2	2 x Csl	231	119	16238	11.9808
OR4X4	4 x Csl	319	227	49239	14.7456

10.8. NOR

NOR2X0, NOR2X1, NOR2X2, NOR2X4, NOR3X0, NOR3X1, NOR3X2, NOR3X4, NOR4X0, NOR4X1

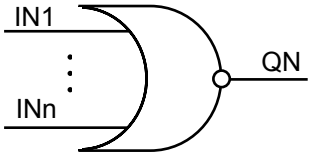


Figure 10.8. Logic Symbol of NOR

Table 10.15. NOR Truth Table (n=2,3,4)

IN1	IN2	. . .	INn	QN
0	0	. . .	0	1
1	X	. . .	X	0
. . .	. . .	. . .	. . .	0
X	1	. . .	X	0
X	X	X	1	0

Table 10.16. NOR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
NOR2X0	0.5 x Csl	114	35	4211	5.5296
NOR2X1	1 x Csl	132	49	619	6.4512
NOR2X2	2 x Csl	129	98	11085	9.2160
NOR2X4	4 x Csl	132	197	2952	14.7456
NOR3X0	0.5 x Csl	118	48	6553	8.2944
NOR3X1	1 x Csl	153	104	16521	11.9808
NOR3X2	2 x Csl	167	157	23975	13.8240
NOR3X4	4 x Csl	200	263	37654	16.5888
NOR4X0	0.5 x Csl	158	48	368	9.2160
NOR4X1	1 x Csl	126	119	14991	15.6672

10.9. XOR

XOR2X1, XOR2X2, XOR3X1, XOR3X2

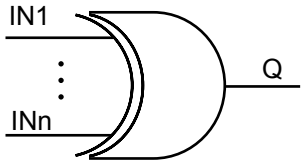


Figure 10.9. Logic Symbol of XOR

Table 10.17. XOR Truth Table (n=2,3)

IN1	IN2	. . .	INn	Q
0	0	. . .	0	0
Odd number of 1's				1
Even number of 1's				0

Table 10.18. XOR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
XOR2X1	1 x Csl	237	89	8702	13.8240
XOR2X2	2 x Csl	251	141	17434	15.6672
XOR3X1	1 x Csl	265	168	21596	22.1184
XOR3X2	2 x Csl	288	224	34276	23.9616

10.10. XNOR

XNOR2X1, XNOR2X2, XNOR3X1, XNOR3X2

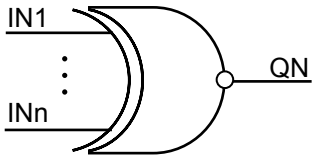


Figure 10.10. Logic Symbol of XNOR

Table 10.19. XNOR Truth Table (n=2,3)

IN1	IN2	. . .	INn	QN
0	0	. . .	0	1
Odd number of 1's				0
Even number of 1's				1

Table 10.20. XNOR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
XNOR2X1	1 x Csl	136	82	16372	13.8240
XNOR2X2	2 x Csl	151	129	24745	15.6672
XNOR3X1	1 x Csl	229	184	27135	22.1184
XNOR3X2	2 x Csl	252	238	37944	23.9616

10.11. AND-OR

AO21X1, AO21X2
Q=(1&2)|3

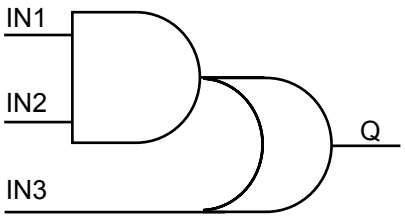


Figure 10.11. Logic Symbol of AND-OR 2/1

Table 10.21. AND-OR 2/1 Truth Table

IN1	IN2	IN3	Q
1	1	X	1
X	X	1	1
0	X	0	0
X	0	0	0

Table 10.22. AND-OR 2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AO21X1	1 x Csl	235	59	9703	10.1376
AO21X2	2 x Csl	267	110	21095	11.9808

AO22X1, AO22X2
Q=(1&2)|(3&4)

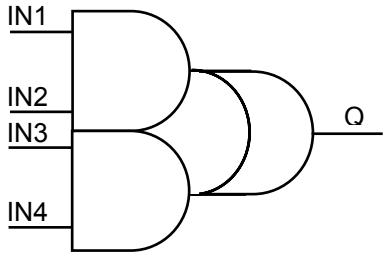


Figure 10.12. Logic Symbol of AND-OR 2/2

Table 10.23. AND-OR 2/2 Truth Table

IN1	IN2	IN3	IN4	Q
X	X	1	1	1
1	1	X	X	1
0	X	0	X	0
X	0	0	X	0
0	X	X	0	0
X	0	X	0	0

Table 10.24. AND-OR 2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AO22X1	1 x Csl	238	63	10662	11.9808
AO22X2	2 x Csl	273	114	20865	12.9024

AO221X1, AO221X2
Q=(1&2)|(3&4)|5

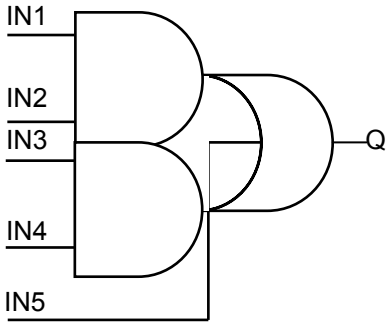


Figure 10.13. Logic Symbol of AND-OR 2/2/1

Table 10.25. AND-OR 2/2/1 Truth Table

IN1	IN2	IN3	IN4	IN5	Q
1	1	X	X	X	1
X	X	1	1	X	1
X	X	X	X	1	1
0	X	0	X	0	0
X	0	0	X	0	0
0	X	X	0	0	0
X	0	X	0	0	0

Table 10.26. AND-OR 2/2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AO221X1	1 x Csl	289	65	13298	12.9024
AO221X2	2 x Csl	314	116	24527	14.7456

AO222X1, AO222X2
Q=(1&2)|(3&4)|(5&6)

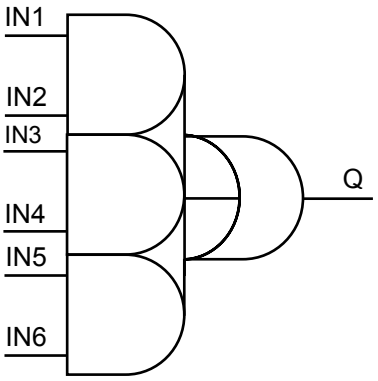


Figure 10.14. Logic Symbol of AND-OR 2/2/2

Table 10.27. AND-OR 2/2/2 Truth Table

IN1	IN2	IN3	IN4	IN5	IN6	Q
1	1	X	X	X	X	1
X	X	1	1	X	X	1
X	X	X	X	1	1	1
0	X	0	X	0	X	0
0	X	0	X	X	0	0
0	X	X	0	0	X	0
0	X	X	0	X	0	0
X	0	0	X	0	X	0
X	0	0	X	X	0	0
X	0	X	0	0	X	0
X	0	X	0	X	0	0

Table 10.28. AND-OR 2/2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AO222X1	1 x Csl	294	69	14175	14.7456
AO222X2	2 x Csl	320	120	25846	15.6672

10.12. AND-OR-Invert

AOI21X1, AOI21X2
QN=!((1&2)|3)

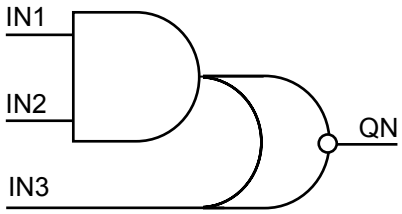


Figure 10.15. Logic Symbol of AND-OR-Invert 2/1

Table 10.29. AND-OR-Invert 2/1 Truth Table

IN1	IN2	IN3	QN
1	1	X	0
X	X	1	0
0	X	0	1
X	0	0	1

Table 10.30. AND-OR-Invert 2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOI21X1	1 x Csl	181	86	13912	11.9808
AOI21X2	2 x Csl	196	137	16301	12.9024

AOI22X1, AOI22X2

QN=!((1&2)|(3&4))

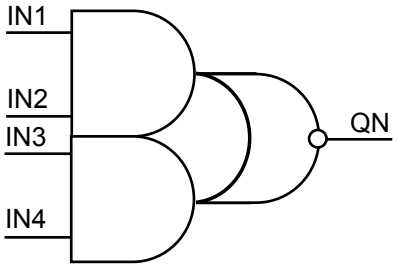


Figure 10.16. Logic Symbol of AND-OR-Invert 2/2

Table 10.31. AND-OR-Invert 2/2 Truth Table

IN1	IN2	IN3	IN4	QN
X	X	1	1	0
1	1	X	X	0
0	X	0	X	1
X	0	0	X	1
0	X	X	0	1
X	0	X	0	1

Table 10.32. AND-OR-Invert 2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOI22X1	1 x Csl	204	89	13290	12.9024
AOI22X2	2 x Csl	235	141	20026	14.7456

AOI221X1, AOI221X2
QN=!((1&2)|(3&4)|5)

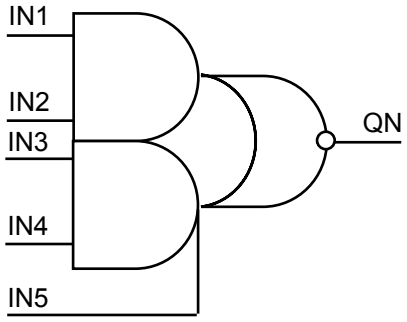


Figure 10.17. Logic Symbol of AND-OR-Invert 2/2/1

Table 10.33. AND-OR-Invert 2/2/1 Truth Table

IN1	IN2	IN3	IN4	IN5	QN
1	1	X	X	X	0
X	X	1	1	X	0
X	X	X	X	1	0
0	X	0	X	0	1
X	0	0	X	0	1
0	X	X	0	0	1
X	0	X	0	0	1

Table 10.34. AND-OR-Invert 2/2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOI221X1	1 x Csl	207	102	14356	14.7456
AOI221X2	2 x Csl	223	154	19564	15.6672

AOI222X1, AOI222X2
QN=!((1&2)|(3&4)|(5&6))

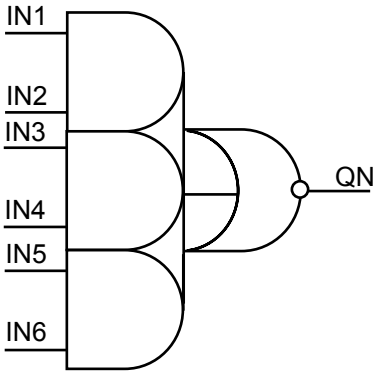


Figure 10.18. Logic Symbol of AND-OR-Invert 2/2/2

Table 10.35. AND-OR-Invert 2/2/2 Truth Table

IN1	IN2	IN3	IN4	IN5	IN6	Q
1	1	X	X	X	X	1
X	X	1	1	X	X	1
X	X	X	X	1	1	1
0	X	0	X	0	X	0
0	X	0	X	X	0	0
0	X	X	0	0	X	0
0	X	X	0	X	0	0
X	0	0	X	0	X	0
X	0	0	X	X	0	0
X	0	X	0	0	X	0
X	0	X	0	X	0	0

Table 10.36. AND-OR-Invert 2/2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOI222X1	1 x Csl	221	109	13982	15.6672
AOI222X2	2 x Csl	245	161	20441	17.5104

10.13. OR-AND

OA21X1, OA21X2
Q=(1|2)&3

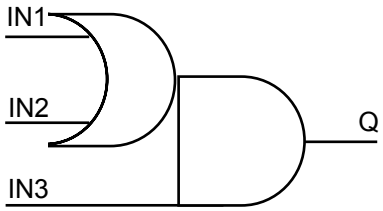


Figure 10.19. Logic Symbol of OR-AND 2/1

Table 10.37. OR-AND 2/1 Truth Table

IN1	IN2	IN3	Q
0	0	X	0
X	X	0	0
1	X	1	1
X	1	1	1

Table 10.38. OR-AND 2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OA21X1	1 x Csl	252	58	8580	9.2160
OA21X2	2 x Csl	231	111	17418	11.0592

OA22X1, OA22X2

Q=(1|2)&(3|4)

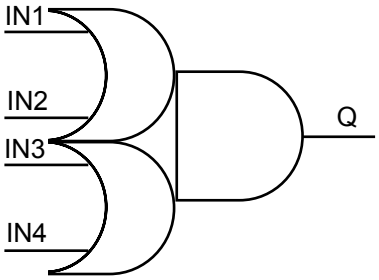


Figure 10.20. Logic Symbol of OR-AND 2/2

Table 10.39. OR-AND 2/2 Truth Table

IN1	IN2	IN3	IN4	Q
0	0	X	X	0
X	X	0	0	0
1	X	1	X	1
X	1	1	X	1
1	X	X	1	1
X	1	X	1	1

Table 10.40. OR-AND 2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OA22X1	1 x Csl	212	63	8038	11.0592
OA22X2	2 x Csl	240	114	17542	12.9024

OA221X1, OA221X2
Q=(1|2)&(3|4)&5

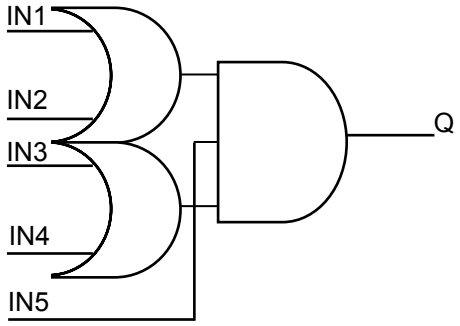


Figure 10.21. Logic Symbol of OR-AND 2/2/1

Table 10.41. OR-AND 2/2/1 Truth Table

IN1	IN2	IN3	IN4	IN5	Q
0	0	X	X	X	0
X	X	0	0	X	0
X	X	X	X	0	0
1	X	1	X	1	1
X	1	1	X	1	1
1	X	X	1	1	1
X	1	X	1	1	1

Table 10.42. OR-AND 2/2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OA221X1	1 x Csl	208	71	9239	12.9024
OA221X2	2 x Csl	236	118	20697	14.7456

OA222X1, OA222X2
Q=(1|2)&(3|4)&(5|6)

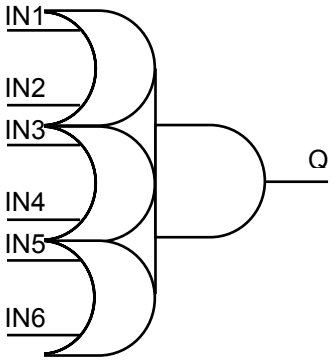


Figure 10.22. Logic Symbol of OR-AND 2/2/2

Table 10.43. OR-AND 2/2/2 Truth Table

IN1	IN2	IN3	IN4	IN5	IN6	Q
0	0	X	X	X	X	0
X	X	0	0	X	X	0
X	X	X	X	0	0	0
1	X	1	X	1	X	1
1	X	1	X	X	1	1
1	X	X	1	1	X	1
1	X	X	1	X	1	1
X	1	1	X	1	X	1
X	1	1	X	X	1	1
X	1	X	1	1	X	1
X	1	X	1	X	1	1

Table 10.44. OR-AND 2/2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OA222X1	1 x Csl	200	75	10254	14.7456
OA222X2	2 x Csl	233	120	22829	15.6672

10.14. OR-AND-Invert

OAI21X1, OAI21X2
QN=!((1|2)&3)

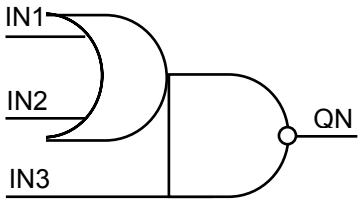


Figure 10.23. Logic Symbol of OR-AND-INVERT 2/1

Table 10.45. OR-AND-INVERT 2/1 Truth Table

IN1	IN2	IN3	QN
0	0	X	1
X	X	0	1
1	X	1	0
X	1	1	0

Table 10.46. OR-AND-INVERT 2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OAI21X1	1 x Csl	159	88	10270	11.0592
OAI21X2	2 x Csl	172	139	15081	11.9808

OAI22X1, OAI22X2
QN=!((1|2)&(3|4))

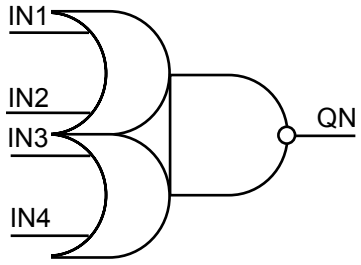


Figure 10.24. Logic Symbol of OR-AND-INVERT 2/2

Table 10.47. OR-AND-INVERT 2/2 Truth Table

IN1	IN2	IN3	IN4	QN
0	0	X	X	1
X	X	0	0	1
1	X	1	X	0
X	1	1	X	0
1	X	X	1	0
X	1	X	1	0

Table 10.48. OR-AND-INVERT 2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OAI22X1	1 x Csl	174	98	10666	12.9024
OAI22X2	2 x Csl	184	150	16509	13.8240

OAI221X1, OAI221X2
QN=!((1|2)&(3|4)&5)

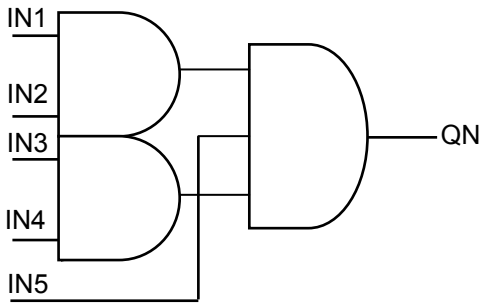


Figure 10.25. Logic Symbol of OR-AND-INVERT 2/2/1

Table 10.49. OR-AND-INVERT 2/2/1 Truth Table

IN1	IN2	IN3	IN4	IN5	QN
0	0	X	X	X	1
X	X	0	0	X	1
X	X	X	X	0	1
1	X	1	X	1	0
X	1	1	X	1	0
1	X	X	1	1	0
X	1	X	1	1	0

Table 10.50. OR-AND-INVERT 2/2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OAI221X1	1 x Csl	219	101	11136	14.7456
OAI221X2	2 x Csl	239	153	18112	15.6672

OAI222X1, OAI222X2
QN=!((1|2)&(3|4)&(5|6))

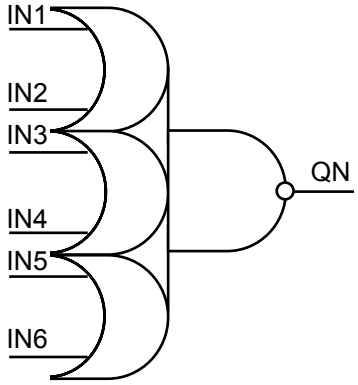


Figure 10.26. Logic Symbol of OR-AND-INVERT 2/2/2

Table 10.51. OR-AND-INVERT 2/2/2 Truth Table

IN1	IN2	IN3	IN4	IN5	IN6	QN
0	0	X	X	X	X	1
X	X	0	0	X	X	1
X	X	X	X	0	0	1
1	X	1	X	1	X	0
1	X	1	X	X	1	0
1	X	X	1	1	X	0
1	X	X	1	X	1	0
X	1	1	X	1	X	0
X	1	1	X	X	1	0
X	1	X	1	1	X	0
X	1	X	1	X	1	0

Table 10.52. OR-AND-INVERT 2/2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OAI222X1	1 x Csl	272	94	11458	15.6672
OAI222X2	2 x Csl	294	144	19106	17.5104

10.15. Multiplexer 2 to 1

MUX21X1, MUX21X2

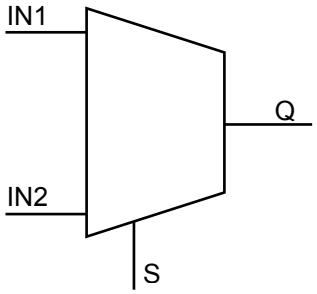


Figure 10.27. Logic Symbol of Multiplexer 2 to 1

Table 10.53. Multiplexer 2 to 1 Truth Table

S	Q
0	IN1
1	IN2

Table 10.54. Multiplexer 2 to 1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
MUX21X1	1 x Csl	223	84	8639	11.0592
MUX21X2	2 x Csl	253	135	17646	12.9024

10.16. Multiplexer 4 to 1

MUX41X1, MUX41X2

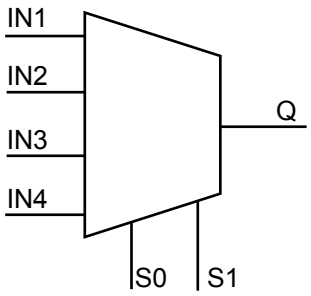


Figure 10.28. Logic Symbol of Multiplexer 4 to 1

Table 10.55. Multiplexer 4 to 1 Truth Table

S1	S0	Q
0	0	IN1
0	1	IN2
1	0	IN3
1	1	IN4

Table 10.56. Multiplexer 4 to 1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
MUX41X1	1 x Csl	250	163	15169	23.0400
MUX41X2	2 x Csl	277	221	27607	24.8832

10.17. Decoder 2 to 4

DEC24X1, DEC24X2

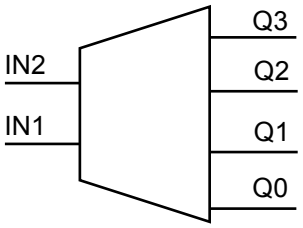


Figure 10.29. Logic Symbol of Decoder 2 to 4

Table 10.57. Decoder 2 to 4 Truth Table

IN2	IN1	Q0	Q1	Q2	Q3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table 10.58. Decoder 2 to 4 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DEC24X1	1 x Csl	Q0	191	23	543	29.4912
		Q1	189			
		Q2	132			
		Q3	127			
DEC24X1	2 x Csl	Q0	162	410	810	36.8640
		Q1	163			
		Q2	161			
		Q3	229			

10.18. Half Adder 1-Bit

HADDX1, HADDX2

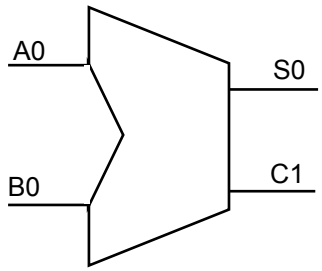


Figure 10.30. Logic Symbol of Half Adder 1-Bit

Table 10.59. Half Adder 1-Bit Truth Table

A0	B0	S0 (sum)	C1 (carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 10.60. Half Adder 1-Bit Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (S0, C1)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
HADDX1	1 x Csl	S0	228	114	8475	15.6672
		C1	160		618	
HADDX2	2 x Csl	S0	251	217	16856	18.4320
		C1	188		796	

10.19. Full Adder 1-Bit

FADDX1, FADDX2

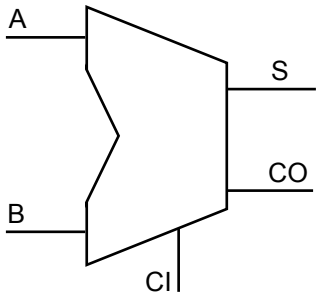


Figure 10.31. Logic Symbol of Full Adder 1-Bit

Table 10.61. Full Adder 1-Bit Truth Table

A	B	CI	S (sum)	CO (carry)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 10.62. Full Adder 1-Bit Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (S, CO)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
FADDX1	1 x Csl	S	205	159	5374	29.4912
		CO	226		713	
FADDX2	2 x Csl	S	226	221	14806	31.3344
		CO	245		835	

10.20. Pos Edge DFF

DFFX1, DFFX2

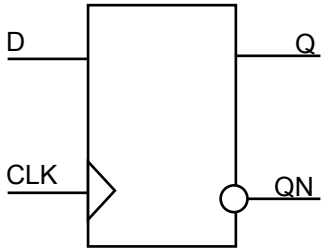


Figure 10.32. Logic Symbol of Pos Edge DFF

Table 10.63. Pos Edge DFF Transition Table

D	CLK	Q	QN
X	Inactive	No change	No change
1	Rise	1	0
0	Rise	0	1

Table 10.64. Pos Edge DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFX1	1 x Csl	Q	217	140	284	24.8832
		QN	193			
DFFX2	2 x Csl	Q	251	206	520	31.3344
		QN	198			

10.21. Pos Edge DFF w/Async Low-Active Set

DFFASX1, DFFASX2

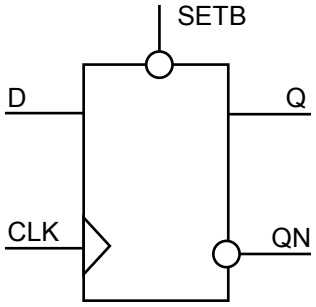


Figure 10.33. Logic Symbol of Pos Edge DFF w/Async Low-Active Set

Table 10.65. Pos Edge DFF w/Async Low-Active Set Transition Table

D	SETB	CLK	Q	QN
X	0	X	1	0
X	1	Inactive	No change	No change
1	1	Rise	1	0
0	1	Rise	0	1

Table 10.66. Pos Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFASX1	1 x Csl	Q	412	152	161	31.3344
		QN	372			
DFFASX2	2 x Csl	Q	470	213	355	34.0992
		QN	411			

10.22. Pos Edge DFF w/Async Low-Active Reset

DFFARX1, DFFARX2

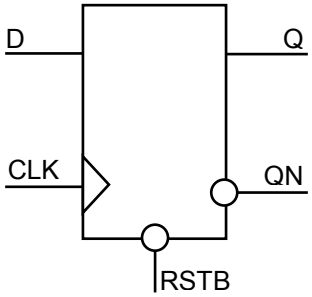


Figure 10.34. Logic Symbol of Pos Edge DFF w/Async Low-Active Reset

Table 10.67. Pos Edge DFF w/Async Low-Active Reset Transition Table

D	RSTB	CLK	Q	QN
X	0	X	0	1
X	1	Inactive	No change	No change
1	1	Rise	1	0
0	1	Rise	0	1

Table 10.68. Pos Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFARX1	1 x Csl	Q	167	164	281	32.2560
		QN	326			
DFFARX2	2 x Csl	Q	213	221	531	34.0992
		QN	345			

10.23. Pos Edge DFF w/Async Low-Active Set & Reset

DFFASRX1, DFFASRX2

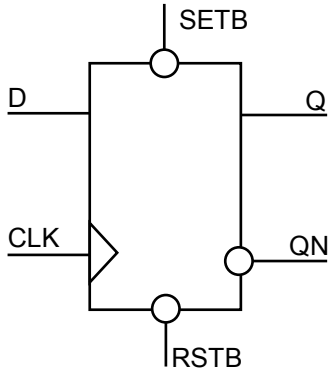


Figure 10.35. Logic Symbol of Pos Edge DFF w/Async Low-Active Set & Reset

Table 10.69. Pos Edge DFF w/Async Low-Active Set & Reset Transition Table

D	SETB	RSTB	CLK	Q	QN	Notes
X	0	0	X	X	X	Not Allowed
X	0	1	X	1	0	
X	1	0	X	0	1	
X	1	1	Inactive	No change	No change	
1	1	1	Rise	1	0	
0	1	1	Rise	0	1	

Table 10.70. Pos Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz+, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFASRX1	1 x Csl	Q	212	167	215	35.0208
		QN	365			
DFFASRX2	2 x Csl	Q	244	271	478	36.8640
		QN	388			

10.24. Pos Edge DFF w/ Sync Low-Active Set & Reset

DFFSSRX1, DFFSSRX2

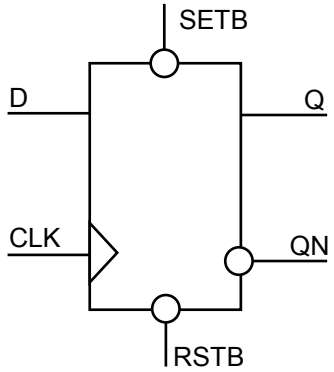


Figure 10.36. Logic Symbol of Pos Edge DFF w/ Sync Low-Active Set & Reset

Table 10.71. Pos Edge DFF w/ Sync Low-Active Set & Reset Transition Table

D	SETB	RSTB	CLK	Q	QN	Notes
X	X	X	Inactive	No change	No change	
0	1	1	Rise	0	1	
1	1	1	Rise	1	0	
X	0	1	Rise	1	0	
X	1	0	Rise	0	1	
X	0	0	Rise	X	X	Not Allowed

Table 10.72. Pos Edge DFF w/ Sync Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFSSRX1	1 x Csl	Q	206	977	460	33.1776
		QN	192			
DFFSSRX2	2 x Csl	Q	254	998	501	37.7856
		QN	205			

10.25. Neg Edge DFF

DFFNX1, DFFNX2

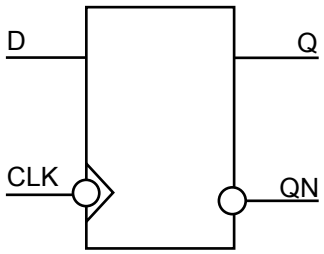


Figure 10.37. Logic Symbol of Neg Edge DFF

Table 10.73. Neg Edge DFF Transition Table

D	CLK	Q	QN
X	Inactive	No change	No change
1	Fall	1	0
0	Fall	0	1

Table 10.74. Neg Edge DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNX1	1 x Csl	Q	395	140	226	28.5696
		QN	365			
DFFNX2	2 x Csl	Q	441	218	537	31.3344
		QN	399			

10.26. Neg Edge DFF w/Async Low-Active Set

DFFNASX1, DFFNASX2

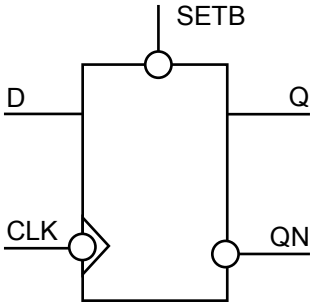


Figure 10.38. Logic Symbol of Neg Edge DFF w/Async Low-Active Set

Table 10.75. Neg Edge DFF w/Async Low-Active Set Transition Table

D	SETB	CLK	Q	QN
X	0	X	1	0
X	1	Inactive	No change	No change
1	1	Fall	1	0
0	1	Fall	0	1

Table 10.76. Neg Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNASX1	1 x Csl	Q	329	129	94	30.4128
		QN	298			
DFFNASX2	2 x Csl	Q	401	191	384	34.0992
		QN	343			

10.27. Neg Edge DFF w/Async Low-Active Reset

DFFNARX1, DFFNARX2

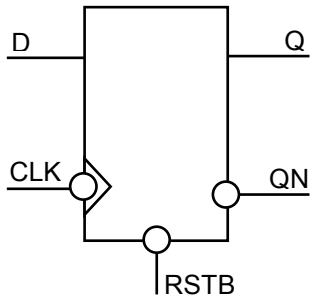


Figure 10.39. Logic Symbol of Neg Edge DFF w/Async Low-Active Reset

Table 10.77. Neg Edge DFF w/Async Low-Active Reset Transition Table

D	RSTB	CLK	Q	QN
X	0	X	0	1
X	1	Inactive	No change	No change
1	1	Fall	1	0
0	1	Fall	0	1

Table 10.78. Neg Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNARX1	1 x Csl	Q	208	149	247	32.2560
		QN	347			
DFFNARX2	2 x Csl	Q	273	206	582	34.0992
		QN	359			

10.28. Neg Edge DFF w/Async Low-Active Set & Reset

DFFNASRX1, DFFNASRX2

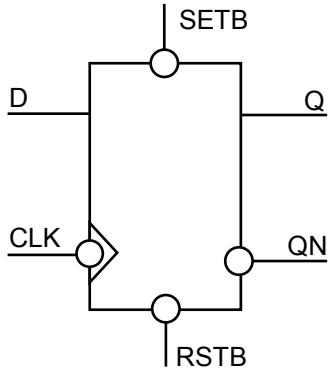


Figure 10.40. Logic Symbol of Neg Edge DFF w/Async Low-Active Set & Reset

Table 10.79. Neg Edge DFF w/Async Low-Active Set & Reset Transition Table

D	SETB	RSTB	CLK	Q	QN	Notes
X	0	0	X	X	X	Not Allowed
X	0	1	X	1	0	
X	1	0	X	0	1	
X	1	1	Inactive	No change	No change	
1	1	1	Fall	1	0	
0	1	1	Fall	0	1	

Table 10.80. Neg Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNASRX1	1 x Csl	Q	177	167	89	35.0208
		QN	365			
DFFNASRX2	2 x Csl	Q	240	270	455	36.8640
		QN	390			

10.29. Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out

DFFNASRQX1, DFFNASRQX2

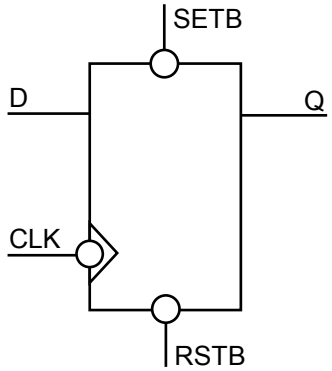


Figure 10.41. Logic Symbol of Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out

Table 10.81. Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out Transition Table

D	SETB	RSTB	CLK	Q	Notes
X	0	0	X	X	Not Allowed
X	0	1	X	1	
X	1	0	X	0	
X	1	1	Inactive	No change	
0	1	1	Fall	0	
1	1	1	Fall	1	

Table 10.82. Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNASRQX1	1 x Csl	Q	168	149	15486	32.2560
DFFNASRQX2	2 x Csl	Q	226	195	23040	34.0992

10.30. Neg Edge DFF w/Async Low-Active Set & Reset, Only QN out

DFFNASRNX1, DFFNASRNX2

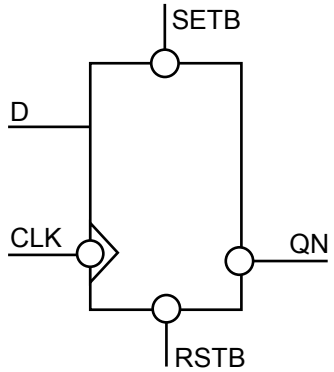


Figure 10.42. Logic Symbol of Neg Edge DFF w/Async Low-Active Set & Reset, Only QN out

Table 10.83. Neg Edge DFF w/Async Low-Active Set & Reset, Only QN out Transition Table

D	SETB	RSTB	CLK	QN	Notes
X	0	0	X	X	Not Allowed
X	0	1	X	0	
X	1	0	X	1	
X	1	1	Inactive	No change	
0	1	1	Fall	1	
1	1	1	Fall	0	

Table 10.84. Neg Edge DFF w/Async Low-Active Set & Reset, Only QN out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNASRNX1	1 x Csl	QN	361	161	20082	32.2560
DFFNASRNX2	2 x Csl	QN	390	222	36153	34.0992

10.31. Scan Pos Edge DFF

SDFFX1, SDFFX2

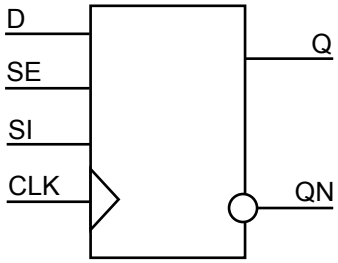


Figure 10.43. Logic Symbol of Scan Pos Edge DFF

Table 10.85. Scan Pos Edge DFF Transition Table

D	SI	SE	CLK	Q	QN
X	X	X	Inactive	No change	No change
1	X	0	Rise	1	0
0	X	0	Rise	0	1
X	1	1	Rise	1	0
X	0	1	Rise	0	1

Table 10.86. Scan Pos Edge DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFX1	1 x Csl	Q	207	159	340	30.4128
		QN	185			
SDFFX2	2 x Csl	Q	249	520972	152711	33.1776
		QN	199			

10.32. Scan Pos Edge DFF w/Async Low-Active Set

SDFFASX1, SDFFASX2

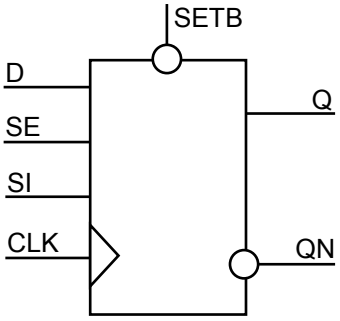


Figure 10.44. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set

Table 10.87. Scan Pos Edge DFF w/Async Low-Active Set Transition Table

D	SI	SE	SETB	CLK	Q	QN
X	X	X	0	X	1	0
X	X	X	1	Inactive	No change	No change
1	X	0	1	Rise	1	0
0	X	0	1	Rise	0	1
X	1	1	1	Rise	1	0
X	0	1	1	Rise	0	1

Table 10.88. Scan Pos Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFASX1	1 x Csl	Q	420	159	149	36.8640
		QN	379			
SDFFASX2	2 x Csl	Q	476	220	364	39.6288
		QN	414			

10.33. Scan Pos Edge DFF w/Async Low-Active Reset

SDFFARX1, SDFFARX2

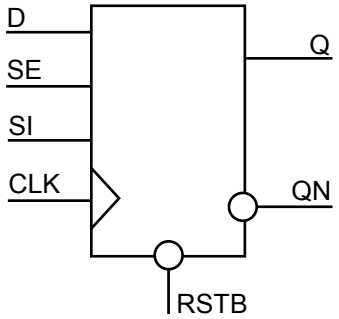


Figure 10.45. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Reset

Table 10.89. Scan Pos Edge DFF w/Async Low-Active Reset Transition Table

D	SI	SE	RSTB	CLK	Q	QN
X	X	X	0	X	0	1
X	X	X	1	Inactive	No change	No change
1	X	0	1	Rise	1	0
0	X	0	1	Rise	0	1
X	1	1	1	Rise	1	0
X	0	1	1	Rise	0	1

Table 10.90. Scan Pos Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFARX1	1 x Csl	Q	166	192	300	37.7856
		QN	326			
SDFFARX2	2 x Csl	Q	210	249	543	39.6288
		QN	343			

10.34. Scan Pos Edge DFF w/Async Low-Active Set & Reset

SDFFASRX1, SDFFASRX2

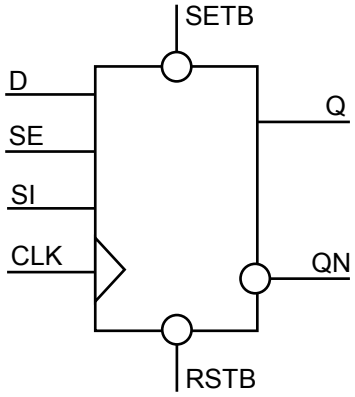


Figure 10.46. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set & Reset

Table 10.91. Scan Pos Edge DFF w/Async Low-Active Set & Reset Transition Table

D	SI	SE	SETB	RSTB	CLK	Q	QN
X	X	X	0	0	X	X	X
X	X	X	0	1	X	1	0
X	X	X	1	0	X	0	1
X	X	X	1	1	Inactive	No change	No change
1	X	0	1	1	Rise	1	0
0	X	0	1	1	Rise	0	1
X	1	1	1	1	Rise	X	1
X	0	1	1	1	Rise	X	0

Table 10.92. Scan Pos Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFASRX1	1 x Csl	Q	202	193	202	40.5504
		QN	362			
SDFFASRX2	2 x Csl	Q	231	297	451	42.3936
		QN	387			

10.35. Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs

SDFFASRSX1, SDFFASRSX2

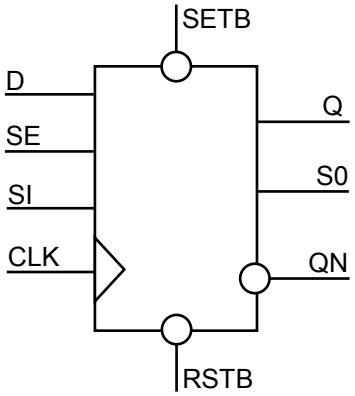


Figure 10.47. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs

Table 10.93. Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs Transition Table

D	SI	SE	SETB	RSTB	CLK	Q	QN	S0	Notes
X	X	X	0	0	X	X	X	X	Not Allowed
X	X	X	0	1	X	1	0	1	
X	X	X	1	0	X	0	1	0	
X	X	X	1	1	Inactive	No change	No change	No change	
1	X	0	1	1	Rise	1	0	1	
0	X	0	1	1	Rise	0	1	0	
X	1	1	1	1	Rise	1	0	1	
X	0	1	1	1	Rise	0	1	0	

Table 10.94. Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN, S0)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFASRSX1	1 x Csl	Q	241	246	1445	42.3936
		QN	363			
		S0	240			
SDFFASRSX2	2 x Csl	Q	289	402	1275	45.1584
		QN	386			
		S0				

10.36. Scan Pos Edge DFF w/ Sync Low-Active Set & Reset

SDFFSSRX1, SDFFSSRX2

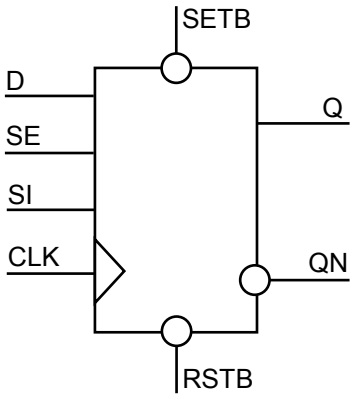


Figure 10.48. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set & Reset

Table 10.95. Scan Pos Edge DFF w/ Sync Low-Active Set & Reset Transition Table

D	SI	SE	SETB	RSTB	CLK	Q	QN
X	X	0	0	0	Rise	X	X
X	X	0	0	1	Rise	1	0
X	X	0	1	0	Rise	0	1
X	X	X	X	X	Inactive	No change	No change
1	X	0	1	1	Rise	1	0
0	X	0	1	1	Rise	0	1
X	1	1	1	1	Rise	1	0
X	0	1	1	1	Rise	0	1

Table 10.96. Scan Pos Edge DFF w/ Sync Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFSSRX1	1 x Csl	Q	203	5169	2821	39.6288
		QN	191			
SDFFSSRX2	2 x Csl	Q	240	5230	2057	43.3152
		QN	199			

10.37. Scan Neg Edge DFF

SDFFNX1, SDFFNX2

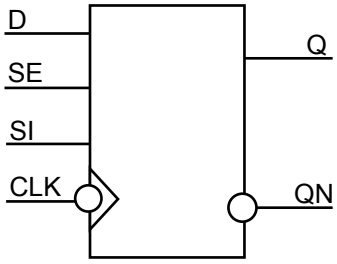


Figure 10.49. Logic Symbol of Scan Neg Edge DFF

Table 10.97. Scan Neg Edge DFF Transition Table

D	SI	SE	CLK	Q	QN
X	X	X	Inactive	No change	No change
1	X	0	Fall	1	0
0	X	0	Fall	0	1
X	1	1	Fall	1	0
X	0	1	Fall	0	1

Table 10.98. Scan Neg Edge DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFNX1	1 x Csl	Q	404	153	218	34.0992
		QN	366			
SDFFNX2	2 x Csl	Q	439	263	570	36.8640
		QN	389			

10.38. Scan Neg Edge DFF w/Async Low-Active Set

SDFFNASX1, SDFFNASX2

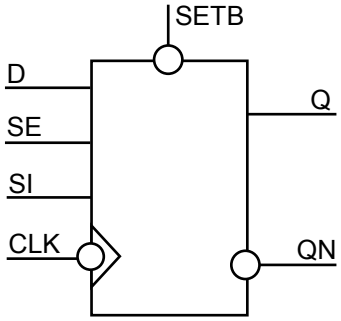


Figure 10.50. Logic Symbol of Scan Neg Edge DFF w/Async Low-Active Set

Table 10.99. Scan Neg Edge DFF w/Async Low-Active Set Transition Table

D	SI	SE	SETB	CLK	Q	QN
X	X	X	0	X	1	0
X	X	X	1	Inactive	No change	No change
1	X	0	1	Fall	1	0
0	X	0	1	Fall	0	1
X	1	1	1	Fall	1	0
X	0	1	1	Fall	0	1

Table 10.100. Scan Neg Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFNASX1	1 x Csl	Q	220	169	156	36.8640
		QN	195			
SDFFNASX2	2 x Csl	Q	287	271	647	39.6288
		QN	248			

10.39. Scan Neg Edge DFF w/Async Low-Active Reset

SDFFNARX1, SDFFNARX2

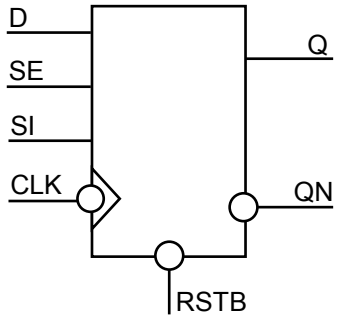


Figure 10.51. Logic Symbol of Scan Neg Edge DFF w/Async Low-Active Reset

Table 10.101. Scan Neg Edge DFF w/Async Low-Active Reset Transition Table

D	SI	SE	RSTB	CLK	Q	QN
X	X	X	0	X	0	1
X	X	X	1	Inactive	No change	No change
1	X	0	1	Fall	1	0
0	X	0	1	Fall	0	1
X	1	1	1	Fall	1	0
X	0	1	1	Fall	0	1

Table 10.102. Scan Neg Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFNARX1	1 x Csl	Q	222	175	233	37.7856
		QN	338			
SDFFNARX2	2 x Csl	Q	148	341	605	39.6288
		QN	239			

10.40. Scan Neg Edge DFF w/Async Low-Active Set & Reset

SDFFNASRX1, SDFFNASRX2

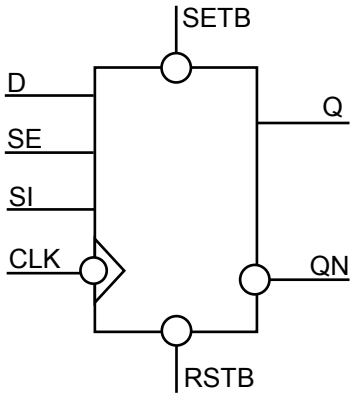


Figure 10.52. Logic Symbol of Scan Neg Edge DFF w/Async Low-Active Set & Reset

Table 10.103. Scan Neg Edge DFF w/Async Low-Active Set & Reset Transition Table

D	SI	SE	SETB	RSTB	CLK	Q	QN
X	X	X	0	0	X	X	X
X	X	X	0	1	X	1	0
X	X	X	1	0	X	0	1
X	X	X	1	1	Inactive	No change	No change
1	X	0	1	1	Fall	1	0
0	X	0	1	1	Fall	0	1
X	1	1	1	1	Fall	X	1
X	0	1	1	1	Fall	X	0

Table 10.104. Scan Neg Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFNASRX1	1 x Csl	Q	184	196	78	40.5504
		QN	367			
SDFFNASRX2	2 x Csl	Q	288	353	626	42.3936
		QN	279			

10.41. RS-NAND Latch

LNANDX1, LNANDX2

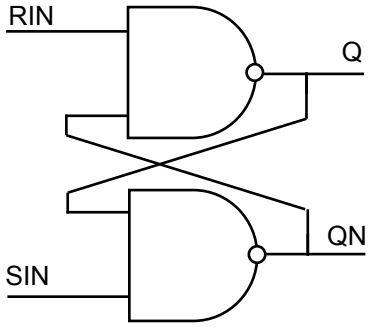


Figure 10.53. Logic Symbol of RS-NAND Latch

Table 10.105. RS-NAND Latch Transition Table

RIN	SIN	Q	QN
0	0	X	X
0	1	1	0
1	0	0	1
1	1	No change	No change

Table 10.106. RS-NAND Latch Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
LNANDX1	1 x Csl	Q	221	621	2359	10.1376
		QN	386			
LNANDX2	2 x Csl	Q	206	124	5741	18.4320
		QN	300			

10.42. High-Active Latch

LATCHX1, LATCHX2

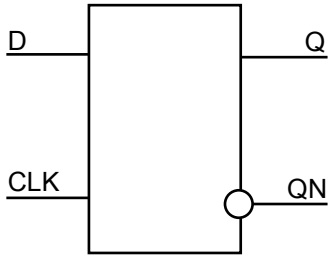


Figure 10.54. Logic Symbol of High-Active Latch

Table 10.107. High-Active Latch Transition Table

D	CLK	Q	QN
X	0	No change	No change
0	1	0	1
1	1	1	0

Table 10.108. High-Active Latch Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
LATCHX1	1 x Csl	Q	219	144	463	22.1184
		QN	234			
LATCHX2	2 x Csl	Q	254	188	681	25.8048
		QN	277			

10.43. High-Active Latch w/ Async Low-Active Set

LASX1, LASX2

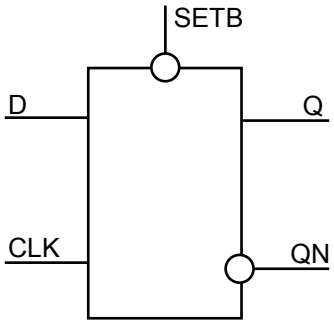


Figure 10.55. Logic Symbol of High-Active Latch w/ Async Low-Active Set

Table 10.109. High-Active Latch w/ Async Low-Active Set Transition Table

D	SETB	CLK	Q	QN
X	1	0	No change	No change
X	0	X	1	0
1	1	1	1	0
0	1	1	0	1

Table 10.110. High-Active Latch w/ Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
LASX1	1 x Csl	Q	223	117	485	24.8832
		QN	286			
LASX2	2 x Csl	Q	217	187	656	29.5696
		QN	320			

10.44. High-Active Latch w/ Async Low-Active Reset

LARX1, LARX2

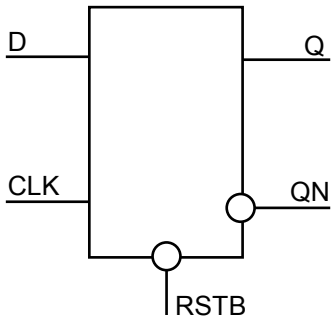


Figure 10.56. Logic Symbol of High-Active Latch w/ Async Low-Active Reset

Table 10.111. High-Active Latch w/ Async Low-Active Reset Transition Table

D	RSTB	CLK	Q	QN
X	1	0	No change	No change
X	0	X	0	1
1	1	1	1	0
0	1	1	0	1

Table 10.112. High-Active Latch w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
LARX1	1 x Csl	Q	257	140	496	25.8048
		QN	263			
LARX2	2 x Csl	Q	299	200	658	29.4912
		QN	281			

10.45. High-Active Latch w/ Async Low-Active Set & Reset

LASRX1, LASRX2

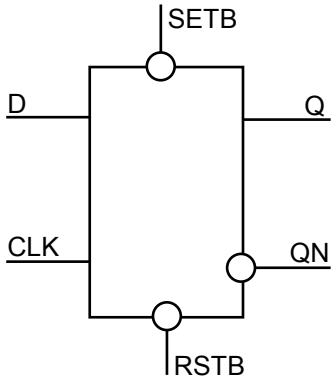


Figure 10.57. Logic Symbol of High-Active Latch w/ Async Low-Active Set & Reset

Table 10.113. High-Active Latch w/ Async Low-Active Set & Reset Transition Table

D	SETB	RSTB	CLK	Q	QN
X	1	1	X	X	X
X	0	1	X	1	0
X	1	0	X	0	1
X	1	1	0	No change	No change
1	1	1	1	1	0
0	1	1	1	0	1

Table 10.114. High-Active Latch w/ Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
LASRX1	1 x Csl	Q	280	139	426	26.7264
		QN	283			
LASRX2	2 x Csl	Q	336	240	577	31.3344
		QN	292			

10.46. High-Active Latch w/ Async Low-Active Set & Reset only Q out

LASRQX1, LASRQX2

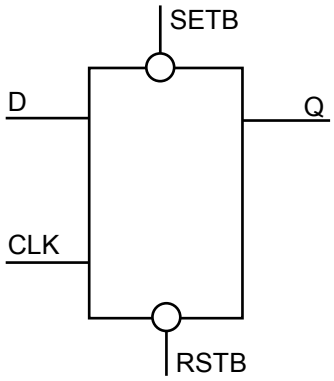


Figure 10.58. Logic Symbol of High-Active Latch w/ Async Low-Active Set & Reset only Q out

Table 10.115. High-Active Latch w/ Async Low-Active Set & Reset only Q out Transition Table

D	SETB	RSTB	CLK	Q
X	0	0	X	X
X	0	1	X	1
X	1	0	X	0
X	1	1	0	No change
1	1	1	1	1
0	1	1	1	0

Table 10.116. High-Active Latch w/ Async Low-Active Set & Reset only Q out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LASRQX1	1 x Csl	252	111	20756	25.8048
LASRQX2	2 x Csl	274	154	29383	26.7264

10.47. High-Active Latch w/ Async Low-Active Set & Reset only QN out

LASRNX1, LASRNX2

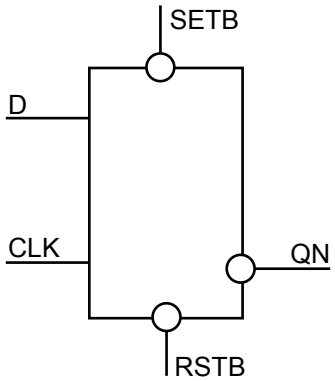


Figure 10.59. Logic Symbol of High-Active Latch w/ Async Low-Active Set & Reset only QN out

Table 10.117. High-Active Latch w/ Async Low-Active Set & Reset only QN out Transition Table

D	SETB	RSTB	CLK	QN
X	0	0	X	X
X	0	1	X	0
X	1	0	X	1
X	1	1	0	No change
1	1	1	1	0
0	1	1	1	1

Table 10.118. High-Active Latch w/ Async Low-Active Set & Reset only QN out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LASRNX1	1 x Csl	282	132	18467	25.8048
LASRNX2	2 x Csl	306	184	32164	27.6480

10.48. Clock Gating cell w/ Latched Pos Edge Control Post

CGLPPSX2, CGLPPSX4, CGLPPSX8, CGLPPSX16

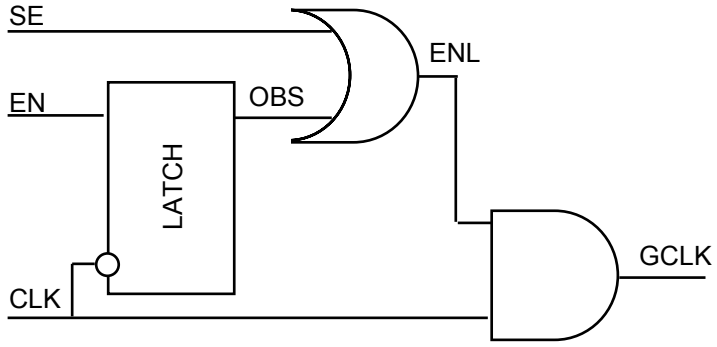


Figure 10.60. Logic Symbol of Clock Gating cell w/ Latched Pos Edge Control Post

Table 10.119. Clock Gating cell w/ Latched Pos Edge Control Post Truth Table

SE	EN	CLK	GCLK
1	X	0	0
1	X	1	1
0	0	0	0
0	0	1	OBS
0	1	0	0
0	1	1	1

Table 10.120. Clock Gating cell w/ Latched Pos Edge Control Post Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
CGLPPSX2	2 x Csl	149	195	19014	25.8048
CGLPPSX4	4 x Csl	159	306	46177	25.805
CGLPPSX8	8 x Csl	149	528	79156	33.1776
CGLPPSX16	16 x Csl	184	977	177360	47.0016

10.49. Clock Gating cell w/ Latched Neg Edge Control Post

CGLNPSX2, CGLNPSX4, CGLNPSX8, CGLNPSX16

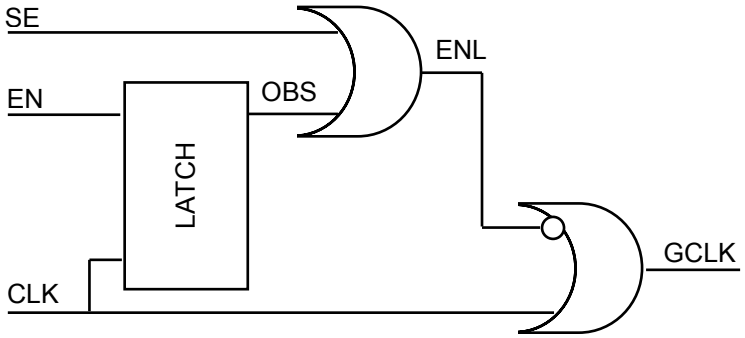


Figure 10.61. Logic Symbol of Clock Gating cell w/ Latched Neg Edge Control Post

Table 10.121. Clock Gating cell w/ Latched Neg Edge Control Post Truth Table

SE	EN	CLK	GCLK
1	X	0	0
1	X	1	1
0	0	0	!OBS
0	0	1	1
0	1	0	0
0	1	1	1

Table 10.122. Clock Gating cell w/ Latched Neg Edge Control Post Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
CGLNPSX2	2 x Csl	388	163	13283	23.0400
CGLNPSX4	4 x Csl	402	270	37938	23.04
CGLNPSX8	8 x Csl	433	487	123160	31.3344
CGLNPSX16	16 x Csl	490	914	175904	44.2368

10.50. Clock Gating cell w/ Latched Pos Edge Control Pre

CGLPPRX2, CGLPPRX8

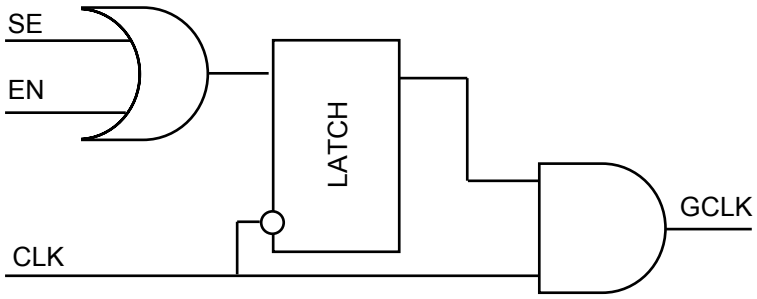


Figure 10.62. Logic Symbol of Clock Gating cell w/ Latched Pos Edge Control Pre

Table 10.123. Clock Gating cell w/ Latched Pos Edge Control Pre Truth Table

SE	EN	CLK	ENL
1	X	0	1
X	1	0	1
0	0	0	1
X	X	1	No change

ENL	CLK	GCLK
0	0	0
0	1	0
1	0	0
1	1	1

Table 10.124. Clock Gating cell w/ Latched Pos Edge Control Pre Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
CGLPPRX2	2 x Csl	246	169	18313	21.1968
CGLPPRX8	8 x Csl	209	491	7656	29.4912

10.51. Clock Gating cell w/ Latched Neg Edge Control Pre

CGLNPRX2, CGLNPRX8

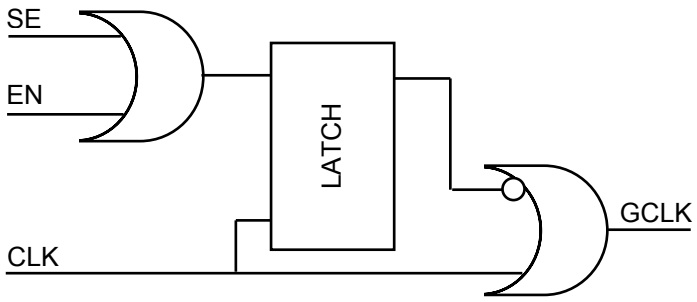


Figure 10.63. Logic Symbol of Clock Gating cell w/ Latched Neg Edge Control Pre

Table 10.125. Clock Gating cell w/ Latched Neg Edge Control Pre Truth Table

SE	EN	CLK	ENL
1	X	1	1
X	1	1	1
0	0	1	1
X	X	0	No change

ENL	CLK	GCLK
0	0	1
0	1	1
1	0	0
1	1	1

Table 10.126. Clock Gating cell w/ Latched Neg Edge Control Pre Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
CGLNPRX2	2 x Csl	244	172	18876	23.0400
CGLNPRX8	8 x Csl	260	499	88348	32.2560

10.52. Non-Inverting Delay Line

DELLN1X2, DELLN2X2, DELLN3X2

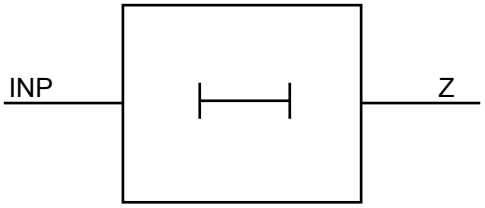


Figure 10.64. Logic Symbol of Non-Inverting Delay Line

Table 10.127. Non-Inverting Delay Line Truth Table

INP	Z
X	IN

Table 10.128. Non-Inverting Delay Line Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
DELLN1X2	2 x Csl	251	121	1585	14.7456
DELLN2X2	2 x Csl	416	122	711	15.6672
DELLN3X2	2 x Csl	589	140	23431	22.1184

10.53. Pass Gate

PGX1, PGX2, PGX4

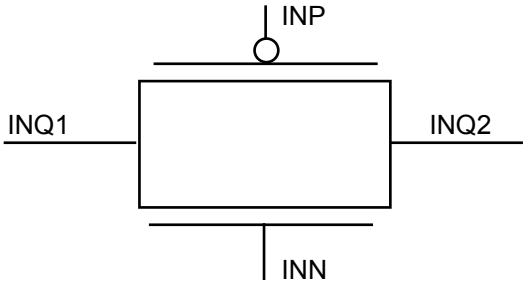


Figure 10.65. Logic Symbol of Pass Gate

Table 10.129. Pass Gate Truth Table

INQ1	INN	INP	INQ2	Notes
X	0	1	Z	
X	X	0	X	Not Allowed
X	1	X	X	Not Allowed
X	1	0	INQ1	

Table 10.130. Pass Gate Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
PGX1	1 x Csl	488	1.8	2966	7.3728
PGX2	2 x Csl	483	3.6	2910	8.2944
PGX4	4 x Csl	482	7.2	6353	10.1376

10.54. Bi-directional Switch w/ Active Low Enable

BSLEX1, BSLEX2, BSLEX4

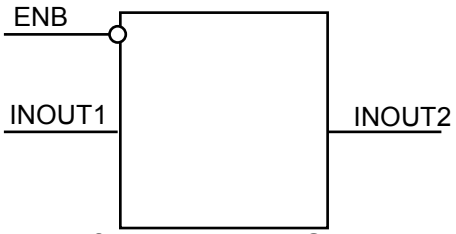


Figure 10.66. Logic Symbol of Bi-directional Switch w/ Active Low Enable

Table 10.131. Bi-directional Switch w/ Active Low Enable Truth Table

INOUT1	ENB	INOUT2
X	1	INOUT1
X	0	Z

Table 10.132. Bi-directional Switch w/ Active Low Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
BSLEX1	1 x Csl	84	17	3188	7.3728
BSLEX2	2 x Csl	84	34	5897	10.1376
BSLEX4	4 x Csl	82	69	6673	12.9024

10.55. Hold 0 Isolation Cell (Logic AND)

ISOLANDX1, ISOLANDX2, ISOLANDX4, ISOLANDX8

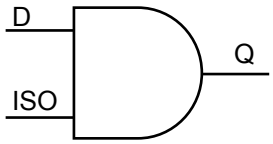


Figure 10.67. Logic Symbol of Hold 0 Isolation Cell (Logic AND)

Table 10.133. Hold 0 Isolation Cell (Logic AND) Truth Table

D	ISO	Q
0	X	0
X	0	0
1	1	1

Table 10.134. Hold 0 Isolation Cell (Logic AND) Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
ISOLANDX1	1 x Csl	186	219	11994	7.3728
ISOLANDX2	2 x Csl	203	380	21809	9.2016
ISOLANDX4	4 x Csl	368	702	70198	11.9808
ISOLANDX8	8 x Csl	258	1356	122438	18.4320

10.56. Hold 0 Isolation Cell (Logic AND), Always On

ISOLANDAOX1, ISOLANDAOX2, ISOLANDAOX4, ISOLANDAOX8

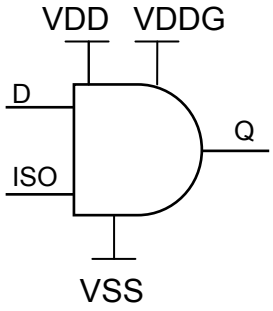


Figure 10.68.Logic Symbol of Hold 0 Isolation Cell (Logic AND),Always On

Table 10.135. Hold 0 Isolation Cell (Logic AND),Always On Truth Table

D	ISO	Q
0	X	0
1	1	0
1	0	1

Table 10.136. Hold 0 Isolation Cell (Logic AND), Always On Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
ISOLANDAOX1	1 x Csl	186	216	13427	7.3728
ISOLANDAOX2	2 x Csl	203	374	28574	9.2016
ISOLANDAOX4	4 x Csl	381	694	76241	29.4912
ISOLANDAOX8	8 x Csl	258	1333	151380	18.4320

10.57. Hold 1 Isolation Cell (Logic OR)

ISOLORX1, ISOLORX2, ISOLORX4, ISOLORX8

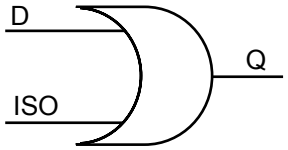


Figure 10.69. Logic Symbol of Hold 0 Isolation Cell (Logic OR)

Table 10.137. Hold 1 Isolation Cell (Logic OR) Truth Table

D	ISO	Q
0	0	0
X	1	1
1	X	1

Table 10.138. Hold 1 Isolation Cell (Logic OR) Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
ISOLORX1	1 x Csl	216	194	7877	7.3728
ISOLORX2	2 x Csl	244	354	15096	9.2160
ISOLORX4	4 x Csl	338	677	38100	11.9808
ISOLORX8	8 x Csl	380	1321	114755	17.5104

10.58. Hold 1 Isolation Cell (Logic OR),Always On

ISOLORAOX1, ISOLORAOX2, ISOLORAOX4, ISOLORAOX8

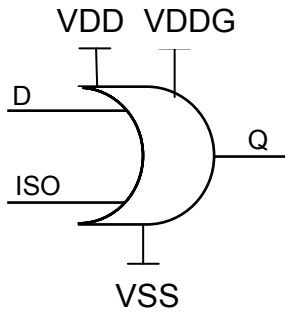


Figure 10.70. Logic Symbol of Hold 0 Isolation Cell (Logic OR), Always On

Table 10.139. Hold 1 Isolation Cell (Logic OR),Always On Truth Table

D	ISO	Q
0	0	0
0	1	1
1	X	1

Table 10.140. Hold 1 Isolation Cell (Logic OR), Always On Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
ISOLORAOX1	1 x Csl	216	528	8991	7.3728
ISOLORAOX2	2 x Csl	244	687	17486	9.2160
ISOLORAOX4	4 x Csl	350	1005	40873	35.0208
ISOLORAOX8	8 x Csl	380	1644	118905	17.5104

10.59. Low to High Level Shifter

LSUPX1, LSUPX2, LSUPX4, LSUPX8

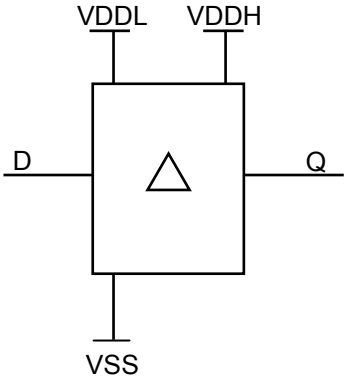


Figure 10.71. Logic Symbol of Low to High Level Shifter

Table 10.141. Low to High Level Shifter Truth Table

IN	OUT
0	0
1	1

Table 10.142. Low to High Level Shifter Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSUPX1	1 x Csl	274	257	16925	22.1184
LSUPX2	2 x Csl	299	418	26803	22.1184
LSUPX4	4 x Csl	332	742	53319	25.8048
LSUPX8	8 x Csl	418	1392	242441	36.8640

10.60. High to Low Level Shifter

LSDNX1, LSDNX2, LSDNX4, LSDNX8

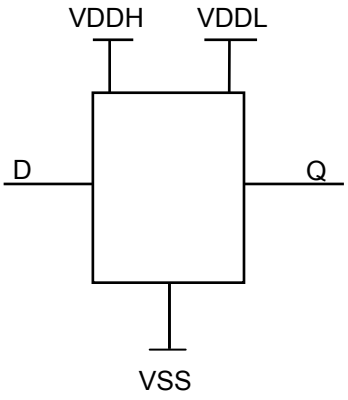


Figure 10.72. Logic Symbol of High to Low Level Shifter

Table 10.143. High to Low Level Shifter

IN	OUT
0	0
1	1

Table 10.144. High to Low Level Shifter Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNX1	1 x Csl	140	177	6750	33.176
LSDNX2	2 x Csl	188	334	18178	35.0208
LSDNX4	4 x Csl	292	618	32462	40.5504
LSDNX8	8 x Csl	185	1521	73831	58.9824

10.61. High to Low Level Shifter, single supply

LSDNSSX1, LSDNSSX2, LSDNSSX4, LSDNSSX8

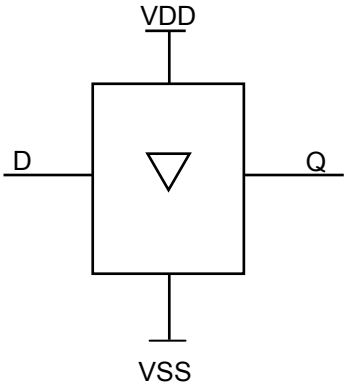


Figure 10.73. Logic Symbol of High to Low Level Shifter

Table 10.145. High to Low Level Shifter

D	Q
0	0
X	1
1	1

Table 10.146. High to Low Level Shifter,Single supply Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNSSX1	1 x Csl	140	177	6123	33.176
LSDNSSX2	2 x Csl	188	334	13253	35.0208
LSDNSSX4	4 x Csl	292	618	31854	10.1376
LSDNSSX8	8 x Csl	185	152	75692	58.9824

10.62. High to Low Level Shifter/ High Activ Enable, single supply

LSDNENSSX1, LSDNENSSX2, LSDNENSSX4, LSDNENSSX8

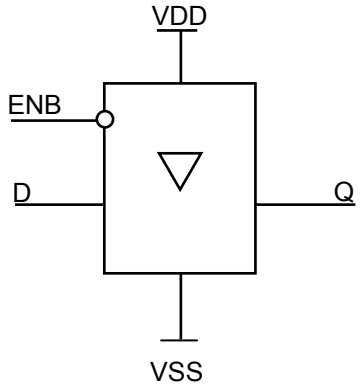


Figure 10.74. Logic Symbol of High to Low Level Shifter/High Activ Enable, single supply

Table 10.147. High to Low Level Shifter/High Activ Enable, single supply

D	Q
0	0
X	1
1	1

Table 10.148. High to Low Level Shifter/High Activ Enable,Single supply Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNENSSX1	1 x Csl	140	194	13260	33.176
LSDNENSSX2	2 x Csl	188	528	24043	35.0208
LSDNENSSX4	4 x Csl	313	199	6817	9.216
LSDNENSSX8	8 x Csl	185	1538	71086	58.9824

10.63. High to Low Level Shifter/ High Activ Enable, Clamp Low , Single supply

LSDNENCLSSX1, LSDNENCLSSX2, LSDNENCLSSX4, LSDNENCLSSX8

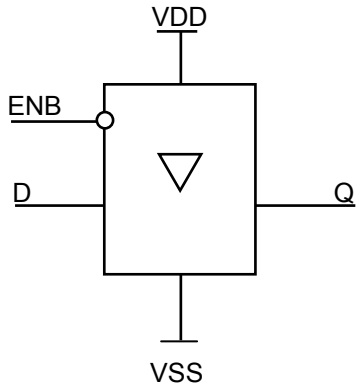


Figure 10.75. Logic Symbol of High to Low Level Shifter/High Activ Enable,Clamp Low, Single Supply

Table 10.149. High to Low Level Shifter/High Activ Enable, Clamp Low,Single Supply

D	Q
0	0
X	1
1	1

Table 10.150. High to Low Level Shifter/High Activ Enable,Single supply Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNENCLSSX1	1 x Csl	140	202	8826	33.176
LSDNENCLSSX2	2 x Csl	188	536	24323	35.0208
LSDNENCLSSX4	4 x Csl	275	894	46062	19.3536
LSDNENCLSSX8	8 x Csl	185	1564	78200	58.9824

10.64. Low to High Level Shifter/ Active Low Enable

LSUPENX1, LSUPENX2, LSUPENX4, LSUPENX8

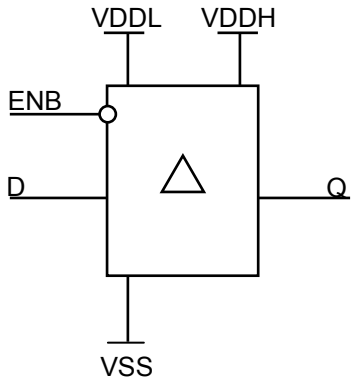


Figure 10.76. Logic Symbol of Low to High Level Shifter/Active Low Enable

Table 10.151. Low to High Level Shifter /Active Low Enable Truth Table

IN	EN	OUT
X	1	1
0	0	0
1	0	1

Table 10.152. Low to High Level Shifter/Active Low Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSUPENX1	1 x Csl	311	432	12791	31.3344
LSUPENX2	2 x Csl	287	563	22348	37.7072
LSUPENX4	4 x Csl	250	1195	41203	44.2368
LSUPENX8	8 x Csl	327	1817	89475	57.1392

10.65. High to Low Level Shifter/ Active Low Enable

LSDNENX1, LSDNENX2, LSDNENX4, LSDNENX8

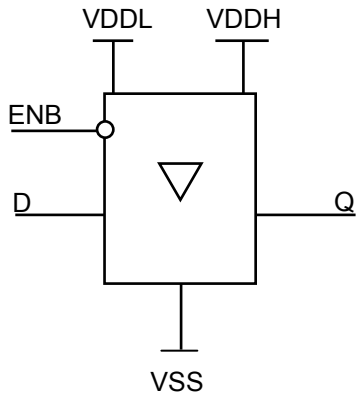


Figure 10.77. Logic Symbol of High to Low Level Shifter/Active Low Enable

Table 10.153. High to Low Level Shifter / Active Low Enable Truth Table

IN	EN	OUT
X	1	1
0	0	0
1	0	1

Table 10.154. High to Low Level Shifter/ Active Low Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNENX1	1 x Csl	133	325	11626	42.3936
LSDNENX2	2 x Csl	157	676	12118	27.648
LSDNENX4	4 x Csl	254	1182	39540	44.2368
LSDNENX8	8 x Csl	273	2594	76265	66.3552

10.66. Low to High Level Shifter/ Active Low Enable

LSUPENCLX1, LSUPENCLX2, LSUPENCLX4, LSUPENCLX8

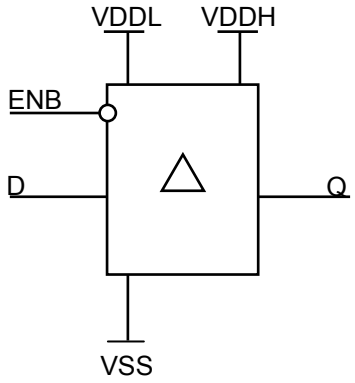


Figure 10.78. Logic Symbol of Low to High Level Shifter/Active Low Enable

Table 10.155. Low to High Level Shifter /Active Low Enable Truth Table

IN	EN	OUT
X	1	0
0	0	0
1	0	1

Table 10.156. Low to High Level Shifter/Active Low Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSUPENCLX1	1 x Csl	363	270	22244	27.648
LSUPENCLX2	2 x Csl	388	397	23038	27.648
LSUPENCLX4	4 x Csl	696	927	64209	47.9232
LSUPENCLX8	8 x Csl	713	2935	435550	88.4736

10.67. High to Low Level Shifter/ Active Low Enable

LSDNENCLX1, LSDNENCLX2, LSDNENCLX4, LSDNENCLX8

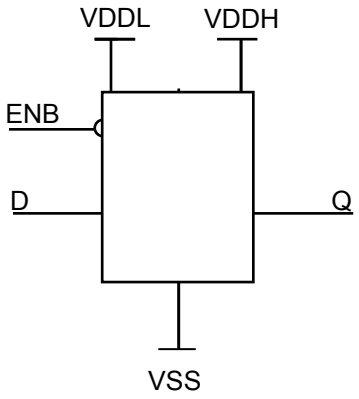


Figure 10.79. Logic Symbol of High to Low Level Shifter/Active Low Enable

Table 10.157. High to Low Level Shifter / Active Low Enable Truth Table

IN	EN	OUT
X	1	0
0	0	0
1	0	1

Table 10.158. High to Low Level Shifter/ Active Low Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNENCLX1	1 x Csl	145	401	13878	42.3936
LSDNENCLX2	2 x Csl	176	880	38880	73.728
LSDNENCLX4	4 x Csl	256	880	38880	75.2544
LSDNENCLX8	8 x Csl	209	1411	72562	87.696

10.68. Pos Edge Retention DFF

RDFFX1, RDFFX2

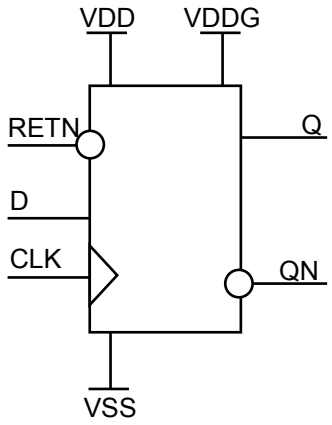


Figure 10.80. Logic Symbol of Pos Edge Retention DFF

Table 10.159. Pos Edge Retention DFF Transition Table

D	CLK	RETN	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	Rise	1	Q2[n]	0	1	Normal mode write 0
1	Rise	1	Q2[n]	1	0	Normal mode write 1
X	Rise	0	Q[n]	Q[n]	QN[n]	Retention mode
X	Fall	X	Q2[n]	Q[n]	QN[n]	
X	0	X	Q2[n]	Q[n]	QN[n]	
X	1	X	Q2[n]	Q[n]	QN[n]	

Table 10.160. Pos Edge Retention DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RDFFX1	1 x Csl	Q	237	635	338	57.96
		QN	284			
RDFFX2	2 x Csl	Q	261	836	514	58.9824
		QN	327			

10.69. Scan Pos Edge Retention DFF

RSDFFX1, RSDFFX2

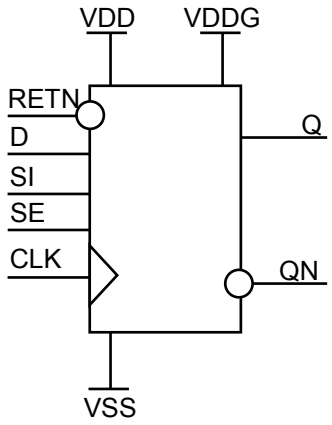


Figure 10.81. Logic Symbol of Scan Pos Edge Retention DFF

Table 10.161. Scan Pos Edge Retention DFF Transition Table

D	CLK	SI	SE	RETN	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	Rise	0	1	1	Q2[n]	0	1	Normal mode write 0
X	Rise	1	1	1	Q2[n]	1	0	Normal mode write 1
0	Rise	X	0	1	Q2[n]	0	1	Scan mode write 0
1	Rise	X	0	1	Q2[n]	1	0	Scan mode write 1
X	Rise	X	X	0	Q[n]	Q[n]	QN[n]	Retention mode
X	Fall	X	X	X	Q2[n]	Q[n]	QN[n]	
X	0	X	X	X	Q2[n]	Q[n]	QN[n]	
X	1	X	X	X	Q2[n]	Q[n]	QN[n]	

Table 10.162. Scan Pos Edge Retention DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RSDFFX1	1 x Csl	Q	240	780	417	66.3552
		QN	287			
RSDFFX2	2 x Csl	Q	256	981	516	68.1984
		QN	323			

10.70. Scan Pos Edge Retention DFF,w/Async Low Activ Reset

RSDFFARX1, RSDFFARX2

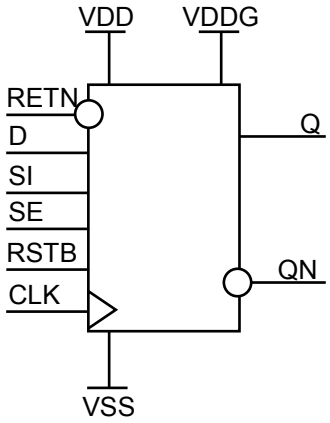


Figure 10.82. Logic Symbol of Scan Pos Edge Retention DFF,w/Async Low Activ Reset

Table 10.163. Scan Pos Edge Retention DFF,w/Async Low Activ Reset Transition Table

RETN	RSTB	CLK	D	SI	SE	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
1	1	Rise	X	0	1	Q2[n]	0	1	Scan mode write 0
1	1	Rise	X	1	1	Q2[n]	1	0	Scan mode write 1
1	1	Rise	0	X	0	Q2[n]	0	1	Normal mode write 0
1	1	Rise	1	X	0	Q2[n]	1	0	Normal mode write 1
0	1	Rise	X	X	X	Q[n]	Q[n]	QN[n]	Retention mode
X	1	Fall	X	X	X	Q2[n]	Q[n]	QN[n]	
X	1	0	X	X	X	Q2[n]	Q[n]	QN[n]	
X	1	1	X	X	X	Q2[n]	Q[n]	QN[n]	
X	0	X	X	X	X	0	0	1	Reset

Table 10.164. Scan Pos Edge Retention DFF,w/Async Low Activ Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RSDFFARX1	1 x Csl	Q	240	854	481	66.3552
		QN	287			
RSDFFARX2	2 x Csl	Q	256	1056	565	68.1984
		QN	323			

10.71. Neg Edge Retention DFF

RDFFNX1, RDFFNX2

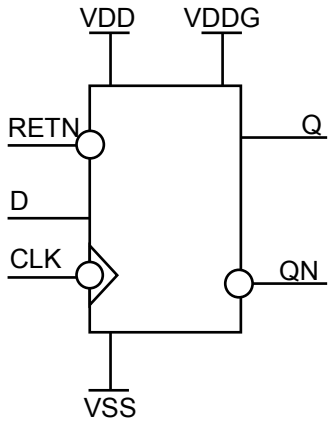


Figure 10.83. Logic Symbol of Pos Edge Retention DFF

Table 10.165. Neg Edge Retention DFF Transition Table

D	CLK	RETN	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	Fall	1	Q2[n]	0	1	Normal mode write 0
1	Fall	1	Q2[n]	1	0	Normal mode write 1
X	Fall	0	Q[n]	Q[n]	QN[n]	Retention mode
X	Rise	X	Q2[n]	Q[n]	QN[n]	
X	0	X	Q2[n]	Q[n]	QN[n]	
X	1	X	Q2[n]	Q[n]	QN[n]	

Table 10.166. Neg Edge Retention DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RDFFNX1	1 x Csl	Q	359	663	424	57.1392
		QN	410			
RDFFNX2	2 x Csl	Q	373	877	568	58.9824
		QN	440			

10.72. Scan Neg Edge Retention DFF

RSDFFNX1, RSDFFNX2

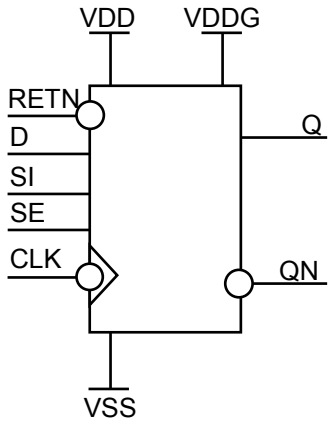


Figure 10.84. Logic Symbol of Scan Neg Edge Retention DFF

Table 10.167. Scan Neg Edge Retention DFF Transition Table

RETN	D	CLK	SI	SE	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
1	X	Fall	0	1	Q2[n]	0	1	Scan mode write 0
1	X	Fall	1	1	Q2[n]	1	0	Scan mode write 1
1	0	Fall	X	0	Q2[n]	0	1	Normal mode write 0
1	1	Fall	X	0	Q2[n]	1	0	Normal mode write 1
0	X	Fall	X	X	Q[n]	Q[n]	QN[n]	Retention mode
X	X	Rise	X	X	Q2[n]	Q[n]	QN[n]	
X	X	0	X	X	Q2[n]	Q[n]	QN[n]	
X	X	1	X	X	Q2[n]	Q[n]	QN[n]	

Table 10.168. Scan Neg Edge Retention DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RSDFFNX1	1 x Csl	Q	363	810	518	66.3552
		QN	409			
RSDFFNX2	2 x Csl	Q	368	1024	671	68.1984
		QN	438			

10.73. Scan Neg Edge Retention DFF,w/Async Low Activ Reset

RSDFFNARX1, RSDFFNARX2

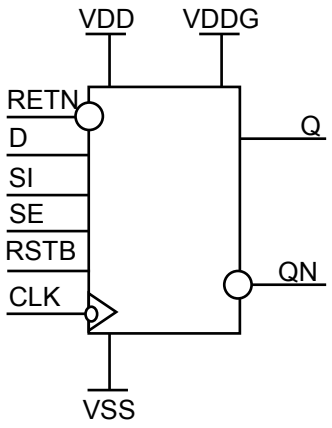


Figure 10.85. Logic Symbol of Scan Neg Edge Retention DFF,w/Async low Activ Reset

Table 10.169. Scan Neg Edge Retention DFF,w/Async low Activ reset Transition Table

RETN	RSTB	D	CLK	SI	SE	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
1	1	X	Fall	0	1	Q2[n]	0	1	Scan mode write 0
1	1	X	Fall	1	1	Q2[n]	1	0	Scan mode write 1
1	1	0	Fall	X	0	Q2[n]	0	1	Normal mode write 0
1	1	1	Fall	X	0	Q2[n]	1	0	Normal mode write 1
0	1	X	Fall	X	X	Q[n]	Q[n]	QN[n]	Retention mode
X	1	X	Rise	X	X	Q2[n]	Q[n]	QN[n]	
X	1	X	0	X	X	Q2[n]	Q[n]	QN[n]	
X	1	X	1	X	X	Q2[n]	Q[n]	QN[n]	
X	0	X	X	X	X	0	0	1	Reset

Table 10.170. Scan Neg Edge Retention DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RSDFFNARX1	1 x Csl	Q	363	886	528	66.3552
		QN	409			
RSDFFNARX2	2 x Csl	Q	368	1104	616	68.1984
		QN	438			

10.74. Pos Edge DFF SR

RDFFSRX1, RDFFSRX2

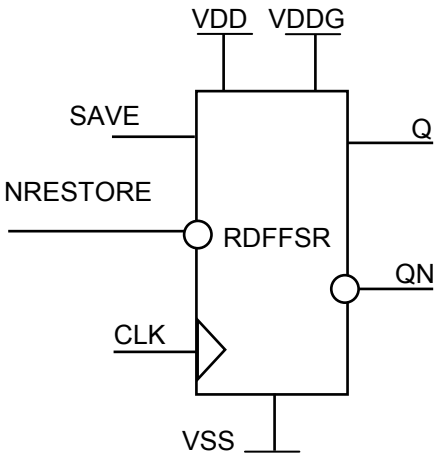


Figure 10.86. Logic Symbol of Pos Edge DFF SR

Table 10.171. Pos Edge DFF SR Transition Table

SAVE	NRESTORE	D	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	1	0	Rise	Q2[n]	0	1	Normal mode write 0
0	1	1	Rise	Q2[n]	1	0	Normal mode write 1
0	X	X	Fall	Q2[n]	Q[n]	QN[n]	
0	X	X	0	Q2[n]	Q[n]	QN[n]	
0	1	X	1	Q2[n]	Q[n]	QN[n]	
1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
0	0	X	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
0	0	X	0	Q2[n]	Q[n]	QN[n]	

Table 10.172. Pos Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFSRX1	1 x Csl	QN	240	616	57568	71.8848
RDFFSRX2	2 x Csl	QN	259	904	107187	70.9632

10.75. Pos Edge Retention DFF,w/Async Low Activ Reset

RDFFARX1, RDFFARX2

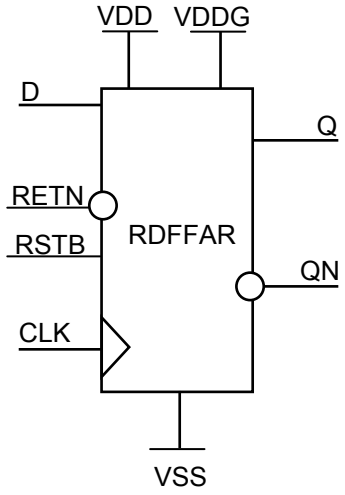


Figure 10.87. Logic Symbol of Pos Edge DFF SR

Table 10.173. Pos Edge DFF, w/Async Low Activ Reset Transition Table

CLK	D	RETN	RSTB	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
Rise	0	1	1	Q2[n]	0	1	Normal mode write 0
Rise	1	1	1	Q2[n]	1	0	Normal mode write 1
Rise	X	0	1	Q[n]	Q[n]	QN[n]	Retention mode
Fall	X	X	1	Q2[n]	Q[n]	QN[n]	
0	X	X	1	Q2[n]	Q[n]	QN[n]	
1	X	X	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	0	0	1	Reset

Table 10.174. Pos Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFARX1	1 x Csl	QN	240	713	400	71.8848
RDFFARX2	2 x Csl	QN	259	912	477	70.9632

10.76. Neg Edge Retention DFF,w/Async Low Activ Reset

RDFFNARX1, RDFFNARX2

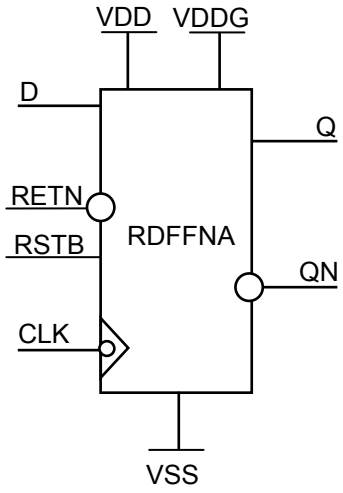


Figure 10.88. Logic Symbol of Pos Edge DFF SR

Table 10.175. Neg Edge DFF,w/Async Low Activ Reset Transition Table

CLK	D	RETN	RSTB	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
Fall	0	1	1	Q2[n]	0	1	Normal mode write 0
Fall	1	1	1	Q2[n]	1	0	Normal mode write 1
Fall	X	0	1	Q[n]	Q[n]	QN[n]	Retention mode
Rise	X	X	1	Q2[n]	Q[n]	QN[n]	
0	X	X	1	Q2[n]	Q[n]	QN[n]	
1	X	X	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	0	0	1	Reset

Table 10.176. Pos Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNARX1	1 x Csl	QN	240	742	445	71.8848
RDFFNARX2	2 x Csl	QN	259	959	529	70.9632

10.77. Pos Edge DFF SR, w/ Async Low-Active Set

RDFFSRASX1, RDFFSRASX2

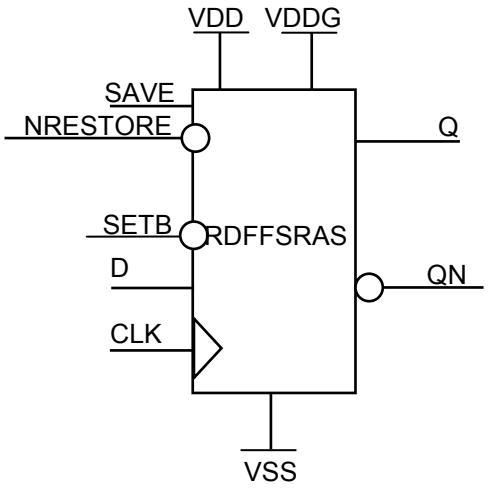


Figure 10.89. Logic Symbol of Pos Edge DFF SR, w/ Async Low-Active Set

Table 10.177. Pos Edge DFF SR, w/ Async Low-Active Set Transition Table

SAVE	NRESTORE	SETB	CLK	D	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	0	X	X	Q2[n]	1	0	SETB mode
0	1	1	Rise	0	Q2[n]	0	1	Normal made write 0
0	1	1	Rise	1	Q2[n]	1	0	Normal mode write 1
0	X	1	Fall	X	Q2[n]	Q[n]	QN[n]	
0	X	1	0	X	Q2[n]	Q[n]	QN[n]	
0	1	1	1	X	Q2[n]	Q[n]	QN[n]	
1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
0	0	1	1	X	Q2[n]	Q2[n]	!Q2[n]	Restore mode
0	0	1	0	X	Q2[n]	Q[n]	QN[n]	

Table 10.178. Pos Edge DFF SR, w/ Async Low-Active Set

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFSRASX1	1 x Csl	QN	340	681	340	80.1792
RDFFSRASX2	2 x Csl	QN	370	948	402	85.7089

10.78. Pos Edge DFF SR, w/ Async Low-Active Reset

RDFFSRARX1, RDFFSRARX2

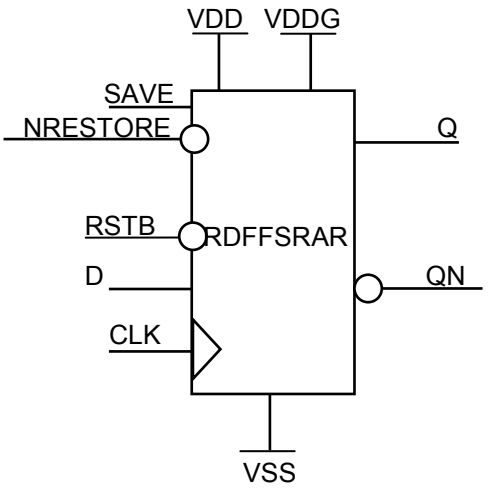


Figure 10.90. Logic Symbol of Pos Edge DFF SR, w/ Async Low-Active Reset

Table 10.179. Pos Edge DFF SR, w/ Async Low-Active Reset Transition Table

SAVE	NRESTORE	RSTB	CLK	D	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	0	X	X	Q2[n]	0	1	RSTB mode
0	1	1	Rise	0	Q2[n]	0	1	Normal made write 0
0	1	1	Rise	1	Q2[n]	1	0	Normal mode write 1
0	X	1	Fall	X	Q2[n]	Q[n]	QN[n]	
0	X	1	0	X	Q2[n]	Q[n]	QN[n]	
0	1	1	1	X	Q2[n]	Q[n]	QN[n]	
1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
0	0	1	1	X	Q2[n]	Q2[n]	!Q2[n]	Restore mode
0	0	1	0	X	Q2[n]	Q[n]	QN[n]	

Table 10.180. Pos Edge DFF SR, w/ Async Low-Active Reset

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFSRARX1	1 x Csl	QN	400	732	27365	73.728
RDFFSRARX2	2 x Csl	QN	423	105	49245	88.4736

10.79. Pos Edge DFF SR, w/ Async Low-Active Set & Reset

RDFFSRASRX1, RDFFSRASRX2

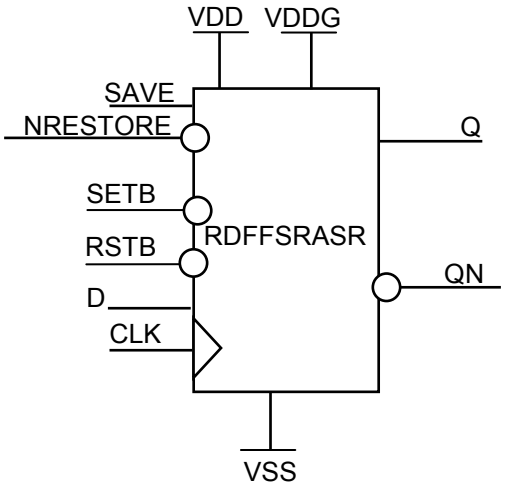


Figure 10.91. Logic Symbol of Pos Edge DFF SR, w/ Async Low-Active Set & Reset

Table 10.181. Pos Edge DFF SR, w/ Async Low-Active Set & Reset Transition Table

SAVE	NRESTORE	SETB	RSTB	D	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	X	0	X	X	Q2[n]	0	1	RSTB mode
0	X	0	1	X	X	Q2[n]	1	0	SETB mode
0	1	1	1	0	Rise	Q2[n]	0	1	Normal mode write 0
0	1	1	1	1	Rise	Q2[n]	1	0	Normal mode write 1
0	X	1	1	X	Fall	Q2[n]	Q[n]	QN[n]	
0	X	1	1	X	0	Q2[n]	Q[n]	QN[n]	
0	1	1	1	X	1	Q2[n]	Q[n]	QN[n]	
1	X	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
0	0	1	1	X	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
0	0	1	1	X	0	Q2[n]	Q[n]	QN[n]	

Table 10.182. Pos Edge DFF SR, w/ Async Low-Active Set & Reset

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFSRASRX1	1 x Csl	QN	465	749	25930	80.1792
RDFFSRASRX2	2 x Csl	QN	493	1098	44321	85.7088

10.80. Pos Edge DFF SR, w/ Sync Low-Active Set & Reset

RDFFSRSSRX1, RDFFSRSSRX2

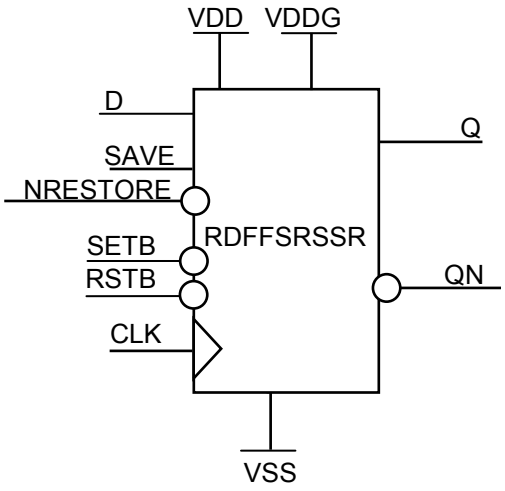


Figure 10.92. Logic Symbol of Pos Edge DFF SR, w/ Sync Low-Active Set & Reset

Table 10.183. Pos Edge DFF SR, w/ Sync Low-Active Set & Reset Transition Table

D	SAVE	NRESTORE	SETB	RSTB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	0	X	X	0	Rise	Q2[n]	0	1	RSTB mode
X	0	X	0	1	Rise	Q2[n]	1	0	SETB mode
0	0	1	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	0	1	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	0	X	X	X	Fall	Q2[n]	Q[n]	QN[n]	
X	0	X	X	X	0	Q2[n]	Q[n]	QN[n]	
X	0	1	X	X	1	Q2[n]	Q[n]	QN[n]	
X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	0	0	1	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	0	0	1	1	0	Q2[n]	Q[n]	QN[n]	

Table 10.184. Pos Edge DFF SR, w/ Sync Low-Active Set & Reset

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFSRSSRX1	1 x Csl	QN	339	7328	48586	82.0224
RDFFSRSSRX2	2 x Csl	QN	416	7613	81891	95.8464

10.81. Neg Edge DFF SR

RDFFNSRX1, RDFFNSRX2

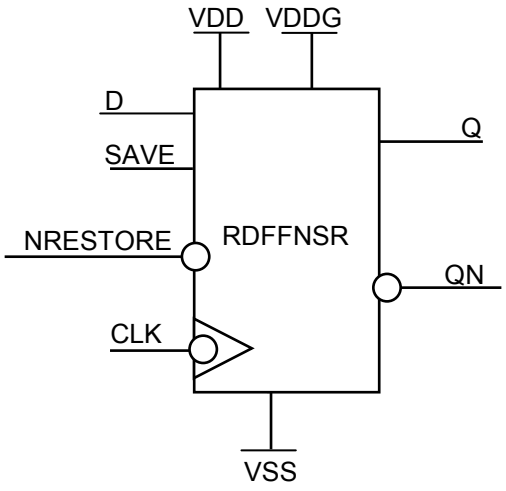


Figure 10.93. Logic Symbol of Neg Edge DFF SR

Table 10.185. Neg Edge DFF SR Transition Table

D	SAVE	NRESTORE	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	0	1	Fall	Q2[n]	0	1	Normal mode write 0
1	0	1	Fall	Q2[n]	1	0	Normal mode write 1
X	0	X	Rise	Q2[n]	Q[n]	QN[n]	
X	0	X	1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	Q2[n]	Q[n]	QN[n]	
X	1	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	0	0	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	0	0	1	Q2[n]	Q[n]	QN[n]	

Table 10.186. Neg Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRX1	1 x Csl	QN	392	616	370	71.8848
RDFFNSRX2	2 x Csl	QN	414	905	729	70.9632

10.82. Neg Edge DFF SR, w/ Async Low-Active Set

RDFFNSRASX1, RDFFNSRASX2

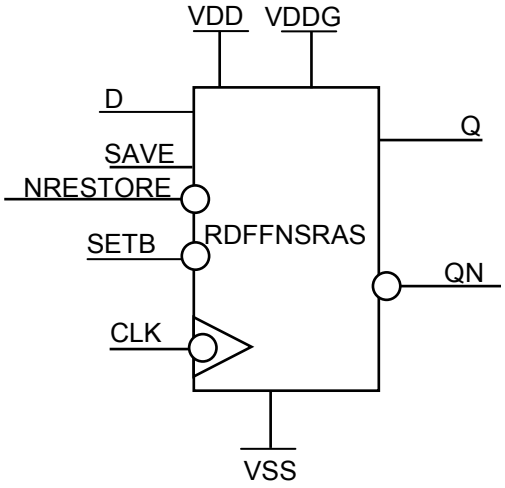


Figure 10.94. Logic Symbol of Edge DFF SR, w/ Async Low-Active Set

Table 10.187. Edge DFF SR, w/ Async Low-Active Set Transition Table

D	SAVE	NRESTORE	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Notes
X	0	X	0	X	Q2[n]	1	0	SETB mode
0	0	1	1	Fall	Q2[n]	0	1	Normal mode 0
1	0	1	1	Fall	Q2[n]	1	0	Normal mode 1
X	0	X	1	Rise	Q2[n]	Q[n]	QN[n]	
X	0	X	1	1	Q2[n]	Q[n]	QN[n]	
X	0	1	1	0	Q2[n]	Q[n]	QN[n]	
X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	0	0	1	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	0	0	1	1	Q2[n]	Q[n]	QN[n]	

Table 10.188. Neg Edge DFF SR, w/ Async Low-Active Set Electrical Parameters and Area

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRASX1	1 x Csl	QN	343	688	350	80.1792
RDFFNSRASX2	2 x Csl	QN	375	934	396	86.6304

10.83. Neg Edge DFF SR, w/ Async Low-Active Reset

RDFFNSRARX1, RDFFNSRARX2

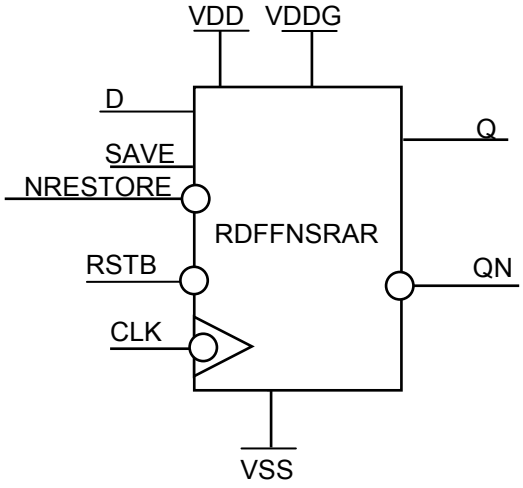


Figure 10.95. Logic Symbol of Pos Edge DFF SR, w/ Async Low-Active Reset

Table 10.189. Edge Pos Edge DFF SR, w/ Async Low-Active Reset Transition Table

D	SAVE	NRESTORE	RSTB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Notes
X	0	X	0	X	Q2[n]	0	1	RSTB mode
0	0	1	1	Fall	Q2[n]	0	1	Normal mode write 0
1	0	1	1	Fall	Q2[n]	1	0	Normal mode write 1
X	0	X	1	Rise	Q2[n]	Q[n]	QN[n]	
X	0	X	1	1	Q2[n]	Q[n]	QN[n]	
X	0	1	1	0	Q2[n]	Q[n]	QN[n]	Save mode
X	1	X	X	X	Q[n]	Q[n]	QN[n]	Restore mode
X	0	0	1	0	Q2[n]	Q2[n]	!Q2[n]	
X	0	0	1	1	Q2[n]	Q[n]	QN[n]	

Table 10.190. Pos Edge DFF SR, w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRARX1	1 x Csl	QN	395	678	28891	77.4144
RDFFNSRARX2	2 x Csl	QN	422	965	51869	77.4144

10.84. Neg Edge DFF SR, w/ Async Low-Active Set & Reset

RDFFNSRASRX1, RDFFNSRASRX2

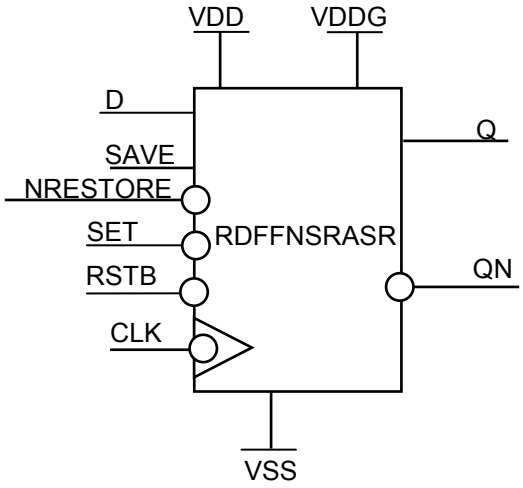


Figure 10.96. Logic Symbol of Neg Edge DFF SR, w/ Async Low-Active Set & Reset

Table 10.191. Neg Edge DFF SR, w/ Async Low-Active Set & Reset Transition Table

D	SAVE	NRESTORE	SETB	RSTB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	0	X	X	0	X	Q2[n]	0	1	RSTB mode
X	0	X	0	1	X	Q2[n]	1	0	SETB mode
0	0	1	1	1	Fall	Q2[n]	0	1	Normal mode write 0
1	0	1	1	1	Fall	Q2[n]	1	0	Normal mode write 1
X	0	X	1	1	Rise	Q2[n]	Q[n]	QN[n]	
X	0	X	1	1	1	Q2[n]	Q[n]	QN[n]	
X	0	1	1	1	0	Q2[n]	Q[n]	QN[n]	
X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	0	0	1	1	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	0	0	1	1	1	Q2[n]	Q[n]	QN[n]	

Table 10.192. Neg Edge DFF SR, w/ Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRASRX1	1 x Csl	QN	465	749	25763	80.1792
RDFFNSRASRX2	2 x Csl	QN	496	1084	45211	86.6304

10.85. Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out

RDFFNSRASRQX1, RDFFNSRASRQX2

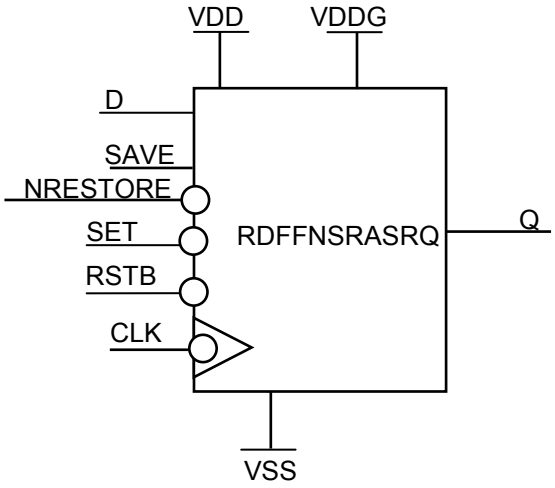


Figure 10.97. Logic Symbol of Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out

Table 10.193.Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out Transition Table

D	SAVE	NRESTORE	SETB	RSTB	CLK	Q2[n+1]	Q[n+1]	Mode
X	0	X	X	0	X	Q2[n]	0	RSTB mode
X	0	X	0	1	X	Q2[n]	1	SETB mode
0	0	1	1	1	Fall	Q2[n]	0	Normal mode write 0
1	0	1	1	1	Fall	Q2[n]	1	Normal mode write 1
X	0	X	1	1	Rise	Q2[n]	Q[n]	
X	0	X	1	1	1	Q2[n]	Q[n]	
X	0	1	1	1	0	Q2[n]	Q[n]	
X	1	X	X	X	X	Q[n]	Q[n]	Save mode
X	0	0	1	1	0	Q2[n]	Q2[n]	Restore mode
X	0	0	1	1	1	Q2[n]	Q[n]	

Table 10.194. Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRASRQX1	1 x Csl	Q	205	712	31437	80.1792
RDFFNSRASRXQ2	2 x Csl	Q	245	822	45462	80.1792

10.86. Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out

RDFFNSRASRNX1, RDFFNSRASRNX2

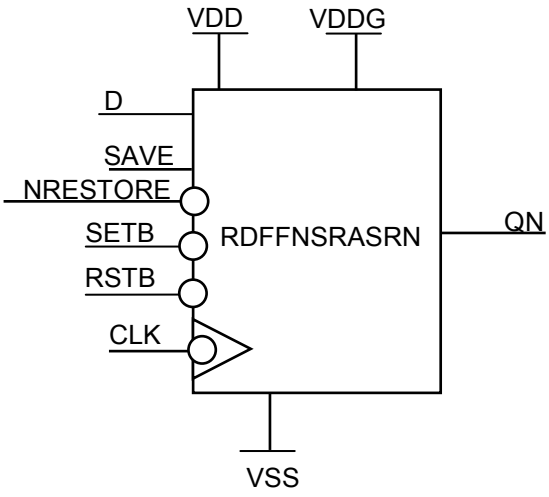


Figure 10.98. Logic Symbol of Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out

Table 10.195. Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out Transition Table

D	SAVE	NRESTORE	SETB	RSTB	CLK	Q2[n+1]	QN[n+1]	Mode
X	0	X	X	0	X	Q2[n]	0	RSTB mode
X	0	X	0	1	X	Q2[n]	1	SETB mode
0	0	1	1	1	Fall	Q2[n]	1	Normal mode write 0
1	0	1	1	1	Fall	Q2[n]	0	Normal mode write 1
X	0	X	1	1	Rise	Q2[n]	Q[n]	
X	0	X	1	1	1	Q2[n]	Q[n]	
x	0	1	1	1	0	Q2[n]	Q[n]	
X	1	X	X	X	X	Q[n]	Q[n]	Save mode
X	0	0	1	1	0	Q2[n]	Q2[n]	Restore mode
X	0	0	1	1	1	Q2[n]	Q[n]	

Table 10.196. Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRASRNX1	1 x Csl	QN	462	636	37558	80.1792
RDFFNSRASRNX2	2 x Csl	QN	493	815	74653	80.1792

10.87. Scan Pos Edge DFF SR

RSDFFSRX1, RSDFFSRX2

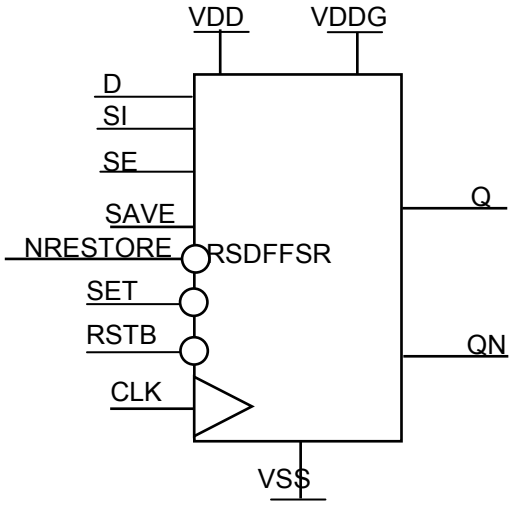


Figure 10.99. Logic Symbol of Scan Pos Edge DFF SR

Table 10.197. Scan Pos Edge DFF SR Transition Table

D	SAVE	NRESTORE	CLK	SE	SI	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	0	1	Rise	0	X	Q2[n]	0	1	Normal mode write 0
1	0	1	Rise	0	X	Q2[n]	1	0	Normal mode write 1
X	0	X	Fall	X	X	Q2[n]	Q[n]	QN[n]	
X	0	X	0	X	X	Q2[n]	Q[n]	QN[n]	
X	0	1	1	X	X	Q2[n]	Q[n]	QN[n]	
X	0	1	Rise	1	0	Q2[n]	0	1	Scan mode write 0
X	0	1	Rise	1	1	Q2[n]	1	0	Scan mode write 1
X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	0	0	1	X	X	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	0	0	0	X	X	Q2[n]	Q[n]	QN[n]	

Table 10.198. Scan Pos Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFSRX1	1 x Csl	QN	239	878	51252	79.2576
RSDFFSRX2	2 x Csl	QN	250	1168	97751	80.1792

10.88. Scan Pos Edge DFF SR, w/ Async Low-Active Set

RSDFFSRASX1, RSDFFSRASX2

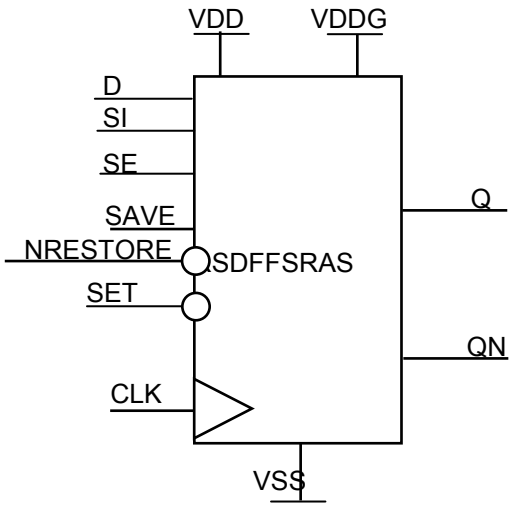


Figure 10.100. Logic Symbol of Scan Pos Edge DFF SR, w/ Async Low-Active Set

Table 10.199. Scan Pos Edge DFF SR, w/ Async Low-Active Set Transition Table

D	SI	SE	SAVE	NRESTORE	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	Fall	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	0	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1		1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	Rise	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	Rise	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	0	Q2[n]	Q[n]	QN[n]	

Table 10.200. Scan Pos Edge DFF SR, w/ Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFSRASX1	1 x Csl	QN	355	961	587	90.3168
RSDFFSRASX2	2 x Csl	QN	411	1145	688	98.6112

10.89. Scan Pos Edge DFF SR, w/ Async Low-Active Reset

RSDFFSRARX1, RSDFFSRARX2

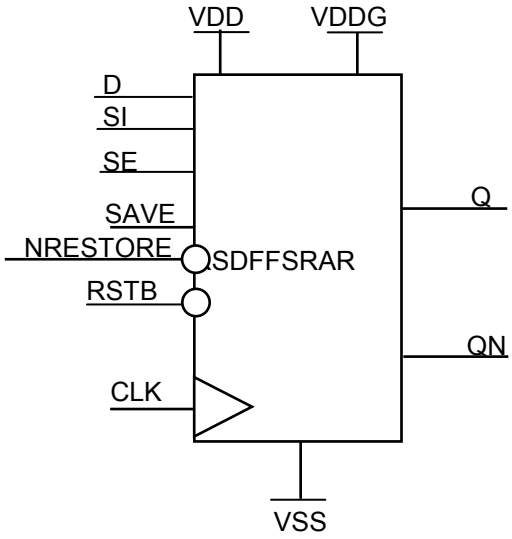


Figure 10.101. Logic Symbol of Scan Pos Edge DFF SR, w/ Async Low-Active Reset

Table 10.201. Scan Pos Edge DFF SR, w/ Async Low-Active Reset Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Q2[n]	0	1	RSTB mode
0	X	0	0	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	Fall	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	0	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1		1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	Rise	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	Rise	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	0	Q2[n]	Q[n]	QN[n]	

Table 10.202. Scan Pos Edge DFF SR, w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFSRARX1	1 x Csl	QN	399	938	26428	82.0224
RSDFFSRARX2	2 x Csl	QN	423	1214	48898	88.4736

10.90. Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset

RSDFFSRASRX1, RSDFFSRASRX2

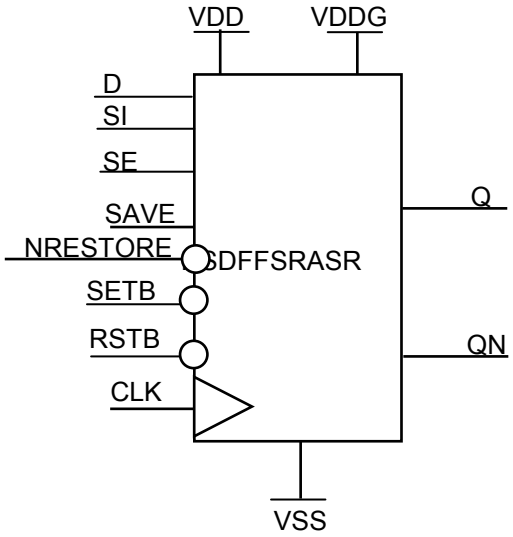


Figure 10.102. Logic Symbol of Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset

Table 10.203. Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	X	Q2[n]	0	1	RSTB mode
X	X	X	0	X	1	0	X	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	1	Fall	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	1	0	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	1	1	1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	1	Rise	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	1	Rise	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	0	Q2[n]	Q[n]	QN[n]	

Table 10.204. Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFSRASRX1	1 x Csl	QN	447	202254	22270	89.3952
RSDFFSRASRX2	2 x Csl	QN	468	1107	43036	96.768

10.91. Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset

RSDFFSRSSRX1, RSDFFSRSSRX2

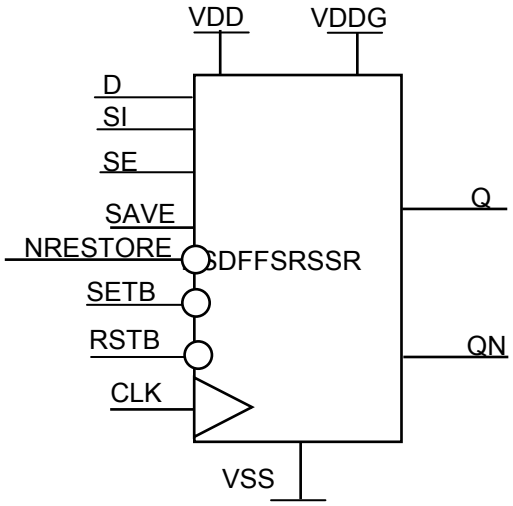


Figure 10.103. Logic Symbol of Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset

Table 10.205. Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Rise	Q2[n]	0	1	RSTB mode
X	X	X	0	X	1	0	Rise	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	X	X	Fall	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	X	X	0	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	X	X	1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	1	Rise	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	1	Rise	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	0	Q2[n]	Q[n]	QN[n]	

Table 10.206. Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFSRSSRX1	1 x Csl	QN	346	25141	40306	86.6304
RSDFFSRSSRX2	2 x Csl	QN	421	25358	6975	91.2384

10.92. Scan Neg Edge DFF SR

RSDFFNSRX1, RSDFFNSRX2

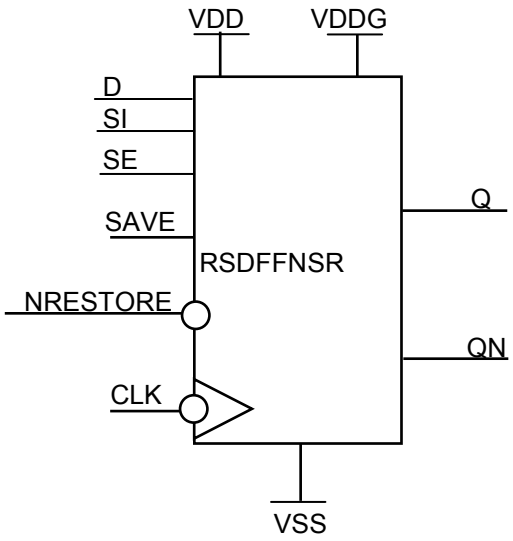


Figure 10.104. Logic Symbol of Scan Neg Edge DFF SR

Table 10.207. Scan Neg Edge DFF SR Transition Table

D	SI	SE	SAVE	NRESTORE	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	0	0	1	Fall	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	Fall	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	Rise	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	0	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	Fall	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	Fall	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	Q2[n]	Q[n]	QN[n]	

Table 10.208. Scan Neg Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRX1	1 x Csl	QN	394	891	566	79.2576
RSDFFNSRX2	2 x Csl	QN	408	1163	960	80.1792

10.93. Scan Neg Edge DFF SR, w/ Async Low-Active Set

RSDFFNSRASX1, RSDFFNSRASX2

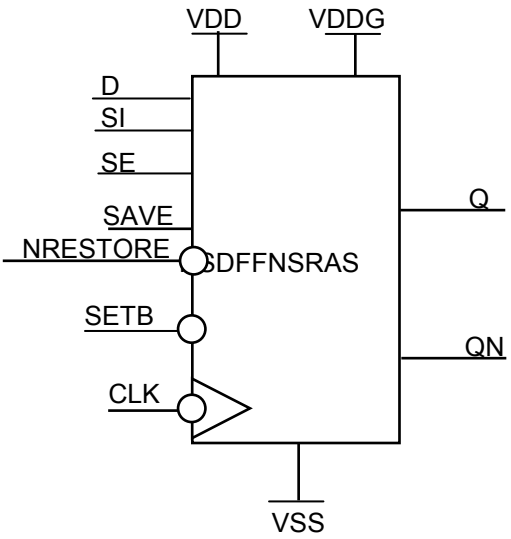


Figure 10.105. Logic Symbol of Scan Neg Edge DFF SR, w/ Async Low-Active Set

Table 10.209. Scan Neg Edge DFF SR, w/ Async Low-Active Set Transition Table

D	SI	SE	SAVE	NRESTORE	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	Fall	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	Fall	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	Rise	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	1	0	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	Fall	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	Fall	Q2[n]	1	0	Scan mode write 1
X	X	X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	Q2[n]	Q[n]	QN[n]	

Table 10.210. Scan Neg Edge DFF SR, w/ Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRASX1	1 x Csl	QN	429	971	639	89.3952
RSDFFNSRASX2	2 x Csl	QN	375	1254	698	94.0032

10.94. Scan Neg Edge DFF SR, w/ Async Low-Active Reset

RSDFFNSRARX1, RSDFFNSRARX2

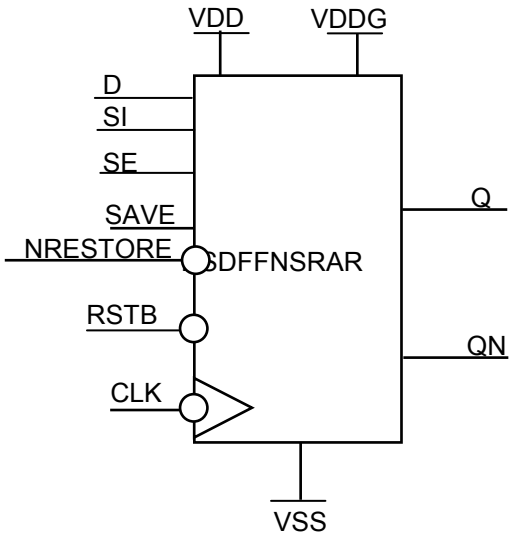


Figure 10.106. Logic Symbol of Scan Pos Edge DFF SR, w/ Async Low-Active Reset

Table 10.211. Scan Pos Edge DFF SR, w/ Async Low-Active Reset Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Q2[n]	0	1	RSTB mode
0	X	0	0	1	1	Fall	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	Fall	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	Rise	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	1	0	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	Fall	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	Fall	Q2[n]	1	0	Scan mode write 1
X	X	X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	Q2[n]	Q[n]	QN[n]	

Table 10.212. Scan Pos Edge DFF SR, w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRARX1	1 x Csl	QN	415	934	28703	82.0224
RSDFFNSRARX2	2 x Csl	QN	421	1167	52380	847872

10.95. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset

RSDFFNSRASRX1, RSDFFNSRASRX2

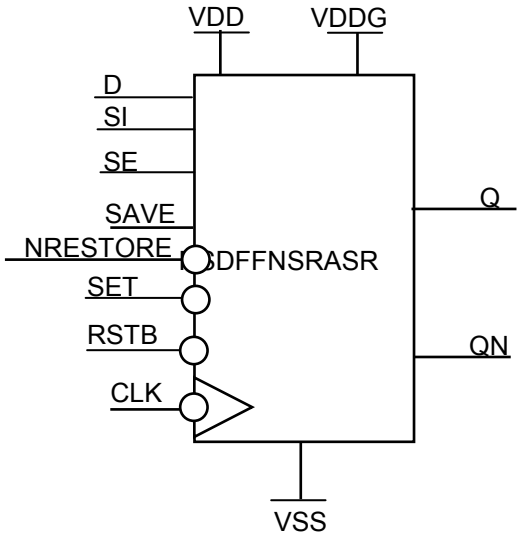


Figure 10.107. Logic Symbol of Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset

Table 10.213. Scan Neg Edge DFF SR, w/ Async Low-Active Set and Reset Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	X	Q2[n]	0	1	RSTB mode
X	X	X	0	X	1	0	X	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	1	Fall	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	1	Fall	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	1	Rise	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	1	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	1	1	0	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	1	Fall	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	1	Fall	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	1	Q2[n]	Q[n]	QN[n]	

Table 10.214. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRASRX1	1 x Csl	QN	458	1018	30111	89.3952
RSDFFNSRASRX2	2 x Csl	QN	468	1370	35916	94.0032

10.96. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out

RSDFFNSRASRQX1, RSDFFNSRASRQX2

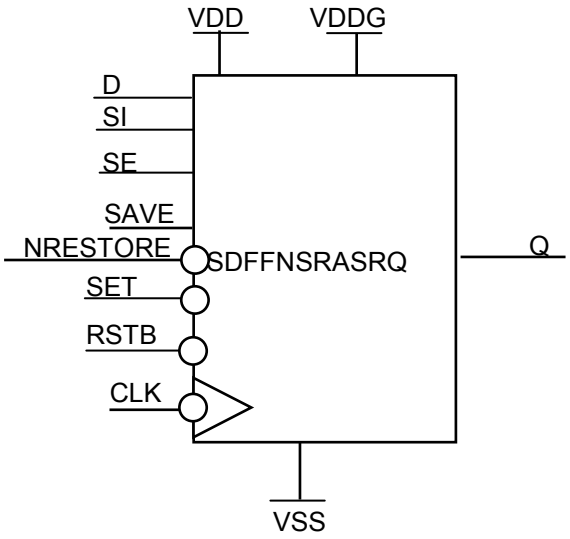


Figure 10.108. Logic Symbol of Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out

Table 10.215. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	SETB	CLK	Q2[n+1]	Q[n+1]	Mode
X	X	X	0	X	0	X	X	Q2[n]	0	RSTB mode
X	X	X	0	X	1	0	X	Q2[n]	1	SETB mode
0	X	0	0	1	1	1	Fall	Q2[n]	0	Normal mode write 0
1	X	0	0	1	1	1	Fall	Q2[n]	1	Normal mode write 1
X	X	X	0	X	1	1	Rise	Q2[n]	Q[n]	
X	X	X	0	X	1	1	1	Q2[n]	Q[n]	
X	X	X	0	1	1	1	0	Q2[n]	Q[n]	
X	0	1	0	1	1	1	Fall	Q2[n]	0	Scan mode write 0
X	1	1	0	1	1	1	Fall	Q2[n]	1	Scan mmode write 1
X	X	X	1	X	X	X	X	Q[n]	Q[n]	Save mode
X	X	X	0	0	1	1	0	Q2[n]	Q2[n]	Restore mode
X	X	X	0	0	1	1	1	Q2[n]	Q[n]	

Table 10.216. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRASRQX1	1 x Csl	Q	219	1035	39351	89.3952
RSDFFNSRASRQX2	2 x Csl	Q	268	1290	75483	94.0032

10.97. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out

RSDFFNSRASRNX1, RSDFFNSRASRNX2

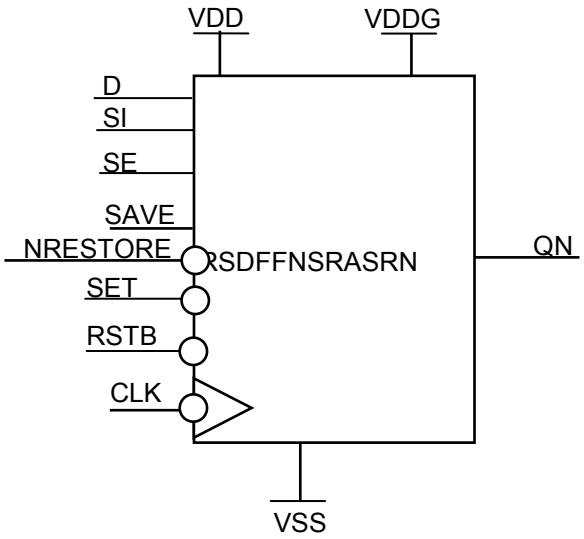


Figure 10.109. Logic Symbol of Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out

Table 10.217. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	SETB	CLK	Q2[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	X	Q2[n]	1	RSTB mode
X	X	X	0	X	1	0	X	Q2[n]	0	SETB mode
0	X	0	0	1	1	1	Fall	Q2[n]	1	Normal mode write 0
1	X	0	0	1	1	1	Fall	Q2[n]	0	Normal mode write 1
X	X	X	0	X	1	1	Rise	Q2[n]	QN[n]	
X	X	X	0	X	1	1	1	Q2[n]	QN[n]	
X	X	X	0	1	1	1	0	Q2[n]	QN[n]	
X	0	1	0	1	1	1	Fall	Q2[n]	1	Scan mode write 0
X	1	1	0	1	1	1	Fall	Q2[n]	0	Scan mmode write 1
X	X	X	1	X	X	X	X	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	1	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	0	Q2[n]	QN[n]	

Table 10.218. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRASRNX1	1 x Csl	QN	450	857	26299	84.7872
RSDFFNSRASRNX2	2 x Csl	QN	471	1010	51815	84.7872

10.98. Header Cell

HEADX2, HEADX4, HEADX8, HEADX16, HEADX32

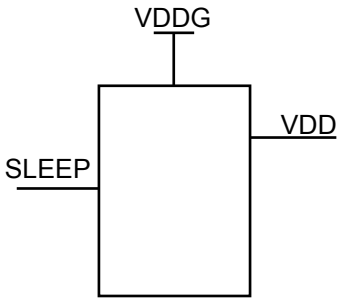


Figure 10.110. Logic Symbol of Header Cell

Table 10.219. Header Cell Truth Table

SLEEP	VDDG	VDD	SLEEPQ
0	1	1	0
1	1	hi-z	1

Table 10.220. Header Cell Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
HEADX2	2 x Csl	-	0.05	5462	27.6480
HEADX4	4 x Csl	-	0.1	11010	33.1776
HEADX8	8 x Csl	-	0.2	22502	44.2368
HEADX16	16 x Csl	-	0.4	44477	66.3552
HEADX32	32 x Csl	-	0.9	89769	112.4352

10.99. Header Cell (with SLEEPOUT output)

HEAD2X2, HEAD2X4, HEAD2X8, HEAD2X16, HEAD2X32

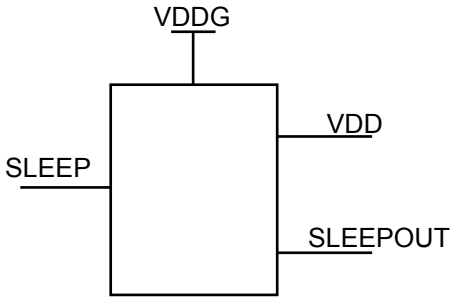


Figure 10.111. Logic Symbol of Header Cell(with SLEEPOUT output

Table 10.221. Header Cell (with SLEEPOUT output) Truth Table

SLEEP	VDDG	VDD	SLEEPOUT
0	1	1	0
1	1	hi-z	1

Table 10.222. Header Cell Electrical Parameters and Areas(with SLEEPOUT output)

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
HEAD2X2	2 x Csl	179	107	1011	27.6480
HEAD2X4	4 x Csl	250	209	2351	33.1776
HEAD2X8	8 x Csl	366	416	5146	44.2368
HEAD2X16	16x Csl	513	831	88288	66.3552
HEAD2X32	32 x Csl	892	1667	510057	112.4352

10.100. Always on Inverter

AOINVX1, AOINVX2, AOINVX4

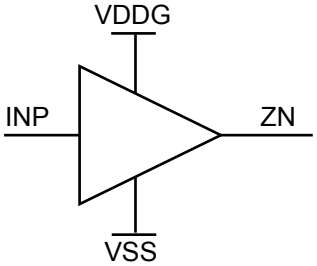


Figure 10.112. Logic Symbol of Always on Inverter

Table 10.223. Always on Inverter Truth Table

IN	VDDG	VSS	Q
0	1	0	1
1	1	0	0

Table 10.224. Always on Inverter Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOINVX1	1 x Csl	161	22	19	22.1184
AOINVX2	2 x Csl	152	52	17	22.1184
AOINVX4	4 x Csl	99	209	4	18.432

10.101. Always on Non-inverting Buffer

AOBUFX1, AOBUFX2, AOBUFX4

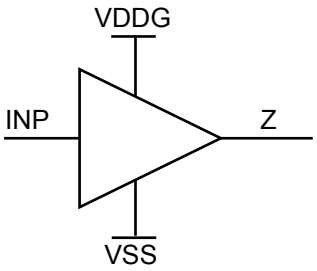


Figure 10.113. Logic Symbol of Always on Non-inverting Buffer

Table 10.225. Always on Non-inverting Buffer Truth Table

IN	VDDG	VSS	Q
0	1	0	0
1	1	0	1

Table 10.226. Always on Non-inverting Buffer Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOBUFX1	1 x Csl	142	55	173	22.1184
AOBUFX2	2 x Csl	187	108	644	22.1184
AOBUFX4	4 x Csl	242	200	1395	27.6480

10.102. Always on Pos Edge DFF, w/ Async Low-Active Reset

AODFFARX1, AODFFARX2

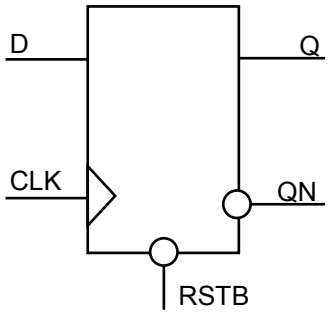


Figure 10.114. Logic Symbol of Always on Pos Edge DFF, w/ Async Low-Active Reset

Table 10.227. Always on Pos Edge DFF, w/ Async Low-Active Reset Transition Table

RSTB	CLK	D	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	X	Q2[n]	0	1	RSTB mode
1	Rise	0	Q2[n]	0	1	Normal mode write 0
1	Rise	1	Q2[n]	1	0	Normal mode write 1
1	Fall	X	Q2[n]	Q[n]	QN[n]	
1	1	X	Q2[n]	Q[n]	QN[n]	
1	0	X	Q2[n]	Q[n]	QN[n]	

Table 10.228. Always on Pos Edge DFF, w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
AODFFARX1	1 x Csl	Q	173	164	4114	46.0800
		QN	337			
AODFFARX2	2 x Csl	Q	216	221	4503	49.7664
		QN	350			

10.103. Always on Neg Edge DFF, w/ Async Low-Active Reset

AODFFNARX1, AODFFNARX2

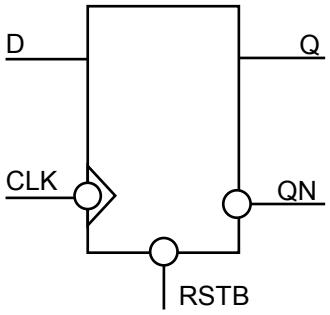


Figure 10.115. Logic Symbol of Always on Neg Edge DFF, w/ Async Low-Active Reset

Table 10.229. Always on Neg Edge DFF, w/ Async Low-Active Reset Transition Table

RSTB	CLK	D	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	X	Q2[n]	0	1	RSTB mode
1	Fall	0	Q2[n]	0	1	Normal mode write 0
1	Fall	1	Q2[n]	1	0	Normal mode write 1
1	Rise	X	Q2[n]	Q[n]	QN[n]	
1	1	X	Q2[n]	Q[n]	QN[n]	
1	0	X	Q2[n]	Q[n]	QN[n]	

Table 10.230. Always on Neg Edge DFF, w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
AODFFNARX1	1 x Csl	Q	174	176	6844	47.9232
		QN	343			
AODFFNARX2	2 x Csl	Q	210	228	6543	47.9232
		QN	227361			

10.104. Bus Keeper

BUSKP

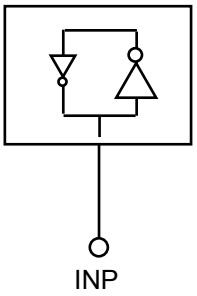


Figure 10.116. Logic Symbol of Bus Keeper

Table 10.231. Bus Keeper Truth Table

Z
1

10.105. P-MOSFET

PMT1, PMT2, PMT3

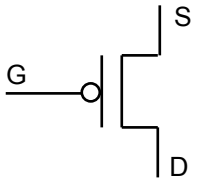


Figure 10.117. Logic Symbol of P-MOSFET

Table 10.232. P-MOSFET Truth Table

Z
1

10.106. N-MOSFET

NMT1, NMT2, NMT3

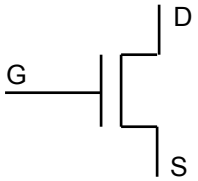


Figure 10.118. Logic Symbol of N-MOSFET

Table 10.233. N-MOSFET Truth Table

Z
1

10.107. Tie High

TIEH

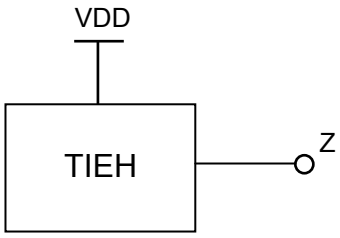


Figure 10.119. Logic Symbol of Tie High

Table 10.234. Tie High Truth Table

Z
1

10.108. Tie Low

TIEL

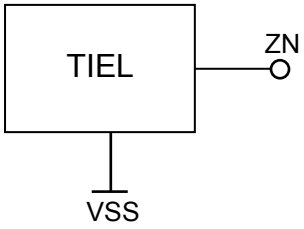


Figure 10.120. Logic Symbol of Tie Low

Table 10.235. Tie Low Truth Table

ZN
0

10.109. Antenna Diode

ANTENNA

Figure 10.121. Logic Symbol of Antenna Diode

Table 10.236. Antenna Diode Truth Table

INP
*

10.110. Decoupling Capacitance

DCAP

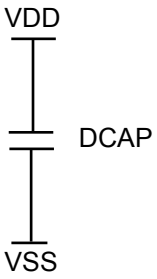


Figure 10.122. Logic Symbol of DCAP Decoupling Capacitance

10.111. Capacitive Load

CLOAD1

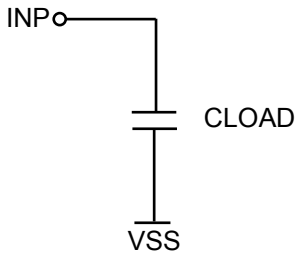


Figure 10.123. Logic Symbol of Capasitive Load

11. Revision history

Table 11.1. Revision history

Revision	Date	Change
A.1	06/01/2007	Initial release
A1.1	06/11/2007	– Capacitive Load cell has been added – Filler cells have been updated – Physical structure of double height (high-low-high) digital standard cells (for Level-Shifter cells: Low-High) has been updated – Symbols have been updated – Electrical parameters and areas of cells have been updated
A1.2	06/06/2008	– Inverting Buffer cells have been updated – Scan Latches cells have been removed – Async cells in Retention Flip-Flops and scan Flip-Flops cells have been removed – Digital Standard Cell Library deliverables have been updated
A.1.3	11/12/2008	– The following cells have been added: Low to High Level Shifters/ Active Low Enable, High to Low Level Shifters/ Active Low Enable – 2 new corners have been added for characterization
A.1.4	27/12/2008	– The table of characterization corners has been updated – The table of characterization corners for Low to High Level Shifters has been removed
A.1.5	27/05/2009	– High-VT cells added
A.1.6	11/07/2009	– Low-VT cells added – 3 grid width single height filler cell (SHFILL3) added – Symbols for TIEH and TIEL have been updated
A.1.7	30/10/2009	– Header cells with SLEEPOUT pin added (HEAD2X*)
A.1.8	28/11/2009	– 1 grid width single height filler cell (SHFILL1) added – 64 grid width single height filler cell (SHFILL64) added – 128 grid width single height filler cell (SHFILL128) added
A.1.9		– Added clamp low level shifter cells – Added retention cells with SAVE and NRESTORE pins
A.1.10	30/09/2010	– Added hold 0 Isolation cells (logic AND),always on – Added hold 1 Isolation cells (logic OR), always on – Added high to low level shifter/single supply cells – Added high to low level shifter/high-active enable,single supply cells – Added high to low level shifter/high-active enable, clamp low, single supply cells – Added scan neg edge retention DFF,with asyncron low-active reset cells

		– Added pos edge retention DFF, with asyncron low-active reset cells – Added neg edge retention DFF, with asyncron low-active reset cells
A.1.11	24/01/2011	– Added file naming conventions – Updated ISOLANDAO* cell truth table – Updated ISOLORAO* cell truth table