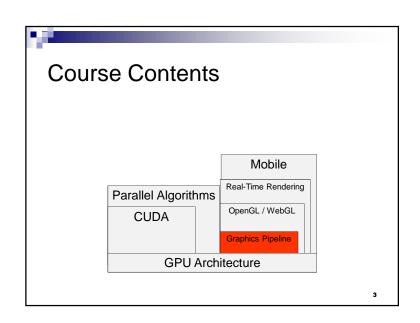
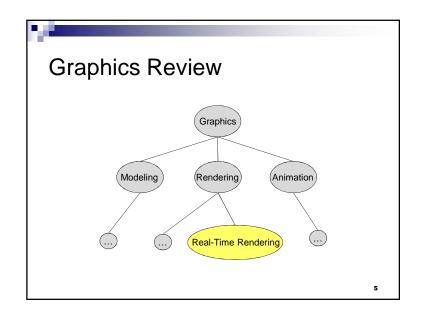


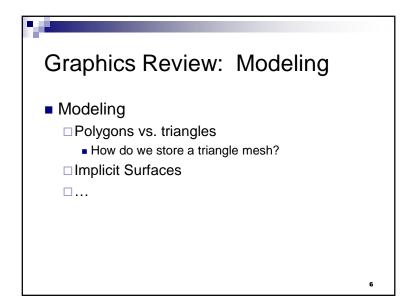
Announcements 10/29 – Eric Lengyel Game Engine Architecture Guest Lecture 10/30 – Class in SIG lab Instead of class on 10/31

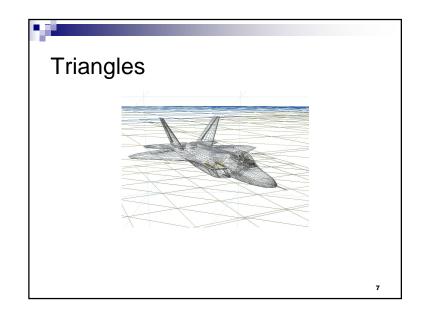


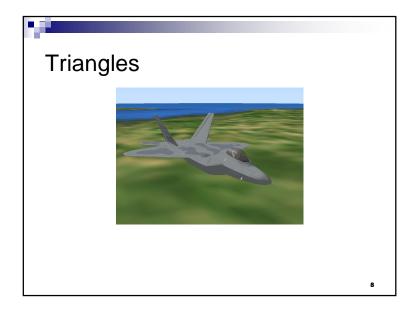
Agenda

Brief Graphics Review
Graphics Pipeline
Mapping the Graphics Pipeline to Hardware

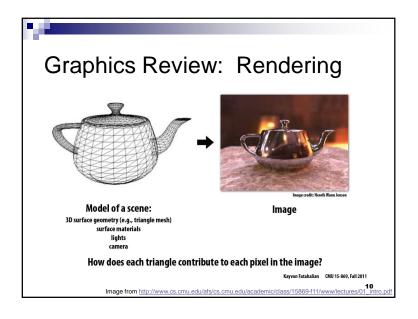


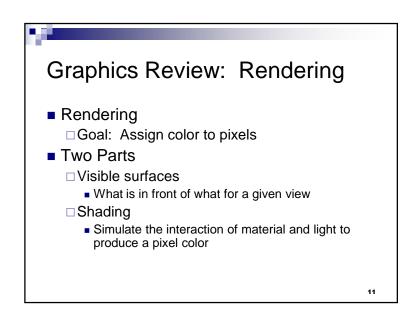








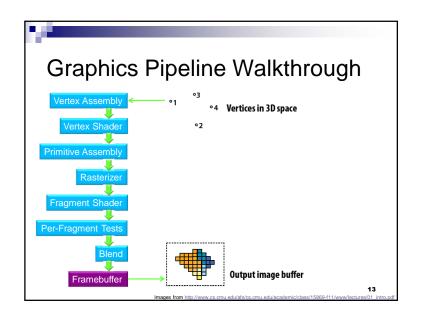


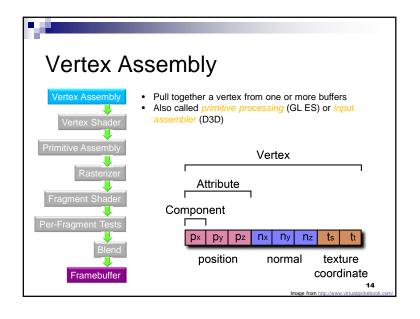


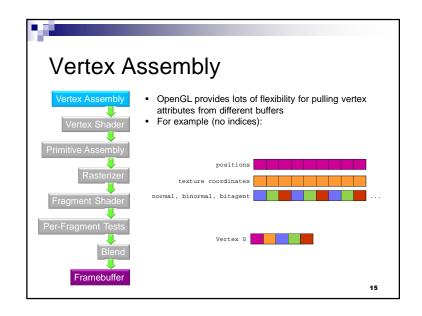
Graphics Review: Animation

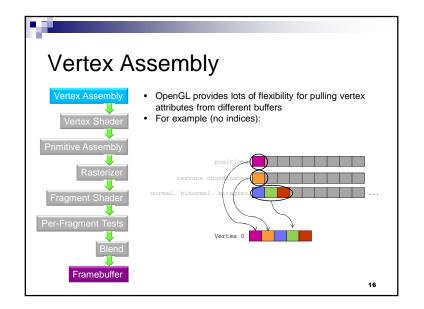
• Move the camera and/or agents, and rerender the scene

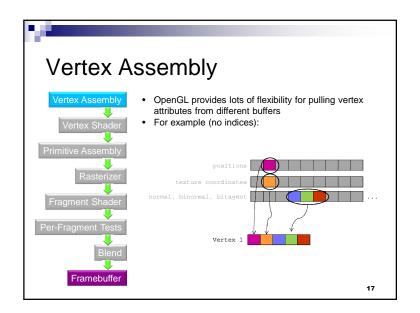
□ In less than 16.6 ms (60 fps)

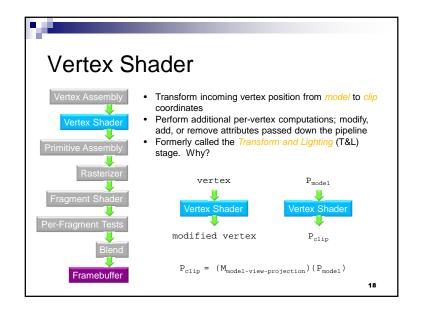


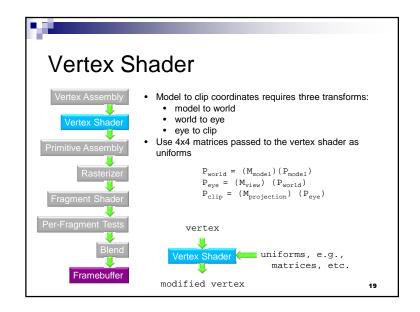


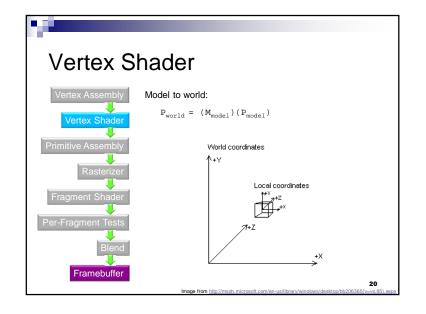


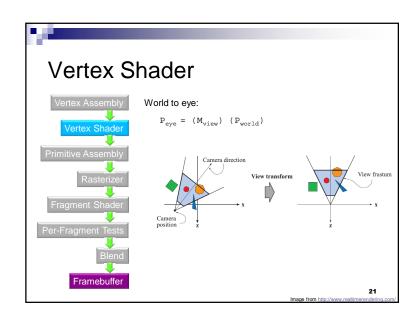


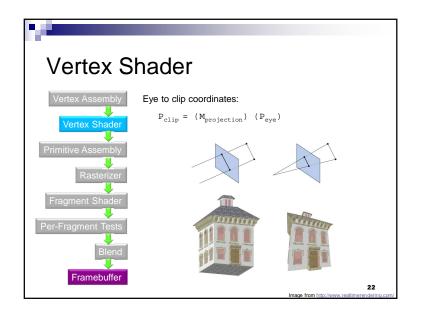


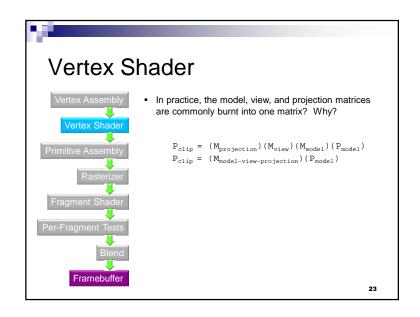


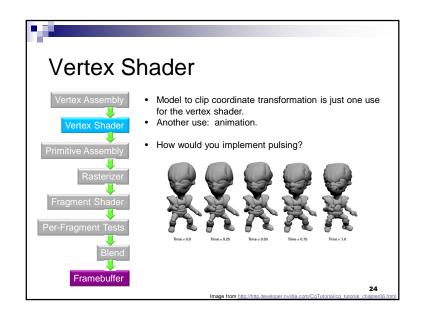


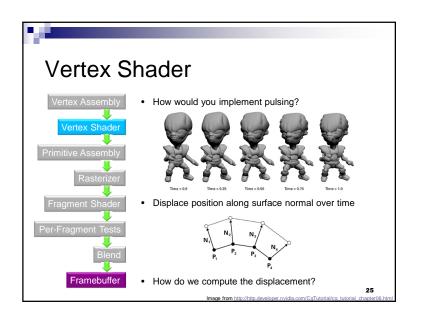


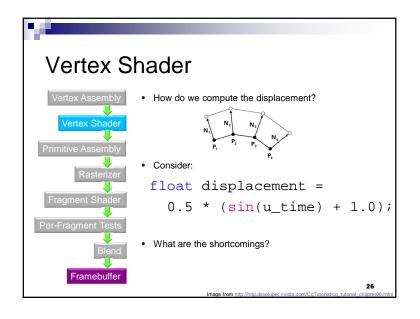


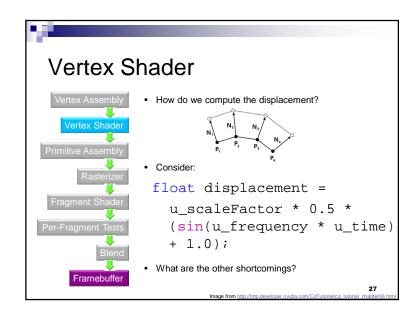


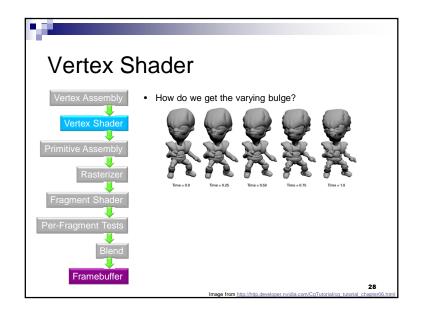


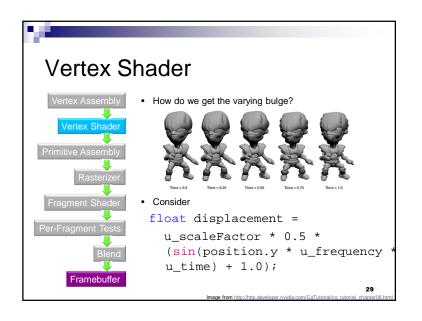


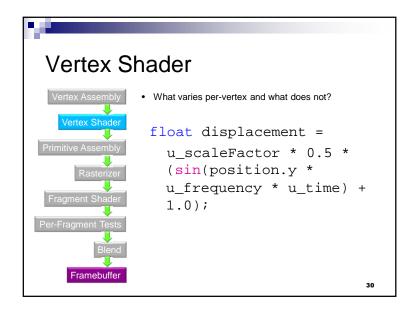


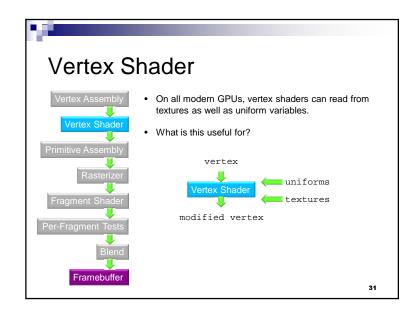


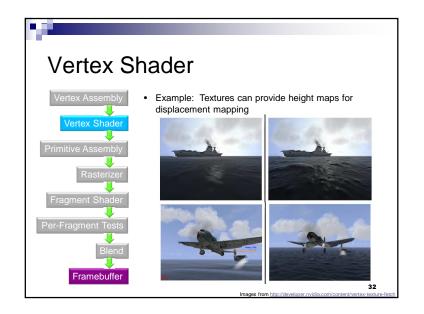


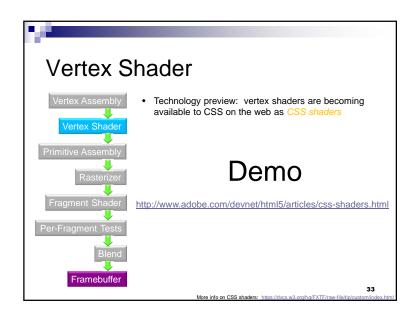


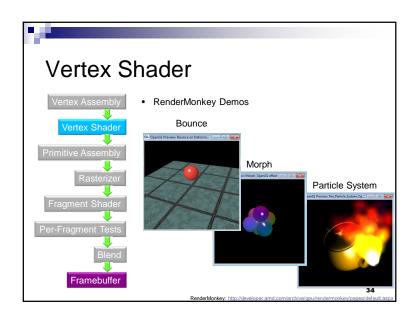


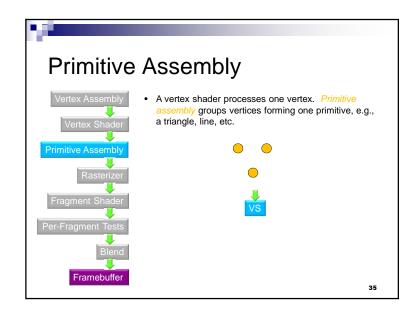


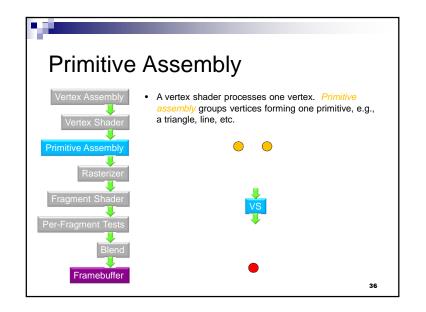


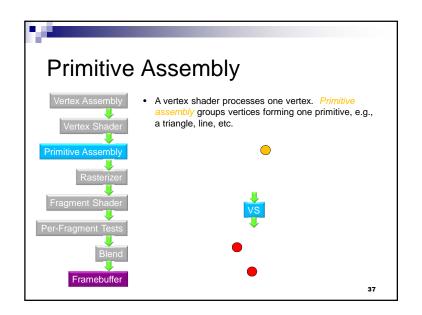


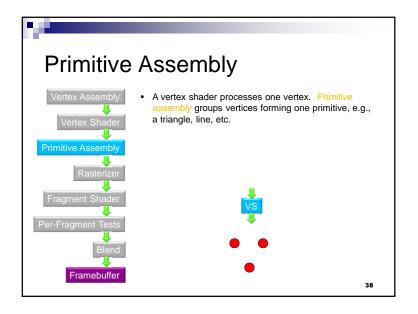


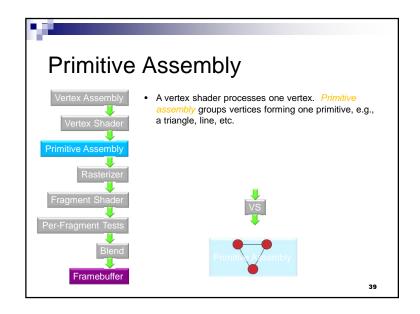


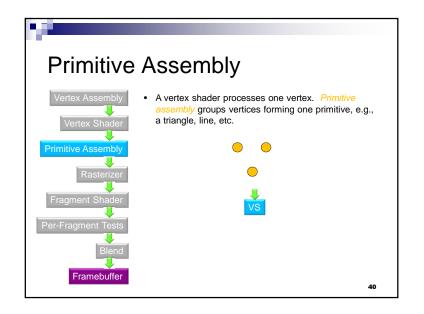


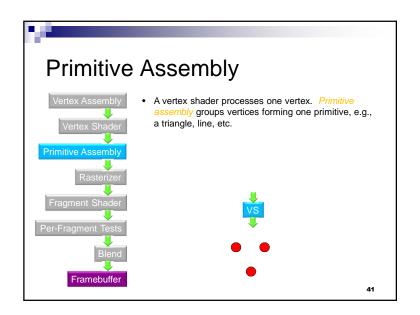


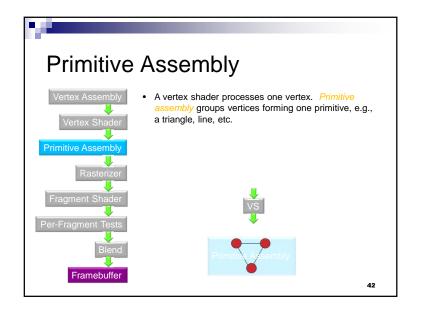


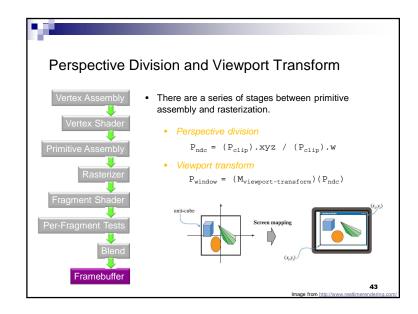


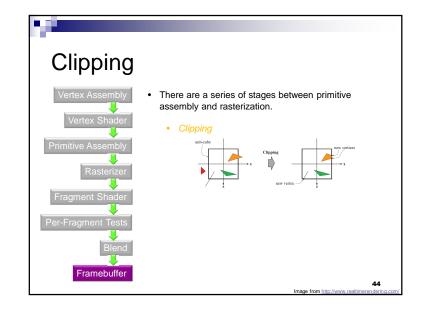


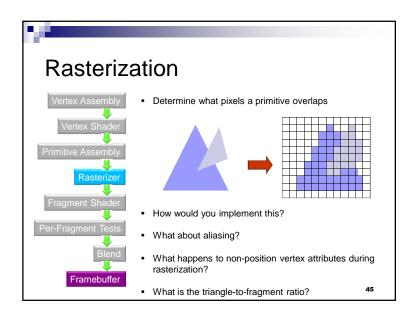


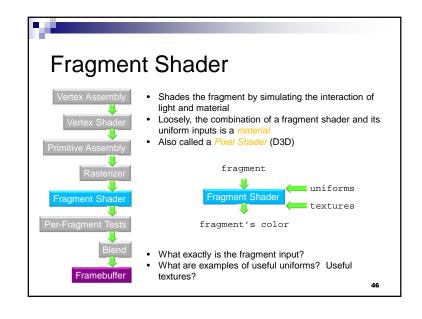


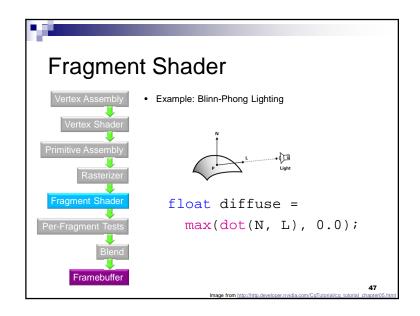


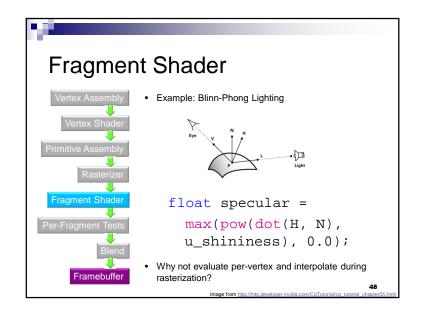


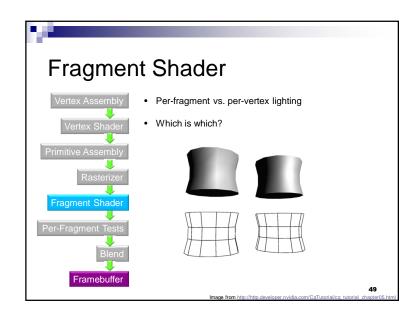


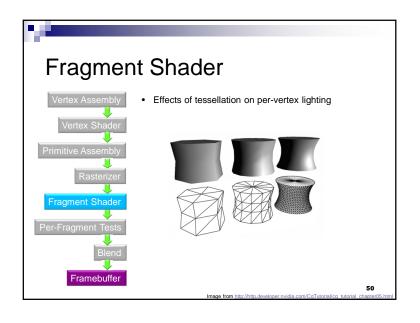


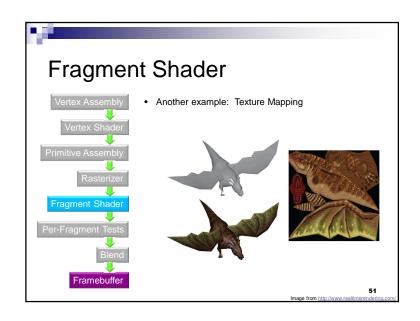


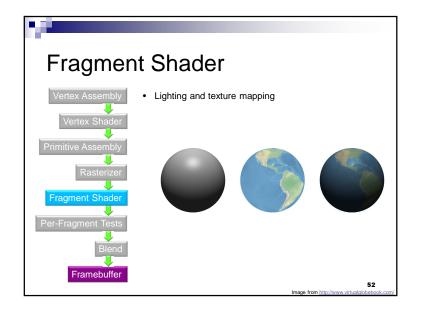


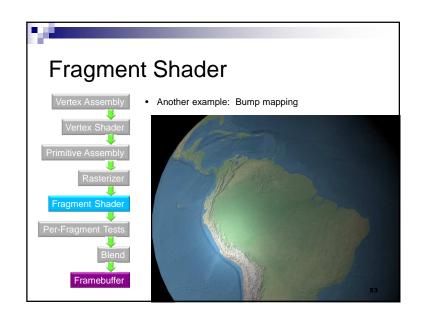


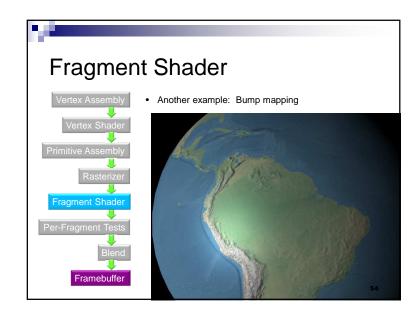


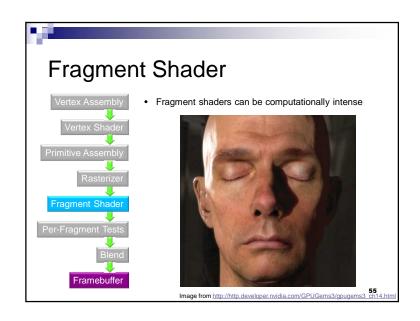


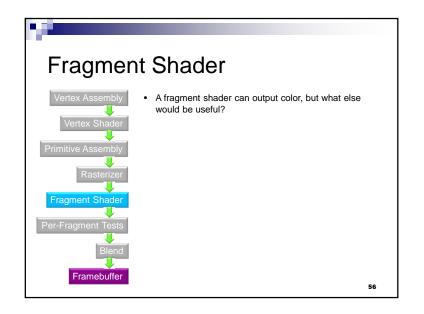


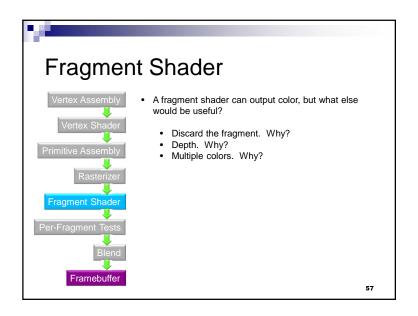


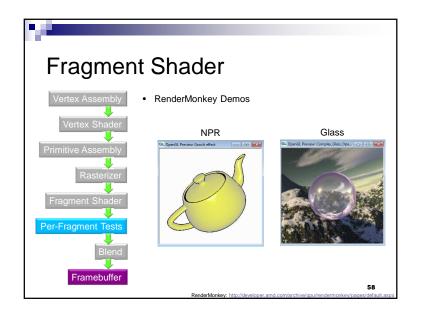


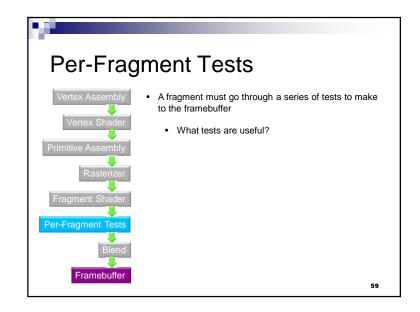


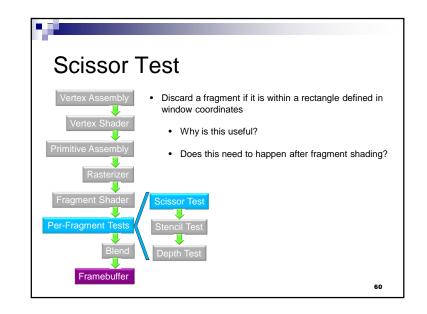


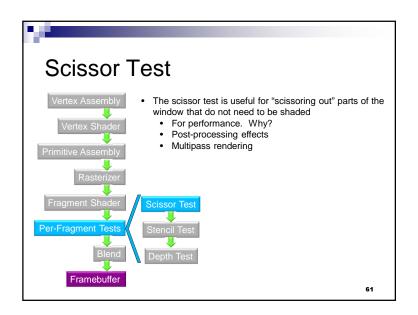


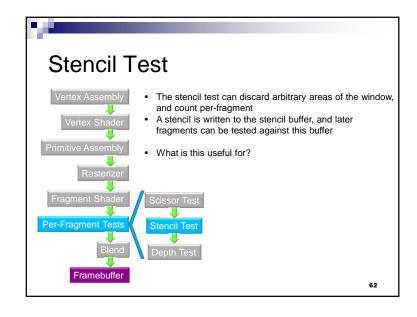


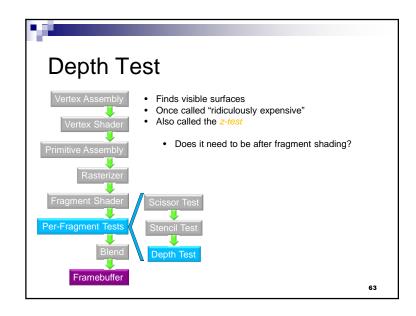


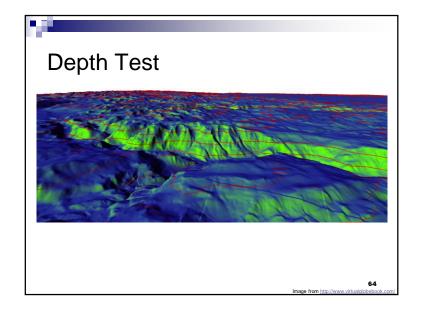


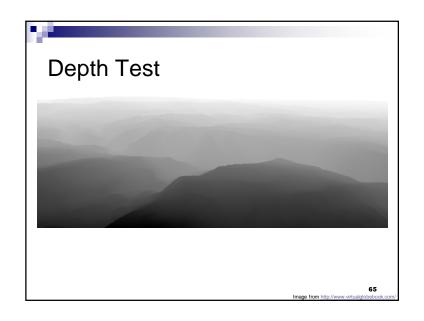


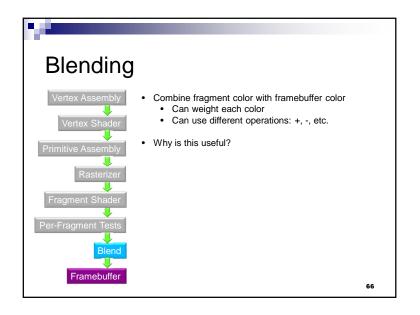


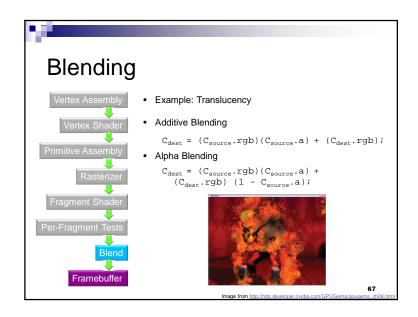


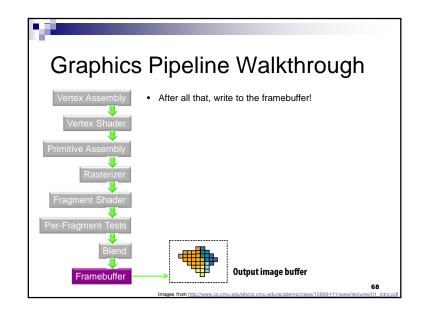








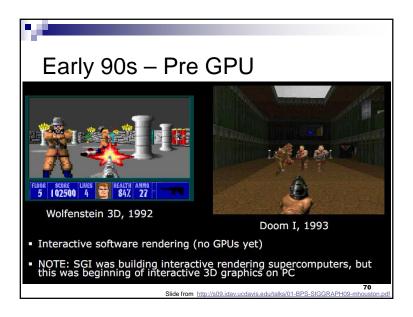




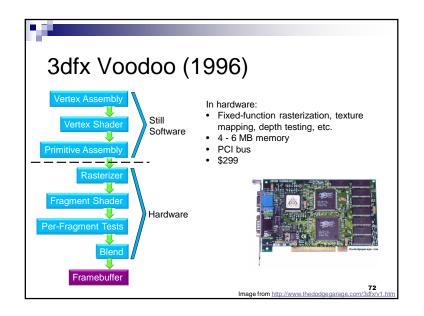
Evolution of the Programmable Graphics Pipeline

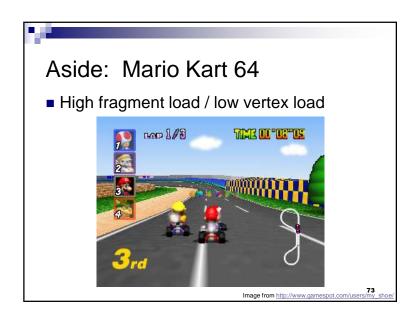
- Pre GPU
- Fixed function GPU
- Programmable GPU
- Unified Shader Processors

69

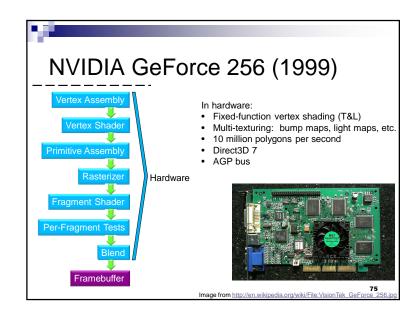


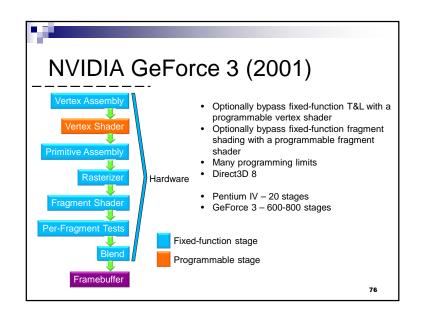
Why GPUs? Exploit Parallelism Pipeline parallel Data-parallel CPU and GPU executing in parallel Hardware: texture filtering, rasterization, MAD, sqrt, etc.

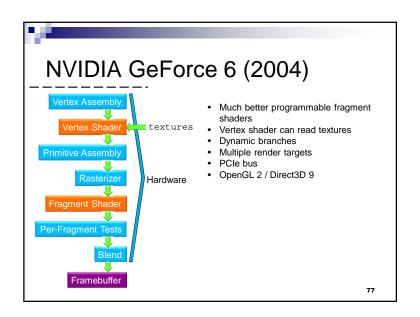


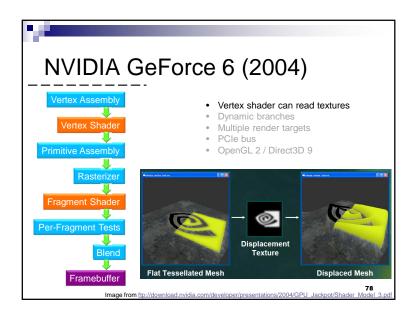


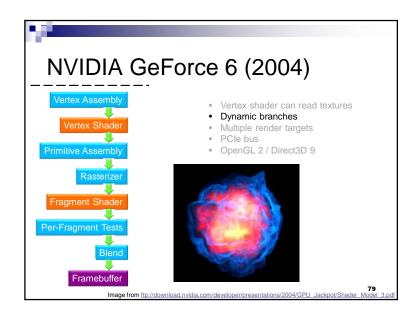


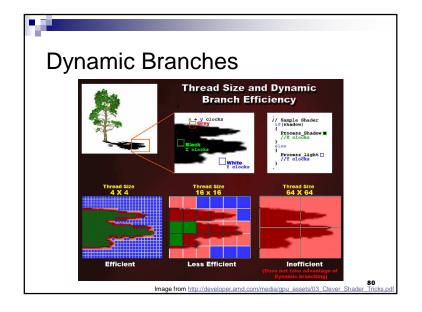


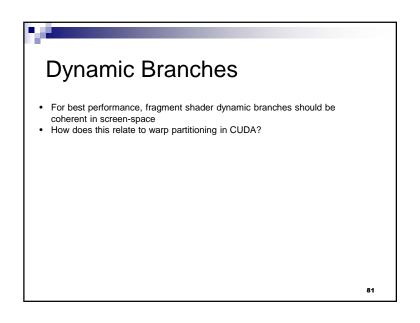


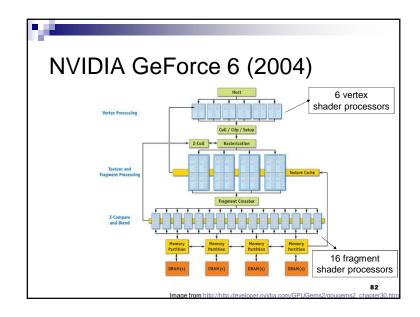


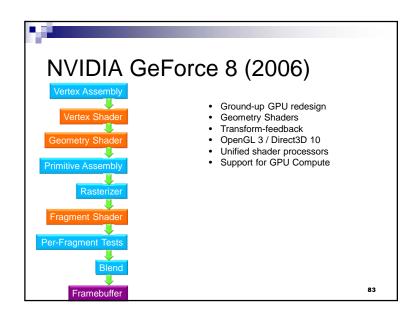


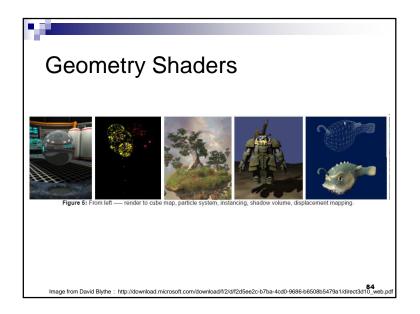


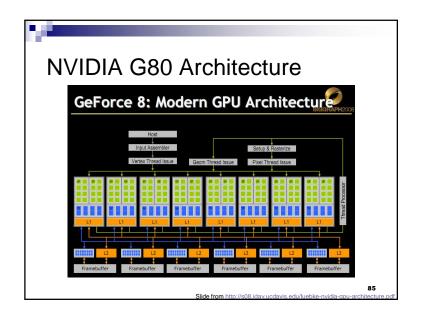


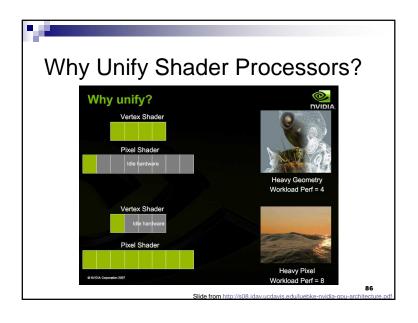


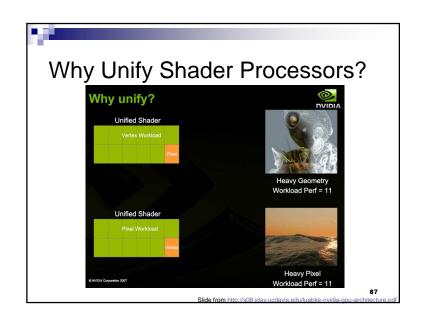


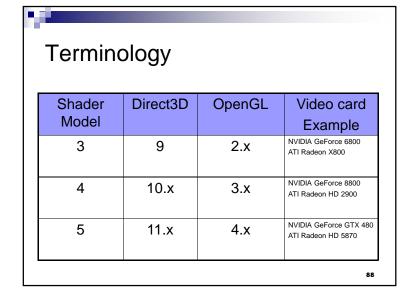












Shader Capabilities SM 2.0/2.XSM 3.0SM 4.0Introduced DX 9.0c, 2004 DX 10, 2007 DX 9.0, 2002 VS Instruction Slots 256 $> 512^{a}$ 4096 65536 VS Max. Steps Executed 65536 ∞ PS Instruction Slots > 96 ≥ 512° $> 65536^{a}$ PS Max. Steps Executed $> 96^{6}$ 65536 ∞ $\geq 12^a$ Temp. Registers 32 4096 > 256VS Constant Registers $> 256^{\circ}$ $14 \times 4096^{\circ}$ PS Constant Registers 32 224 14×4096 Flow Control, Predication Optional dYes Yes VS Textures None 4^e $128 \times 512^{\,j}$ PS Textures 16 16 128×512^{f} Integer Support No No Yes VS Input Registers 16 16 16 89 $16/32^{h}$ Interpolator Registers 10 PS Output Registers

Table courtesy of A K Peters, Ltd. http://www.realtimerendering.com

Evolution of the Graphics Pipe	U	rammable	
Software Rendering Frame Buffer Pre 1996 Customized Software Rendering	Input Data Transformation and Lighting Primitive Setup Rasterization Pixel/Fragment Processing Frame Buffer Blend Frame Buffer Brame Buffer	Input Data Vertex Shading DX10 Geometry Shadiny Primitive Setup Prame Buffer Blend Frame Buffer Buffer DX10	
Slide from Mike Houston: http://s09.idav.ucdavis.edu/talks/01-BPS-SIGGRAPH09-mhouston.pdf			

