$$J = J_0 \left(e^{\frac{V_a - J(R_n + R_p)}{V_T}} - 1 \right)$$

$V_a - J(R_n+R_p)$ → Voltage drop across Quasi neutral region

Hard to Solve

Earlier ($V_a = 0.8$)

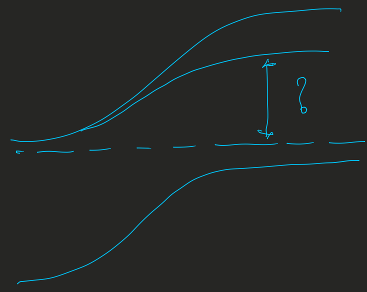
$\Delta n_p = 2.8 \times 10^{15}\ cm^{-3}$

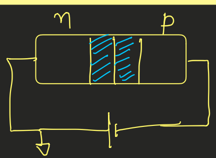
$E^p_{Fn} = 0.026 \ln\left(\frac{N_C}{n_p}\right)$

Quasi fermi level for e^- in p region

$= 0.026 \times \ln\left(\frac{2.8 \times 10^{19}}{2.8 \times 10^{15}}\right)$

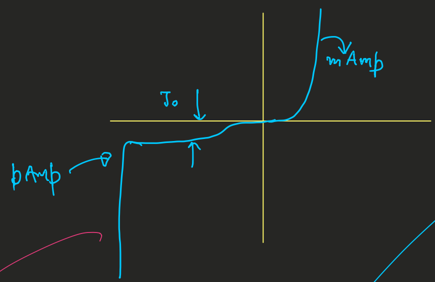
$= 0.026 \ln(10^4)$





(reverse Biased) → $J = J_0 (e^{V/V_T} - 1)$ V is large & -ve

$\approx -J_0$



Slope $\approx \frac{1}{R_n + R_p}$

as reverse Bias ↑; Depletion region gets wider

KE ↑ ; e^- Collides with Bound e^-

& it Can launch a Bound e^- & thus Create a $e^- - h^+$ pair

of the very very few free mobile Carriers

$1e^-$ generate $\to 1e^-$, $1h^+$

$\therefore 1e^- \longrightarrow 2e^-, 1h^+$

$2e^- + h^+$ → $2e^-$ $1h^+$, $2e^-$ $1h^+$

$2e^- + h^+$ → $2e^-$ $1h^+$, $2e^-$ $1h^+$

This effect is K/a **Avalanche effect**

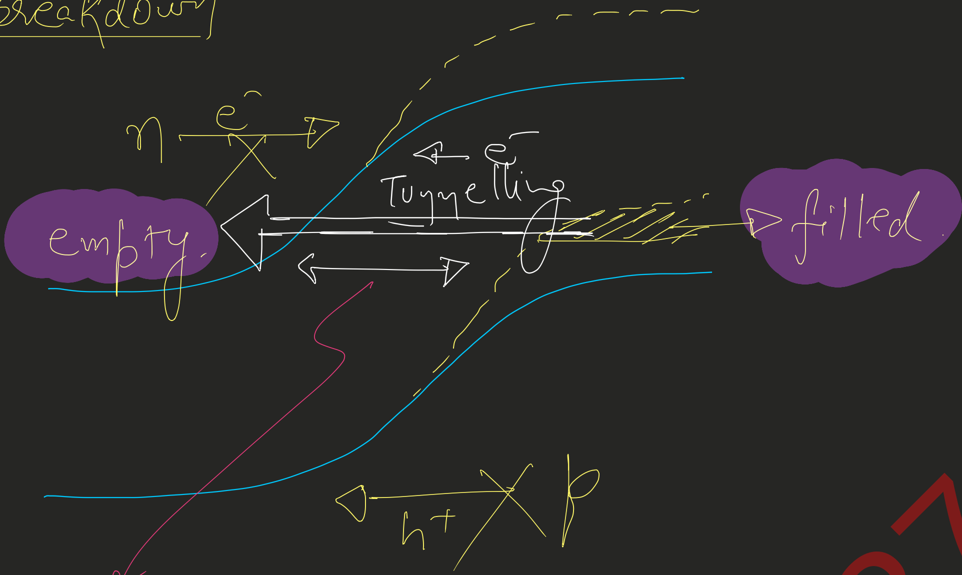
$\therefore$ Depletion region flooded with e^- & h^+ ⟹ huge Current {mostly ltd by resistance of p, n region}

* Each material has it's own E_{cr} → Critical Electric field

{larger bandgap → more the E_{crit}}

e^- $\frac{e^-}{h^+}$ $\Big\updownarrow E_g$

Zener Breakdown



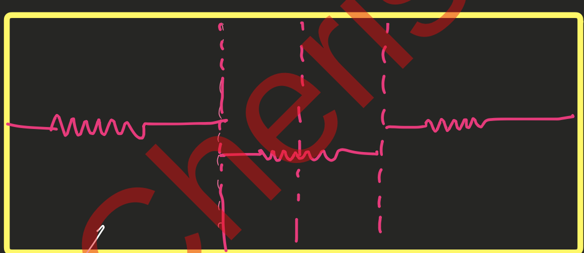
{Tunnelling dist should be small
width of depletion region ↓ ⟶ if doping density ↑ ⟹ Tunnelling prob ↑

(N_A/N_D ↑)

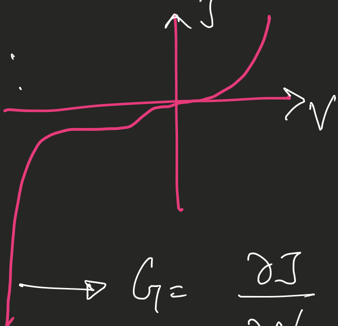
↓ generally happen at relatively lower bias

Hence Breakdown characteristic governed by
- ⟶ Avalanche (less doping density)
- ⟶ Zener (more doping density)

Diode



Sum of 3 Resistances.



$\longrightarrow G = \dfrac{\partial J}{\partial V}$

Conductance.

$R_{dyn} = \dfrac{\partial V}{\partial I}$

$G \to \infty$

$R \to$ Small

Avalanche Diode
↓
most sensitive Photo diode.

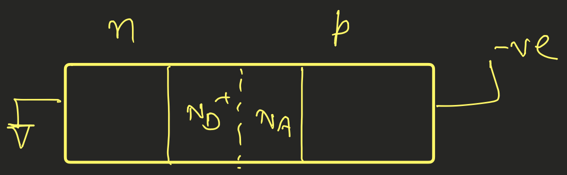
we just keep V_a on verge of Breakdown; & then we apply $h\nu$; even when 1 photon generated ⟶ it will get detected as it will initiate Avalanche

$\because$ Depletion region is due to lack of e^-/h^+. But in breakdown; free Carriers $\uparrow$
So they try to $\downarrow(W_n + W_p)$ but V_a tries to $\uparrow(W_n+W_p)$. Thus they Compete &
ultimately J gets Stabilized.

Capacitance

(for diode under Rev. bias)

1



$\equiv$

$$W \propto \sqrt{(V_{bi} + |V_a|)}$$

$$C_{dep} = \frac{dQ}{dV} = \left(\frac{\epsilon}{W_{dep}}\right) \text{ per-unit-area}$$

Temporary Capacitor

$\therefore$ Called as

Varactor Diode

$$\simeq V^{-n}$$

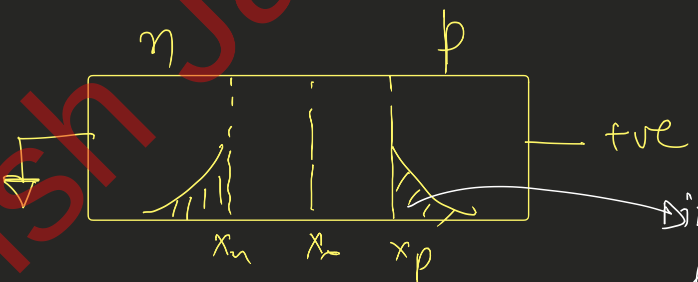
for ideal Cu; $W \propto V^{1/2}$

$n = 1/2$

$$\therefore \quad C \propto \frac{\epsilon A}{W} \propto V^{-1/2} \propto V^{-n}$$

2

in forward Bias



integrate this profile to get Charge here

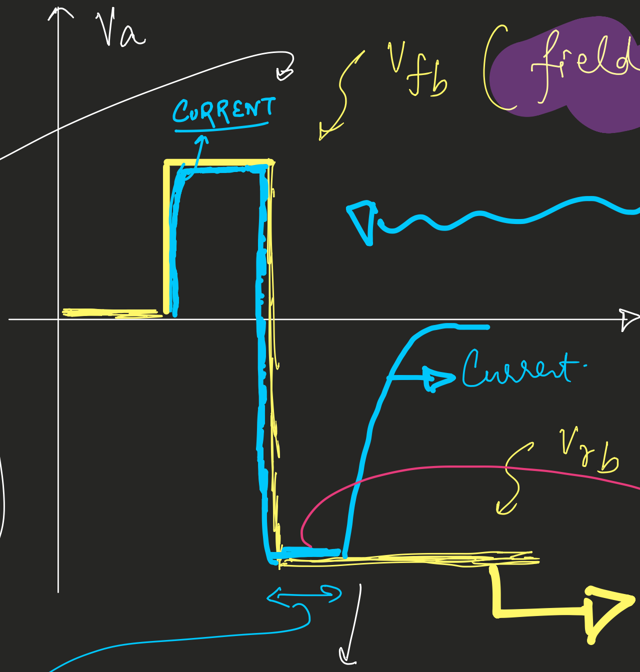
$$\Delta p_n = p_{n0}\left(e^{V/V_T} - 1\right)$$

$$Q_1 = \int_{x_p}^{\infty} \Delta n_p \, dx$$

$$Q_2 = \int_{-\infty}^{x_n} \Delta p_n \, dx$$

minority Charges on P & n Sides respectively

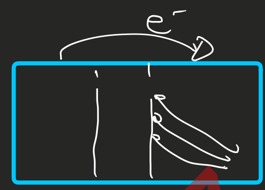
#



almost there inst. (very little delay)

V_{fb} (field set up instantaneously)

TURN ON TRANSIENT



this is the time when stored charges gets eliminated.

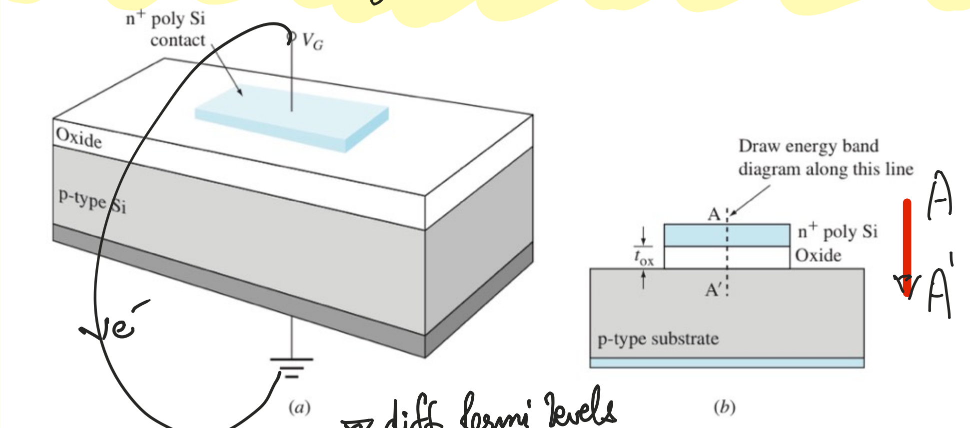
TURN OFF TRANSIENT.

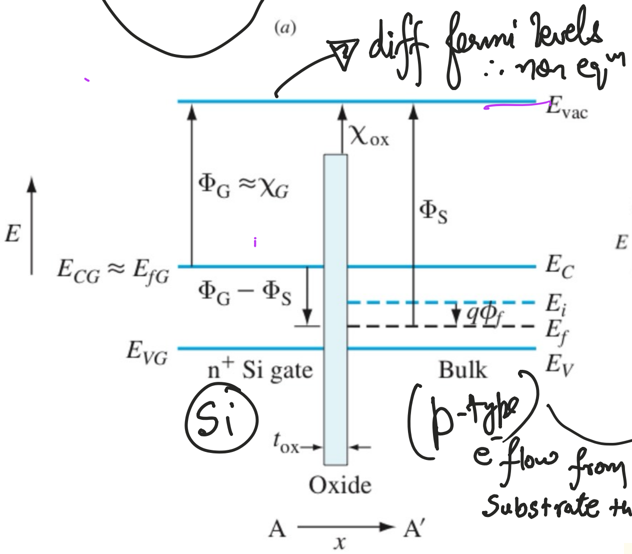
e^- & h^+ are dragged out

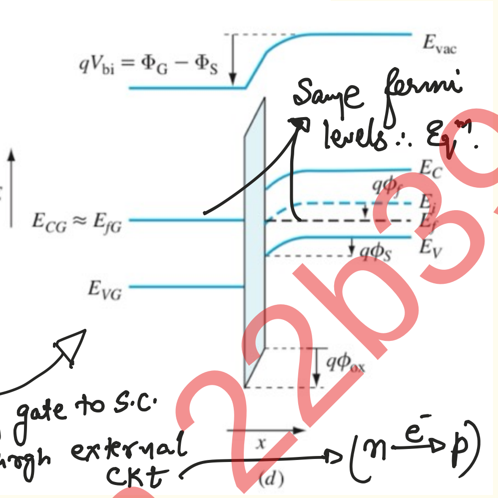
↳ as a large E.F. is set up due to reverse Biased

$$\left.\begin{aligned} e^- &: \; p \to n \\ h^+ &: \; n \to p. \end{aligned}\right\} \text{due to large EF}$$

General Mosfet Structure {p-type Substrate with n-type Silicon Gate}







ϕ_f :- $|V_{fermi} - V_{intrinsic}|$
ϕ_G :- V_{gate} / V_{metal}
ϕ_S :- $V_{semiconductor}$

Energy Band diagram with Charge Neutrality | Energy Band diagram at equilibrium → no Current flow.

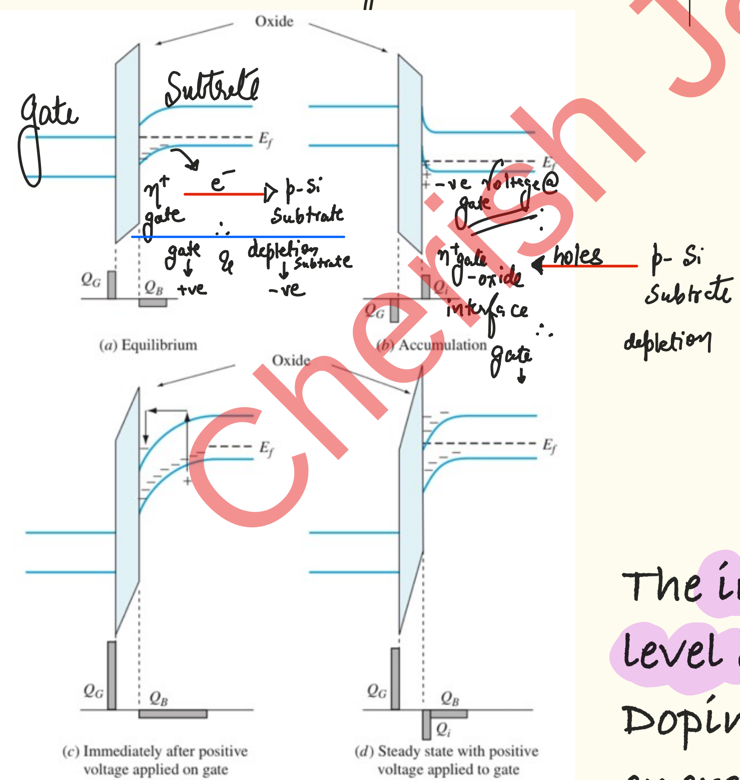
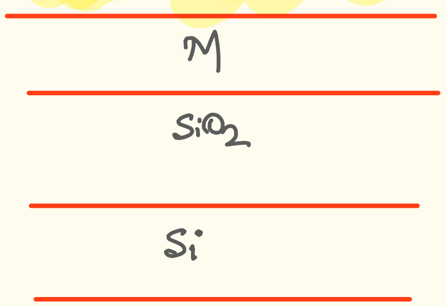


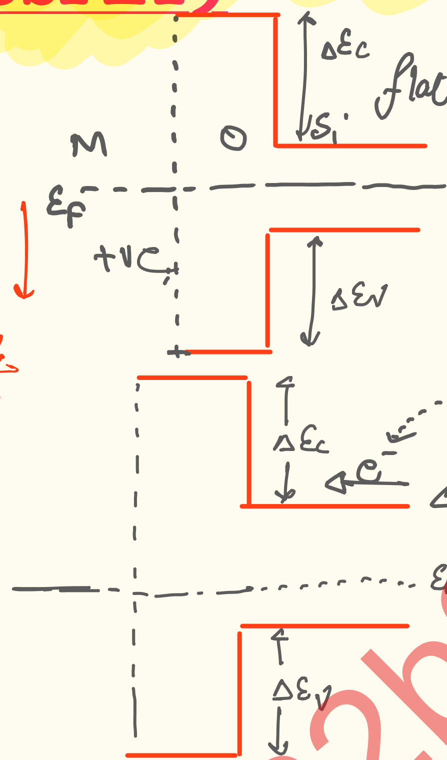
Figure 7.2 Energy band diagrams for the n^+-Si/oxide/p-Si capacitor of Figure 7.1 along with the charge distributions for three bias conditions. In (a) the case for equilibrium is indicated. Electrons from the n^+ gate transfer to the p-Si substrate, resulting in a positive gate and a negative depletion region in the substrate. The accumulation condition is indicated in (b). Here a negative voltage is applied to the gate with respect to the substrate such that holes accumulate at the silicon-to-oxide interface. The situation for a positive 2 V step voltage is shown in (c) immediately after the application of the voltage. With time, electrons generated in the transition region are trapped in the potential well at the interface until steady state is reach as indicated in (d).

Fermi level is sort of like the "sea level" of the Fermi sea which extends throughout the materials. Electrons flow when there is a difference in Fermi level between two different places, just like water flows when there is a difference in sea level. (disclaimer: limited analogy)

The intrinsic Fermi level is the Fermi level of an undoped semiconductor. Doping changes the distribution of energy states, thus the Fermi level depends on it and will generally not be the same as the intrinsic one.

Metal oxide semiconductor field effect transistor (MOSFET)





Flat Band Diagram

pulled down on applying +ve Bias

ΔE_c & ΔE_V = Const. Can't be changed

on apply +ve Bias

Silicon is p-type

On app +ve Bias; e^- L ← R

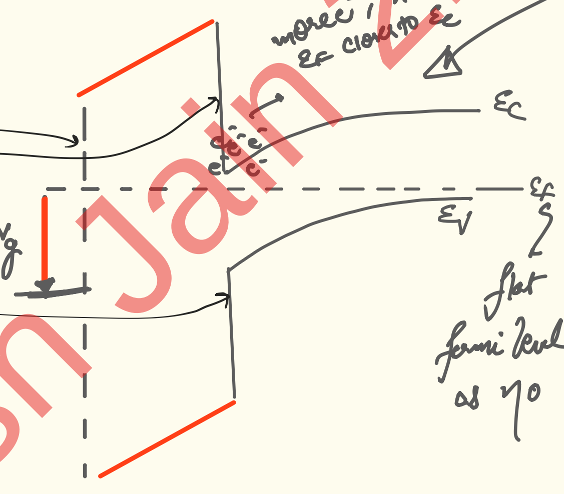
(Check Book) $\Delta E_c > \Delta E_V$.

$\Delta E_c + \Delta E_V \simeq 8 eV$

$\Delta E_c = 4.5 eV$

$\Delta E_V = 3.5 eV$

$\Delta E_c > \Delta E_V$



more e^-; hence E_F closer to E_c

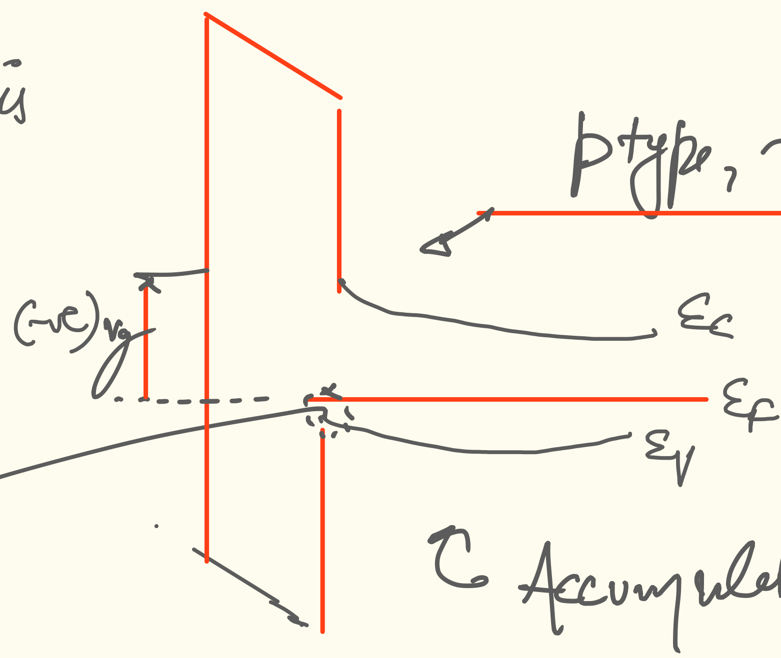
V_{GS} directly applied on left so more bend on left as Comp. to right. also e^- like to be near +ve V_{GS}

Hence if more e^- near this Surface then it means Conduction band near fermi level as Compared to valence Band.

flat fermi level as no Current.

This is K/a inversion [earlier

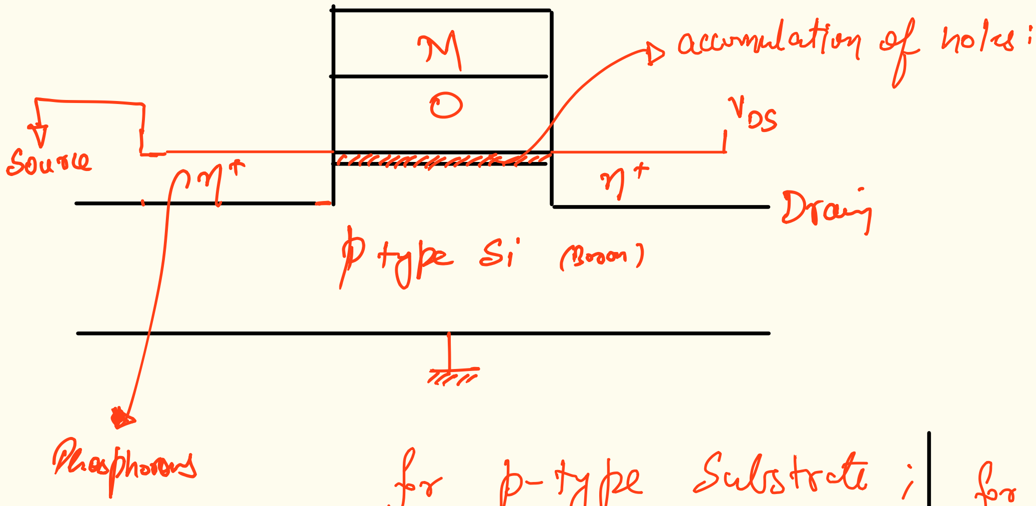
* Band Bending in accumulation is Very Small

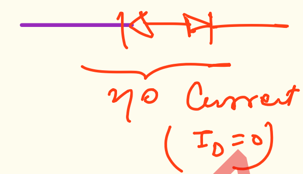


p type, -ve bias

more holes

⊂ Accumulation





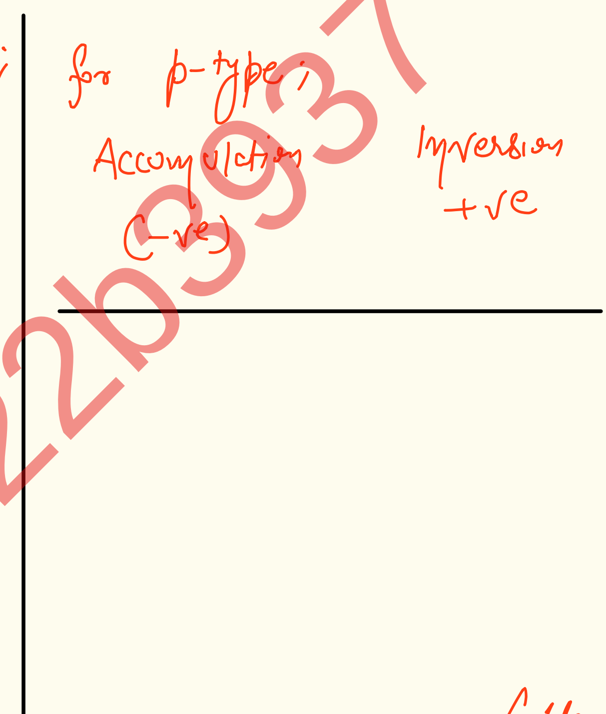
for p-type Substrate ;

when $V_{DS} = +ve$
$V_{GS} = -ve$

then ; $I_{DS} = 0$

when $V_{DS} = +ve$
$V_{GS} = +ve$
$I_{DS} =$ finite.

for p-type ;



* e^- Can Come in the Channel after a Threshold Voltage

$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}}$$

per unit area

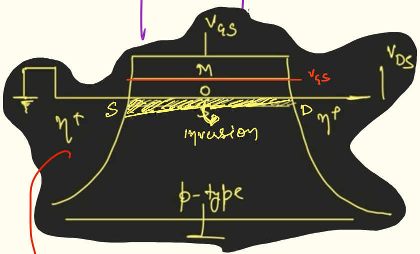
$$Q = C_{ox} \cdot V_{GS} \quad \left\{ \begin{array}{l} \text{assuming} \\ V_{DS} = 0 \end{array} \right\}$$

$$Q_{inv} = C_{ox} \cdot (V_{GS} - V_T)$$

$$I_{DS} = f(V_{DS}, V_{GS})$$

$$Q = C_{ox} \cdot V_{GS}$$

Some Characteristics of Mosfet



n- mosfet

n- FET

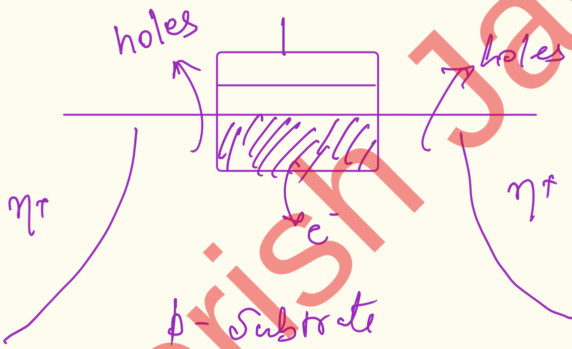
1. 4-Terminal Device
2. for n-mos; $V_S = V_{SUB} = 0$
3. V_T = Threshold Voltage = +ve
4. Enhancement mode
   $I_{DS} = 0$, $V_{GS} < V_T$
   Subthreshold region
5. $V_{GS} \geq V_T$; above threshold
   $I_{DS} > 0$
6. Source → Source the e^-
7. Drain :→ Drains the e^-
8. majority Carrier Device w.r.t. S/D
9. Unipolar device
10. Heart of Device - mos Capacitor

* for transistor
$n = 10^{18} cm^{-3}$
$\mu_n = 300 cm^2/V.S.$

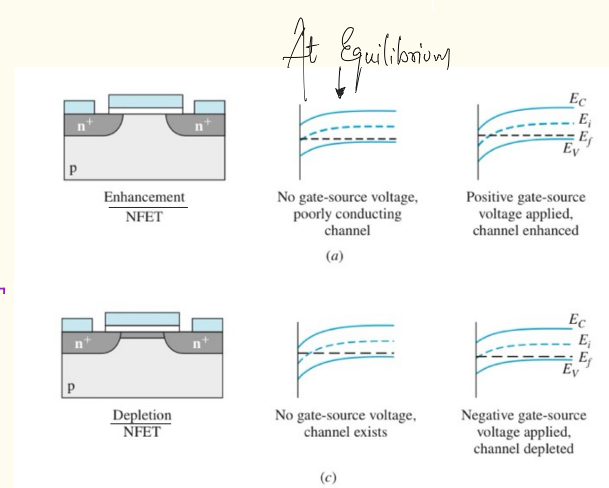
Depletion Mode : $V_{GS} < 0$

In Enhancement mode ; Current flows from Source Edge to Drain Edge

if it is not the Cox ; then Current = 0



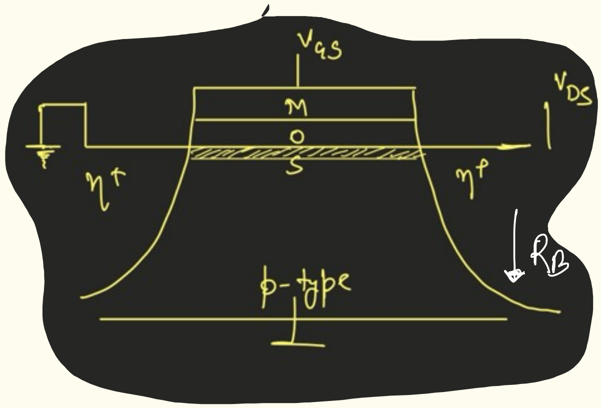
$n^+ - p - n - p - n^+$
Current = 0



if longer gate length ;

Reverse Bias

$I_G = I_{sub} = 0 \rightarrow$ always due to Oxide Insulation irrespective of RB/FB



$I_G = 0 \ \forall \ V_{DS}$ & V_{GS} {Cuz of Oxide}

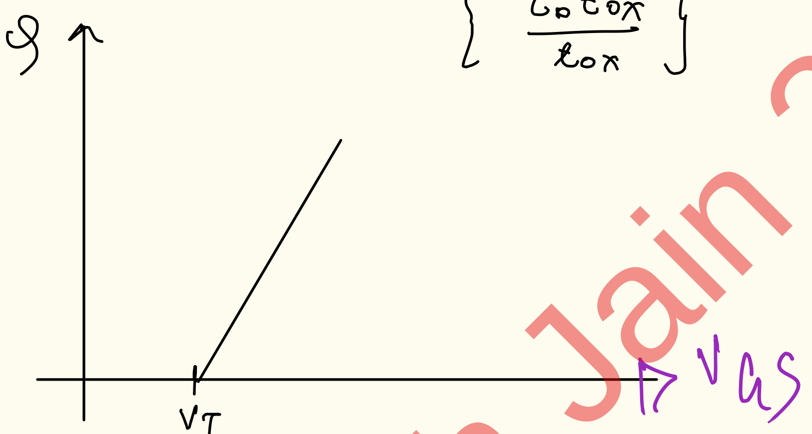
$I_{sub} = 0 \ \forall \ V_{DS}$ & V_{GS}

$I_{DS} = 0 \ \forall \ V_{DS}$ & $V_{GS} < V_T$

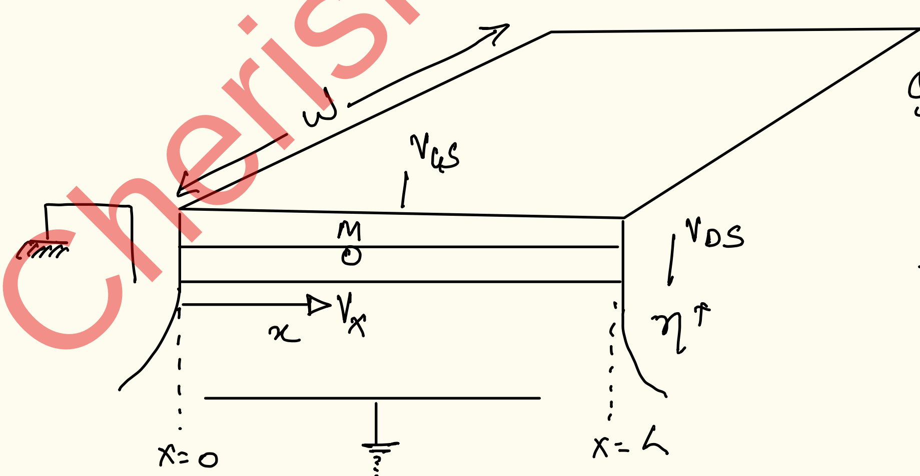
$I_{DS} \neq 0$ Only when $V_{GS} > V_T$ & $V_{DS} = +ve$

* $Q = C_{ox}(V_{GS} - V_T) \rightarrow$ Don't ask why V_T

$C_{ox} \rightarrow$ Capacitance / Area $\left\{ \dfrac{\epsilon_0 \epsilon_{ox}}{t_{ox}} \right\}$



Overlap Capacitor



$Q = C_{ox}(V_{GS} - V_T - V_x)$

$I_{DS} = Q\, v_{el}$ — (1)

$I = \sigma E$
$= (n q \mu) E$
$= n q\, v$
$= Q \cdot v_{el}$ — (2)

By (1) & (2)

$I_{DS} = Q v_{el} = \mu_n \cdot C_{ox} \cdot (V_{GS} - V_T - V_x) \cdot E$

$= -\mu_n C_{ox}(V_{GS} - V_T - V_x)\left(\dfrac{dV_x}{dx}\right)$

$$\int_0^L I_{DS}\,dx = -\mu_n C_{ox} \int_0^{V_{DS}} (V_{GS} - V_T - V_x)\,dV_x$$

$$I_{DS} \cdot L = -\mu_n C_{ox} \left\{ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right\}$$

$$I_{DS} = -\mu_n C_{ox} \left\{ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right\}$$

now this is analysis of a 2D model; but as shown above it's a 3D model; so:-

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

So; $I_{DS} = f(V_{GS}, V_{DS})$

Valid if:-

1) $V_{GS} > V_T$ { not when $V_{GS} = V_T$ }

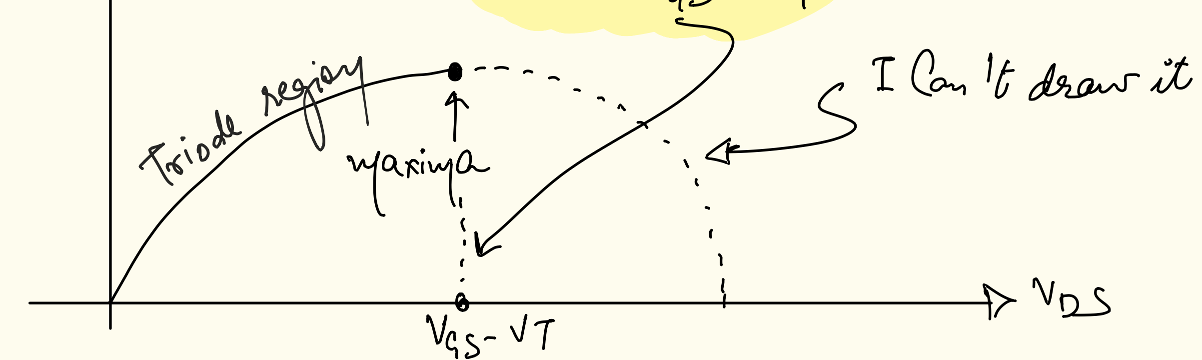
2) $V_{DS} > 0$

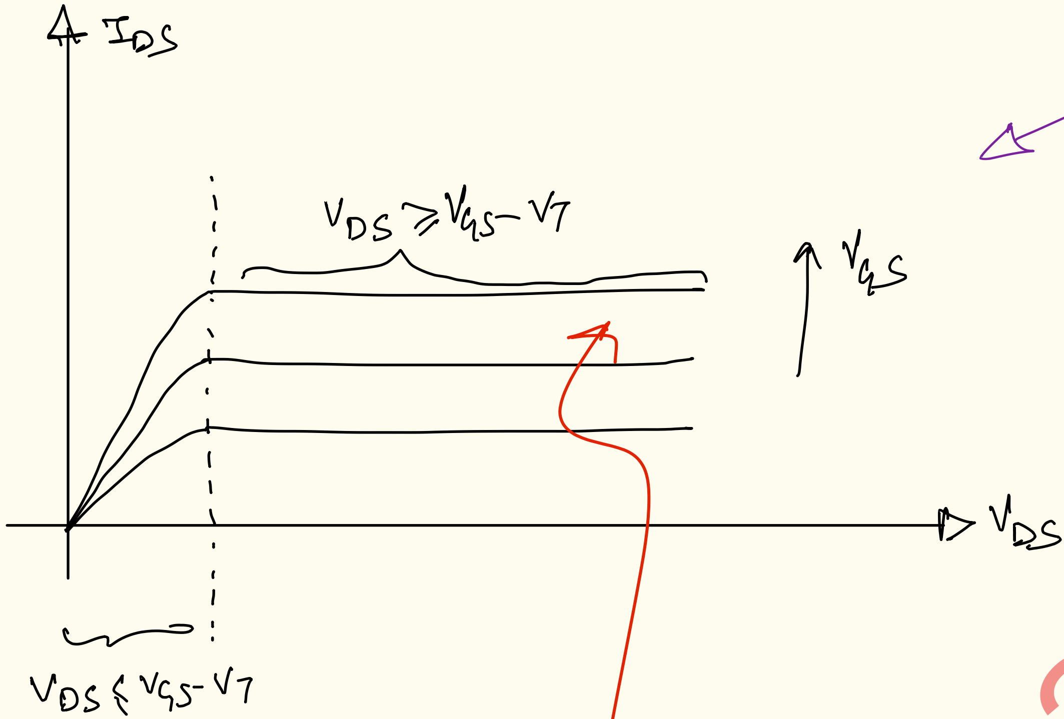
3) $V_{DS} < V_{GS} - V_T$

$$Q = -\underbrace{W C_{ox} (V_{GS} - V_T - V_x)}_{\text{Should be +ve } \forall x}$$

@ $x = L$, $V_x = V_{DS}$

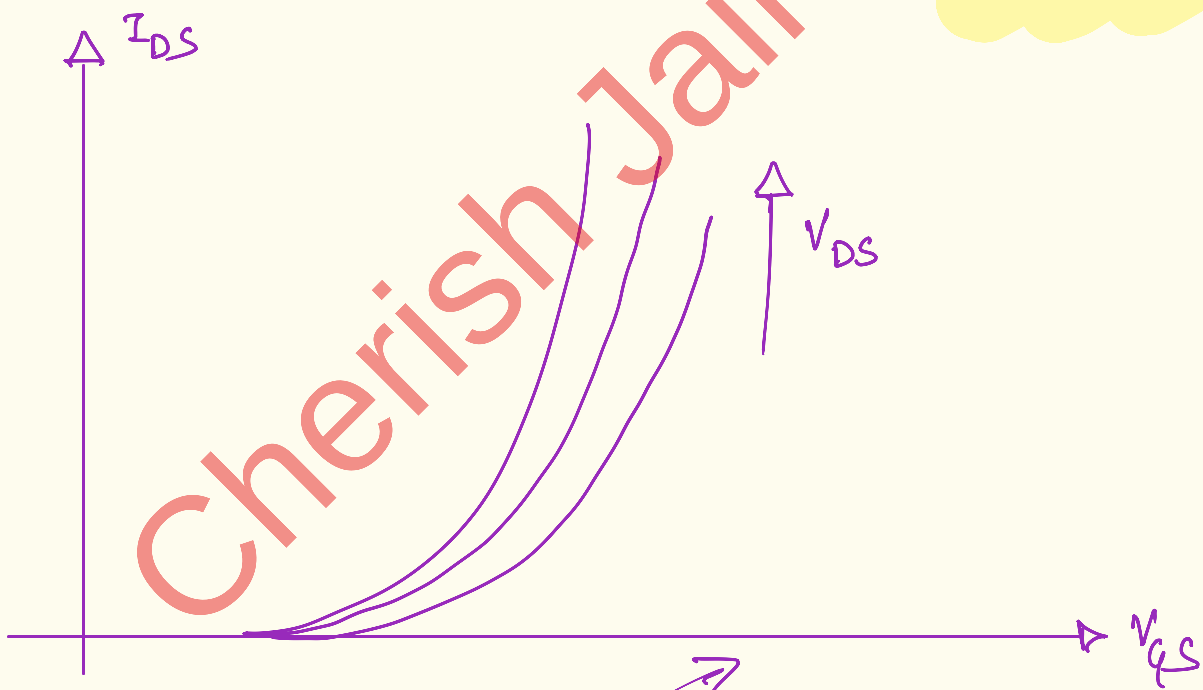
Hence $V_{DS} \leq V_{GS} - V_T$



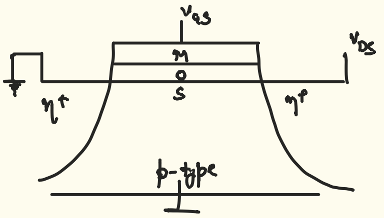


Output Characteristic

Here for Saturation region; $I_{DS} = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2$

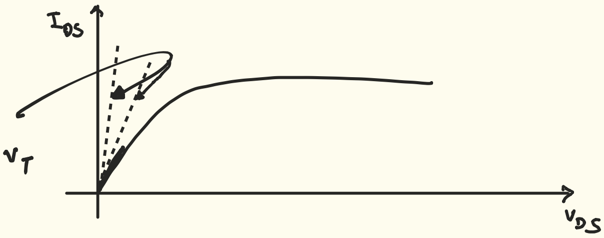


Transfer Characteristic



$$I_{DS} = \frac{\mu_n C_{ox} W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad ; \quad V_{DS} \le V_{GS}-V_T$$

$$= \frac{\mu_n C_{ox} W}{2L}\left[(V_{GS}-V_T)^2\right] \quad ; \quad V_{DS} > V_{GS}-V_T$$



Slope decided by $V_{GS}-V_T$

Case I :- $V_{DS} << V_{GS}-V_T$

$$I_{DS} \approx \frac{\mu_n C_{ox} W}{L}\left[V_{GS}-V_T\right] V_{DS}$$

(Linear Region)

* Voltage Variable Resistor

Case II :- $V_{DS} > V_{GS}-V_T$

$$I_{DS} = \frac{\mu_n C_{ox} W}{2L}(V_{GS}-V_T)^2$$

Independent of V_{DS}
(Saturation Region)
Also k/a Constant Current Region

Output parameters

$$\frac{\partial I_{DS}}{\partial V_{DS}} = 0$$

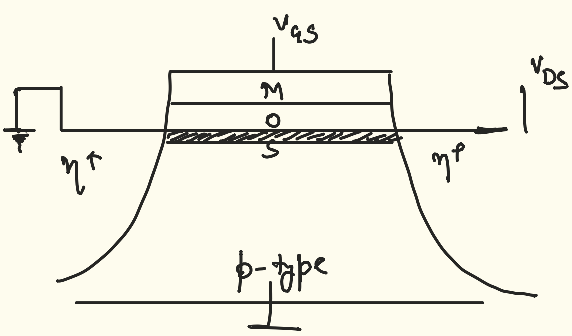
$\therefore$ Dynamic Conductance $= 0$ ~~(but $\frac{I_{DS}}{V_{DS}}$ = finite)~~

Dynamic Resistance $= \infty$

Case III :- $V_{DS} = V_{GS} - V_T$

$$\begin{cases} \rho(x) = C_{ox}(V_{GS}-V_T-V_x) \\ \rho(x=0) = C_{ox}(V_{GS}-V_T) & V|_{x=0} = 0 = V_S \\ \rho(x=L) = 0 & V|_{x=L} = V_{DS} \end{cases}$$

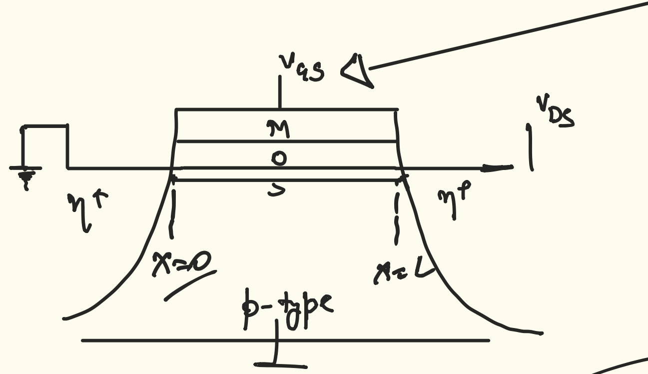
why Current saturates ?



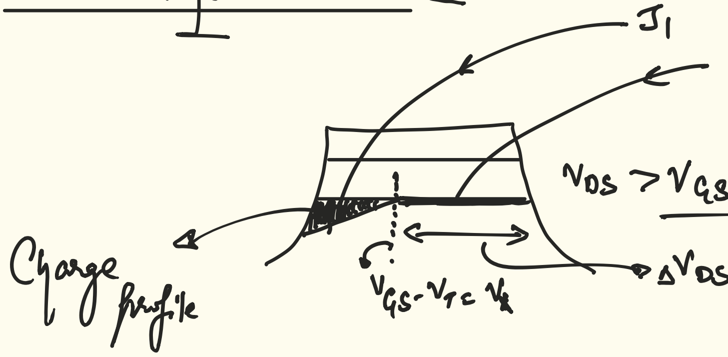
$$\rho = C_{ox}(V_{GS}-V_T-V_{DS})$$

$$\Rightarrow \rho > 0 \Rightarrow V_{GS}-V_T > V_{DS}$$

what happens when $V_{GS}-V_T < V_{DS}$



$$Q(x) = C_{ox}\left(V_{GS} - V_T - V_x\right)$$



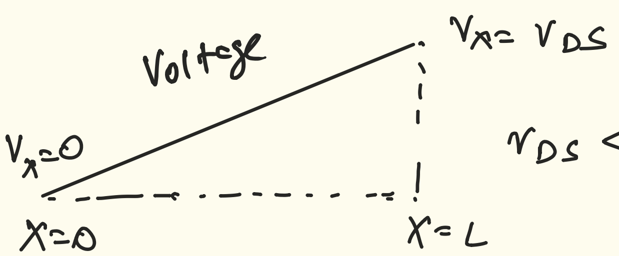
$V_{DS} > V_{GS} - V_T$

$\Delta V_{DS} = V_{DS} - \underbrace{(V_{GS} - V_T)}$

$= V_{DS} - V_{DS,sat}$

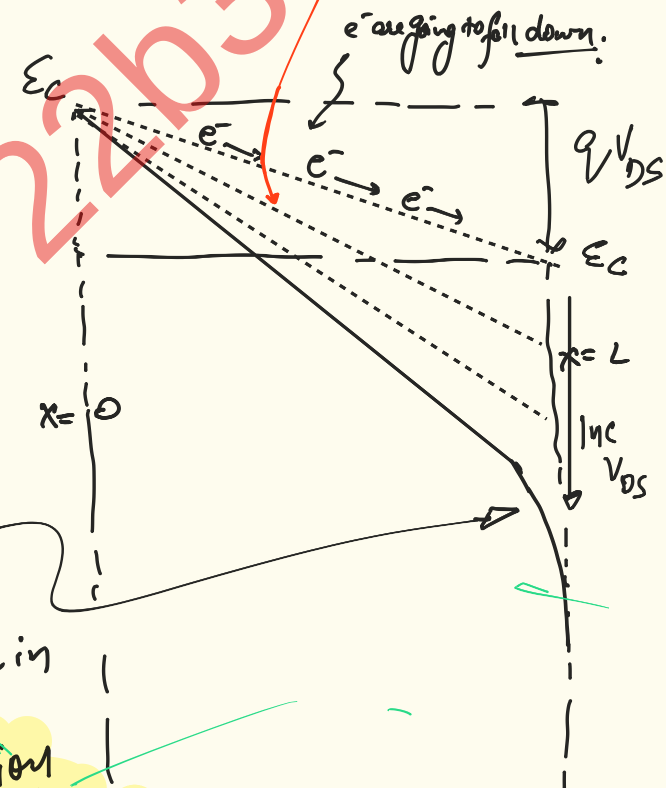
* Channel is pinched off.

E.F linear as $\left(\mathcal{E} = \frac{V_{DS}}{L}\right)$

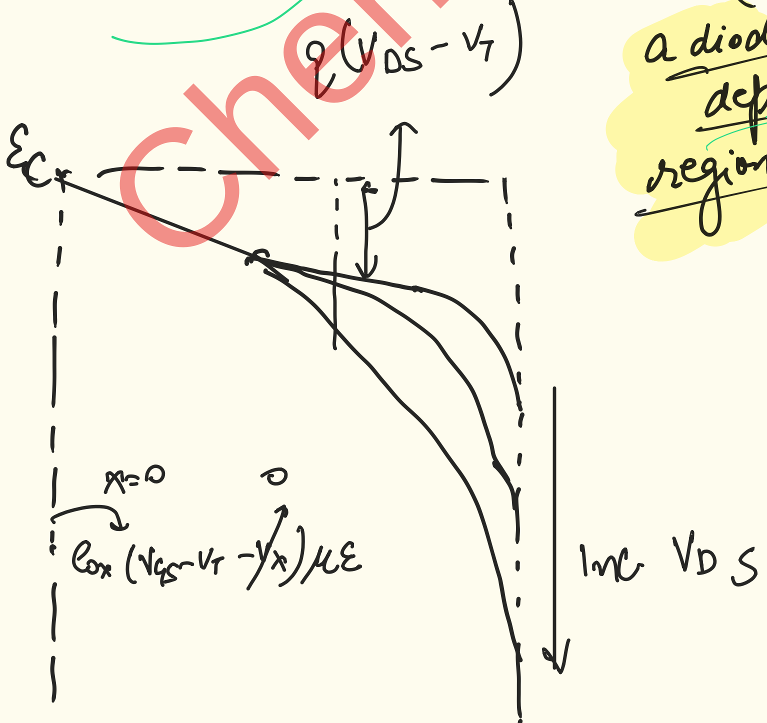


$V_{DS} << V_{GS} - V_T$

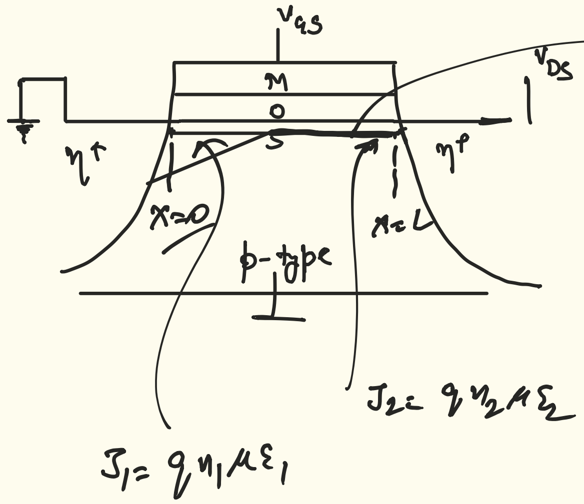
e⁻ are going to fall down.



Parabolic Profile (like in a diode depletion region {Charge=0})



Beyond pinched off; you can't change EF or some charge



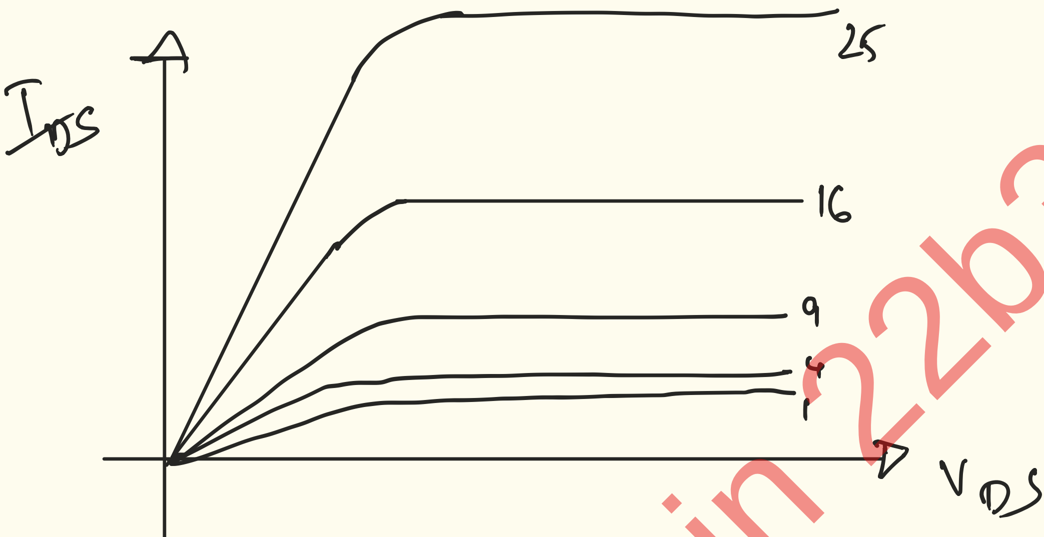
Current becomes Const once pinched off region starts.

$n_1 >> n_2$

$\varepsilon_1 << \varepsilon_2$

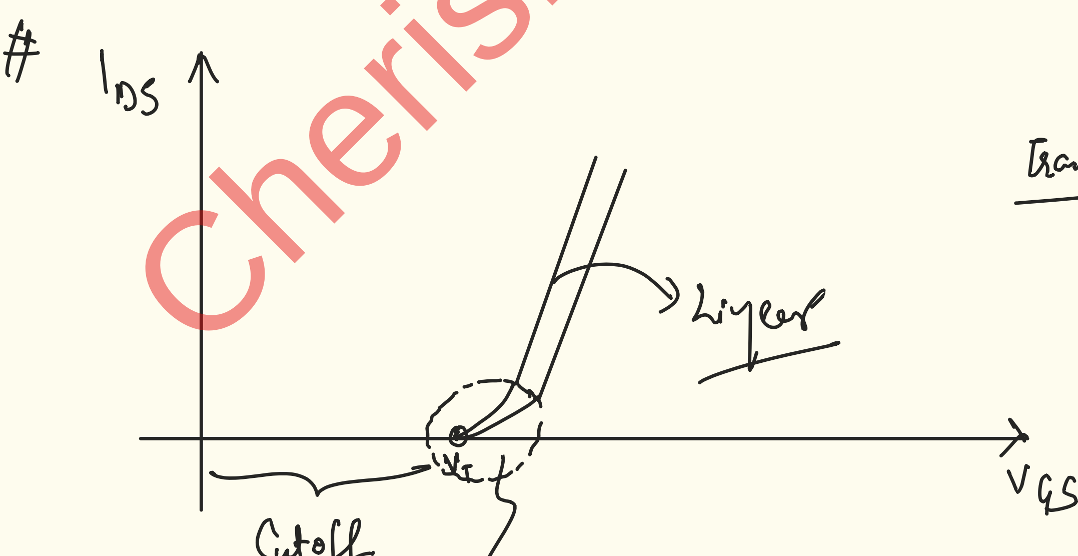
* Beyond pinchoff; Current is limited by Source injection.

{See [S | Channel | D] eg. from Book}



$$I_{DS} = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2$$

#



Transfer Characteristics

Saturation

$I_{DS} = 0 \; ; \; V_{GS} \leq V_T$

$V_{DS} >> V_{GS} - V_T$

Small Signal Analysis

$$I_{DS} = f(V_{DS}, V_{GS})$$

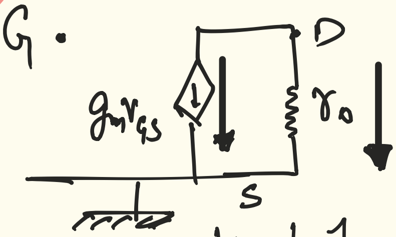
$$dI_{DS} = \frac{\partial f}{\partial V_{DS}} V_{DS} + \frac{\partial f}{\partial V_{GS}} V_{GS}$$

$v_{DS} \leftarrow$ Small Signal AC

$V_{DS} \leftarrow$ DC

$V'_{DS} \leftarrow$ DC + AC

$$\boxed{i_{ds} = \frac{1}{r_o} v_{ds} + g_m v_{gs}}$$

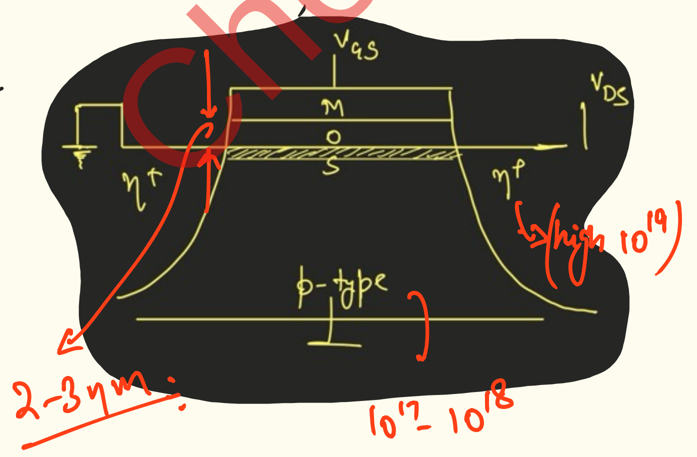


level 1

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\mu_n C_{ox} W}{L}(V_{GS} - V_T)$$

$$r_o = \left[\frac{\partial I_{DS}}{\partial V_{DS}}\right]^{-1} \approx \infty$$

#



$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}}$$

we want $C_{ox} \uparrow$
C_{ox} is large

$$Q = C_{ox}(V_{GS} - V_T)$$

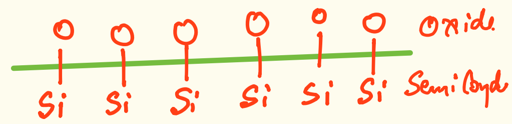
$$Q \uparrow \rightarrow J \uparrow$$

$$\boxed{g_m = \frac{\partial I_{DS}}{\partial V_{GS}}}$$

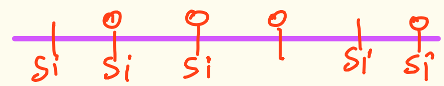
for SiO_2; $\epsilon_{ox} \simeq 3$

most Stable oxide :- Si / SiO_2 ;

Ideally ; we want →



But due to defects →



to ↑ C_{ox} ; t_{ox} ↓

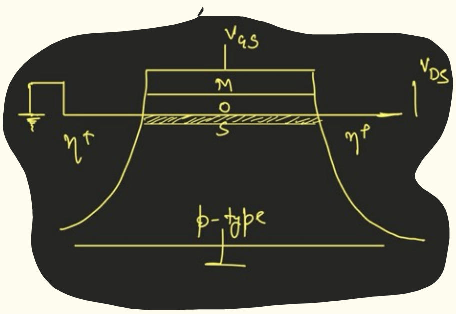
ple tried replacing Si with InGaAs for high
't good

$Q = CV$; V

$V_{GS} \neq V_T$

$V_{GS} < 0$ → Accum
$V_{GS} \in 0, V_T$ → Depl
$V_{GS} > V_T$ → Inves

V_T



$V_{DS} << V_{GS} - V_T$

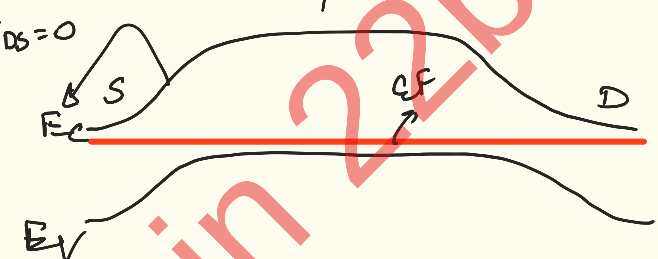
$I_{DS} \approx \frac{\mu_n C_{ox} W}{L} [V_{GS} - V_T] V_{DS}$

$V_{DS} > V_{GS} - V_T$

$I_{DS} = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2$

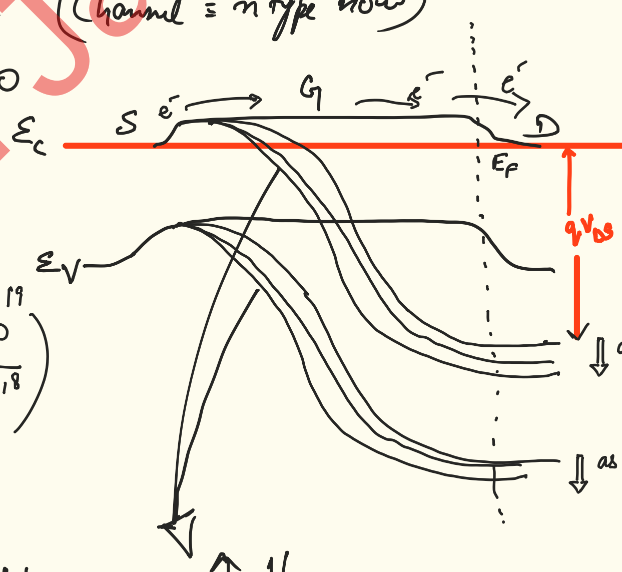
$V_{GS} < V_T$:-

$V_{DS} = 0$



$V_{GS} \geq V_T$ (Channel = n type now)

$V_{DS} = 0$



(fermi level close to $\mathcal{E}_c$)

$\Downarrow$ as u $\uparrow$ V_{DS} for $V_{DS} < V_{GS} - V_T$

but once $V_{DS} > V_{GS} - V_T$

$\Downarrow$ as u $\uparrow$ V_{DS}

Barrier height $= \frac{k_B T}{q} \ln\left(\frac{10^{19}}{10^{18}}\right)$

$\equiv kT \ln\left(\frac{N_C}{n_s}\right)$

Happens on $\uparrow V_{DS}$

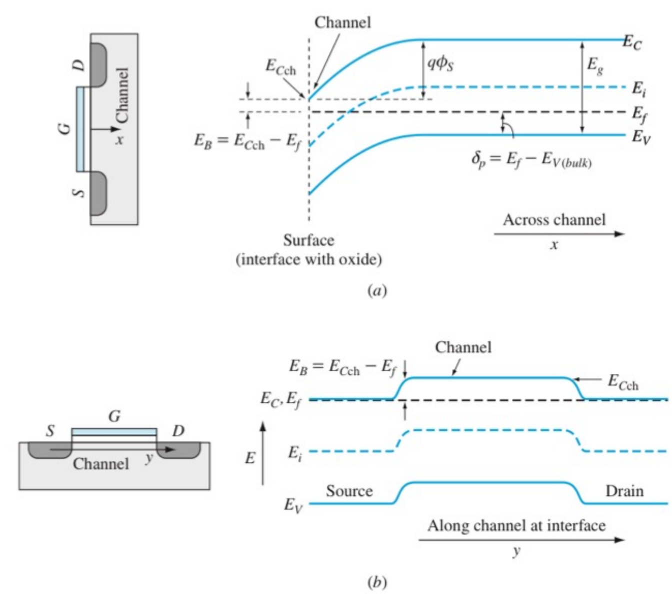
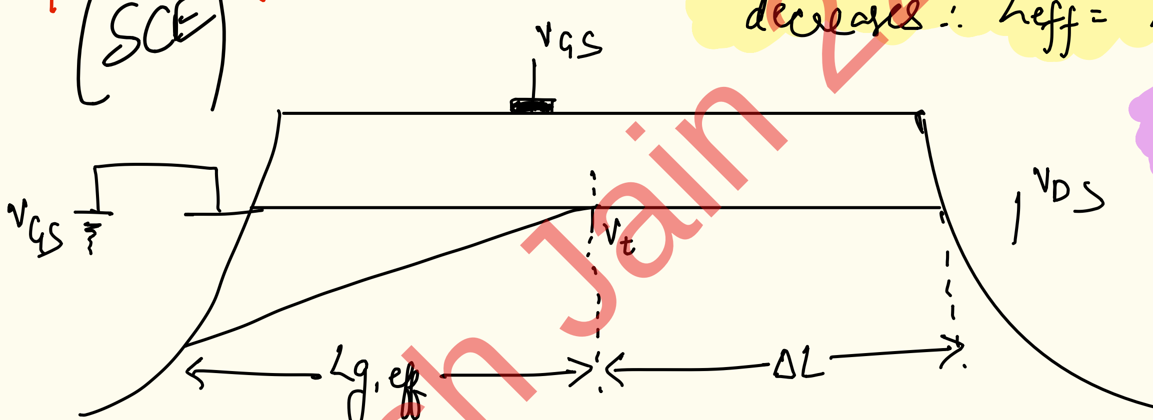


Figure 7.14 The energy band diagram of the NFET across the channel (a) and along the channel (b), with zero voltage between the drain and the source.

Small Channel Effects

[SCE]

If $V(x)$ becomes 0 somewhere before $x = L$; effective length decreases ∴ $L_{eff} = L - \Delta L$



$V_{DS} \uparrow \Rightarrow L_{eff} \downarrow$

$I \uparrow$

resulted in pinchoff

$V_{DS} > V_{DS,Sat}$

Hence $I_{DS} = \dfrac{\mu_n C_{ox} W}{2(L - \Delta L)} (V_{GS} - V_T)^2 \approx \dfrac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2 \left(1 + \dfrac{\Delta L}{L}\right)$

$$\frac{\Delta L}{L} = \lambda (V_{DS} - V_{DS,Sat})$$

Don't ask why! it's a fact

So; $\boxed{I_{DS} = I_{DS_0} \left(1 + \lambda (V_{DS} - V_{DS,Sat})\right)}$

$\frac{\Delta L}{L} \approx \lambda (V_{DS} - V_{DS,Sat})$ $\{\lambda \approx 0.01 - 0.03\}$

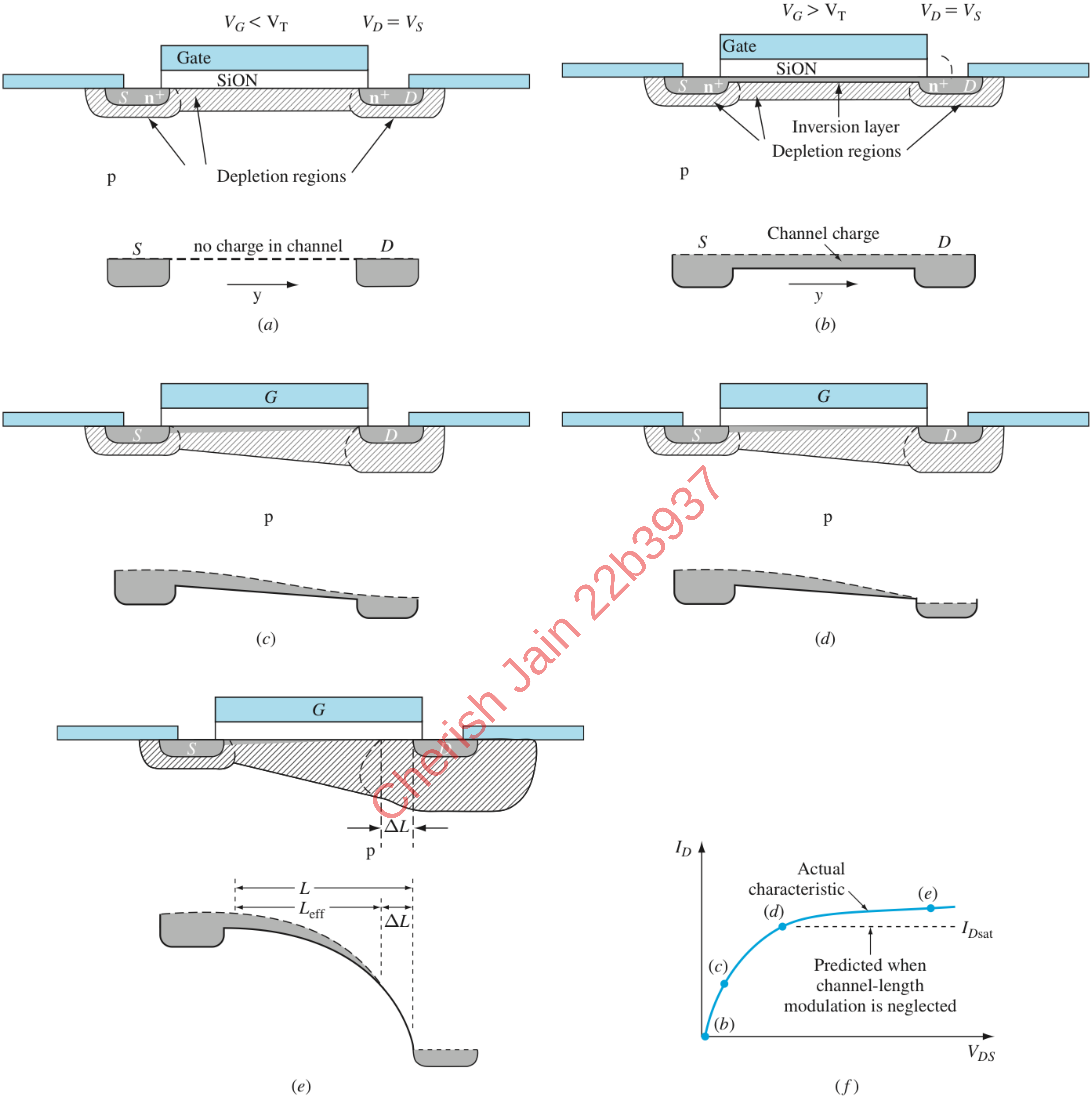


Figure 7.24 Qualitative explanation for channel-length modulation. Parts (a) to (e) show the energy bands (top) and hybrid diagrams (bottom). Parts (a) to (d) repeat the explanation of the simple long-channel model. In (e), as the drain voltage continues to increase, the point at which the channel charge approaches 0 (shaded region), or the point at which $V_{ch} = V_{GS} - V_T$, moves along the channel toward the source. The channel becomes effectively shorter. (e) The corresponding points on the I_D-V_{DS} characteristics are shown in (f). From point (d) on, the simple model predicts constant current (dashed line).

$1+\lambda V_{ds}=0$

$\lambda = \frac{-1}{V_{DS}}$

$\frac{\Delta L}{L_g}$ } Substantial only when L_g is small.

eg → $\frac{5nm}{1\mu m} = 0.005$ → negligible

$\frac{\Delta L}{L} = \lambda (V_{DS} - V_{DS,sat})$

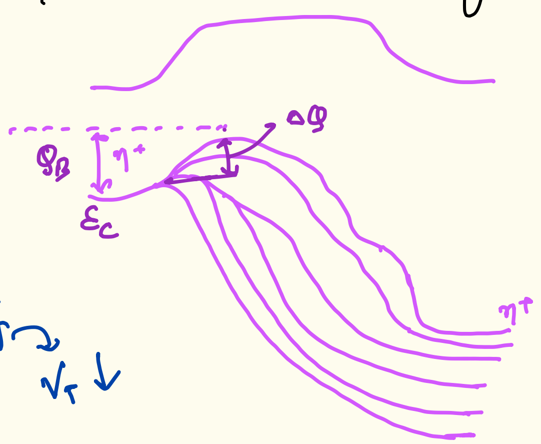
→ Small for longer Gate length Transistor

if Substrate doping ↑; λ becomes less sensitive i.e. λ is ↓

Hence to ↓ gate length we tend to increase doping.

② Drain Induced Barrier Lowering.

→ Source to Barrier lowering



Source → more e^- → Channel $I \uparrow$ → $V_T \downarrow$

$V_T = V_{T0} - \sigma (V_{DS} - \cancel{V_{DS,eff}})$ → negligible; Hence ignored

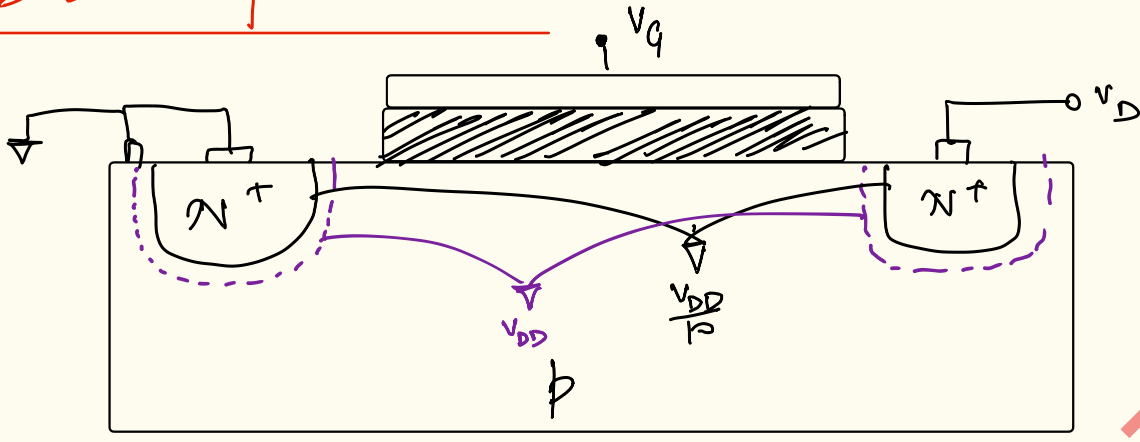
$\Delta V_T = \sigma V_{DS}$

σ: V_T roll off factor

Effect k/a DIBL

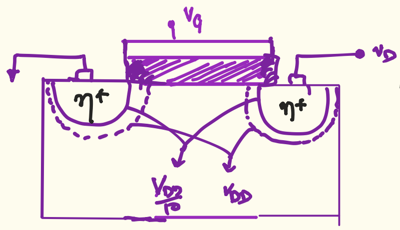
DIBL in detail

*



V_T remains same whether $V_{DS} = V_{DD}$ or $\frac{V_{DD}}{10}$

but if MOS



$V_{DS_1} = \frac{V_{DD}}{10} \Rightarrow V_{TH} = V_{TLIN}$ → linear

$V_{DS_2} = V_{DD} \Rightarrow V_{TH} = V_{TSAT}$ → sat

for long channel; $V_{TLIN} = V_{TSAT}$

now; for achieving threshold voltage is easy @ V_{DD} as channel length has reduced

⟹ Drain voltage ⟹ lowering Threshold

* Depletion region protrudes more in "p" part as n region is n^+

note

In short channel devices; SCE are dominant in both sublinear & saturation regions.

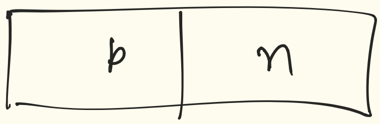
But in long channel; they are prominent in saturation region only!!

Diff b/w n^+ & n Semiconductor

p-n diode v/s p-n^+ diode.

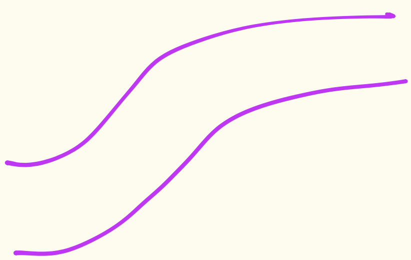
$N_D W_n = N_A W_p$

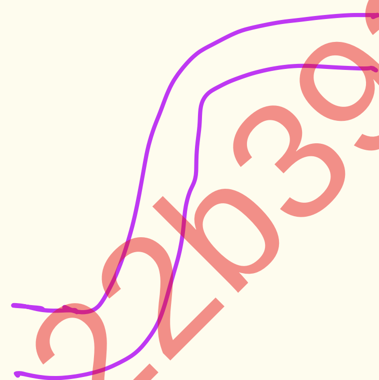
more less



hence w less

whichever higher doped; depletion region protrusion less in that region



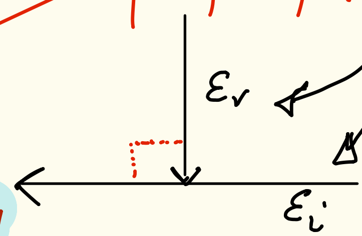


$$J_{DS} = \frac{\mu_n C_{ox} W}{2L}\left(V_{GS} - V_T'\right)^2\left(1 + \lambda\left(V_{DS} - V_{DS,sat}\right)\right)$$

③ Surface Scattering

Assumption: $\frac{\partial \mathcal{E}_x}{\partial x} \gg \frac{\partial \mathcal{E}_y}{y}$ → $|V_{DS}| \gg |V_{GS}|$

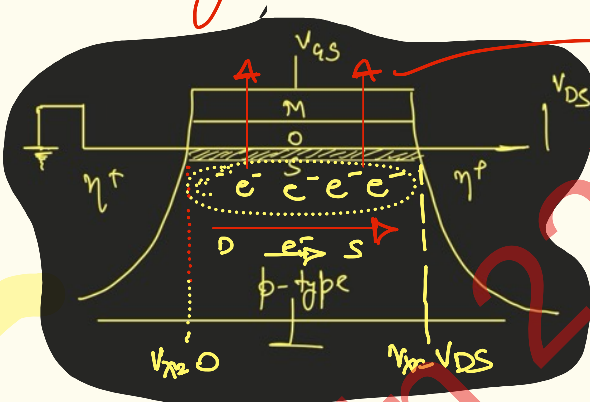
$\underbrace{\qquad}_{\mu = \mu_{lf}}$ ⟶ low field



These are orthogonal to each other

* This approxim. is k/a Gradual Channel approx. / GCA

As Collision ↑ ;
$\tau \downarrow \Rightarrow \mu_{lf} \downarrow$
↓
μ_{lf} dec. by a factor of 3~6



e^- pulled when V_G↑ with much stronger force

but they are moving from left to right
⇓
results in more friction

low field mobility (vertical) = $\mu = \frac{\mu_{lf}}{1 + \theta(V_{GS} - V_T - V_x)}$ ← Const

when V_{GS}↓

friction not here

We should have used this while integration but V_x → won't allow us :

Hence $\mu = \frac{\mu_{lf}}{1 + \theta(V_{GS} - V_T)}$ {get rid of V_x}
↓
why / How?
Out of scope of this Course

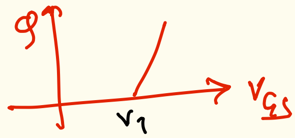
$$\therefore\ I_{DS} = \frac{\mu_{lf} C_{ox} W \left(V_{GS} - V_T'\right)^2\left(1 + \lambda\left(V_{DS} - V_{DS,sat}\right)\right)}{2L\left(1 + \theta\left(V_{GS} - V_T\right)\right)}$$

V_T :- Voltage @ which some carriers can move in channel

Shorter Channel :- As you apply V_{GS} ;

Shorter Channel length MOSFET

Should be much larger as Channel length smaller to ensure φ to supersede effect of V_{DS} on Charge Carriers



no charge channel formed

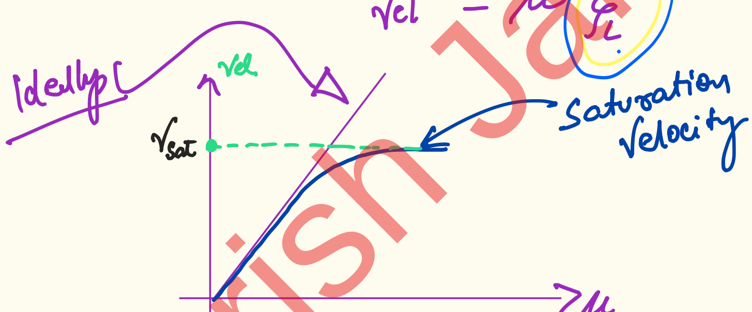
holes acts as Charge Carrier & starts acting as Resistor

if we don't apply ; Current gets Ctrld by V_{DS}

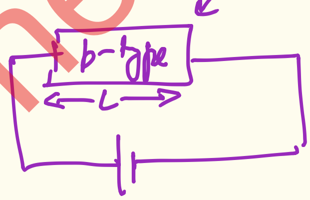
as $V_{GS}\uparrow$; $\mu\downarrow \rightarrow I\downarrow$

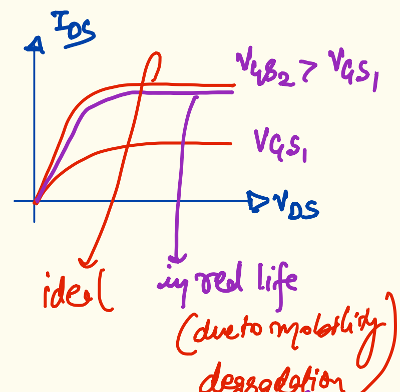
④ Velocity Saturation

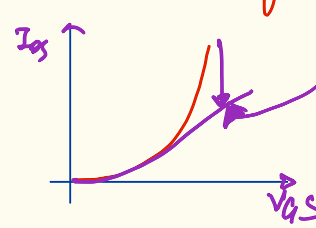
$vel = \mu \varepsilon_L$



as u keep on inc μ ; but after a level ; due to lattice Scattr. of host lattice ; we Can't incr. vel ,

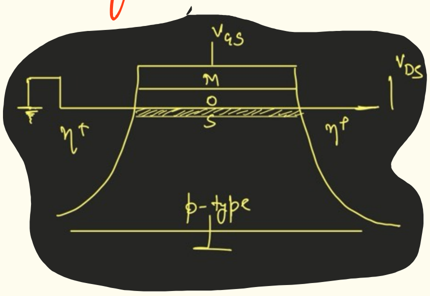






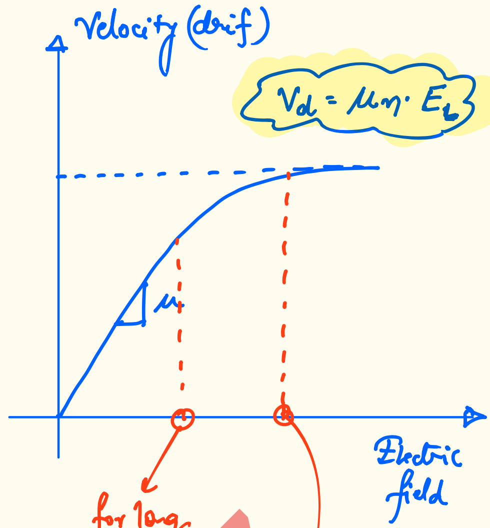
So ; $$vel = \frac{\mu \varepsilon}{1 + \left(\varepsilon/\varepsilon_L\right)}$$

Velocity Saturation



$\vec{E}_L = \dfrac{V_{DS}}{L}$; if $L \downarrow\downarrow$ $\vec{E}_L \uparrow\uparrow\uparrow$

lateral electric field



for long Channel

you will be here for long Channel.

we reach Sat^n vel already at even low V_{DS}

Hence Even if u increase V_{DS} ; velocity will have no more increment.

Hence I_{DS} saturates even before pinch off Cond^n

$V_{D\,Sat} = V_{DS}$ @ which drift velocity of electrons = Saturation velocity

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{min} - \frac{V_{min}^2}{2} \right]$$

$$\mathcal{E}_L = \frac{V_{DS}}{L}$$

$$V_{min} = \min \{ V_{D\,sat} ,\ V_{GS} - V_{Th} \}$$

$$|V_{el}| = \mu |\mathcal{E}_L|$$

$$\mu = \frac{\mu_{ef}}{1 + \frac{\mu_{ef} |\mathcal{E}_L|}{\text{Sat}^n \text{ vel.}}}$$

use this μ in I_{DS} formula.

$$I_D = \frac{W C'_{ox} \mu_{lf}}{L + \frac{\mu_{lf} V_{DS}}{\upsilon_{sat}}} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad V_{DS} \le V_{DSsat}$$

$$I_{Dsat} = \frac{W C'_{ox} \mu_{lf}}{L + \frac{\mu_{lf} V_{DSsat}}{\upsilon_{sat}}} \left[(V_{GS} - V_T) V_{DSsat} - \frac{V_{DSsat}^2}{2} \right] \quad V_{DS} \ge V_{DSsat}$$

$$\varepsilon_L = \frac{V_{DS}}{L}$$

$$I_D = \frac{I_D (\text{no velocity saturation model})}{1 + \frac{\mu_{lf} V_{DS}}{L \upsilon_{sat}}} \quad V_{DS} \le V_{DSsat}$$

$$I_{Dsat} = \frac{I_{Dsat} (\text{no velocity saturation model})}{1 + \frac{\mu_{lf} V_{DSsat}}{L \upsilon_{sat}}} \quad V_{DS} \ge V_{DSsat}$$

$$V_{Dsat} = \frac{2(V_{GS} - V_T)}{\left[\left(1 + \frac{2 \mu_{lf} (V_{GS} - V_T)}{\upsilon_{sat} L} \right)^{1/2} + 1 \right]}$$

{for Velocity Saturation}

Short Channel Effects :- $L \le 90nm$

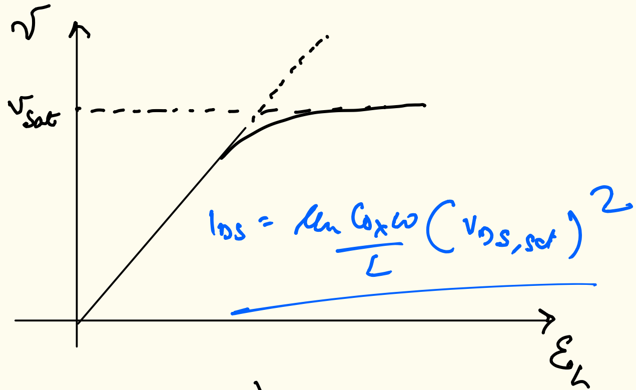
Long " :- $L > 180nm$

$v = \mu_f \mathcal{E}_L$

$$v = \frac{\mu_{if}\,\mathcal{E}_L}{1 + \mathcal{E}_L/\mathcal{E}_c}$$

μ

$\mu \downarrow$



$$\frac{I}{W} = \mu_f' C_{ox}(V_{GS} - V_T - V_x)\frac{dV_x}{dx}$$

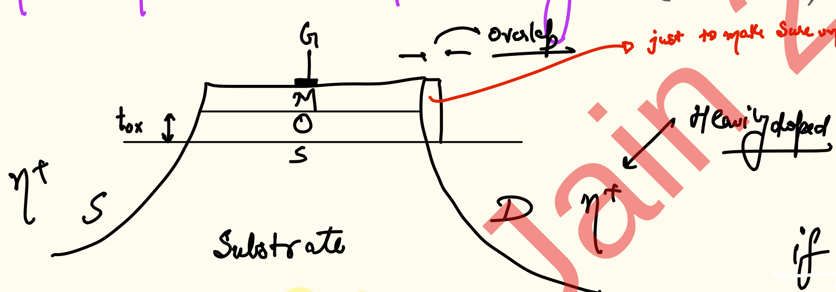
$$I_{DS} = \frac{I_{DS}\,(\text{w/o vel Sat}^n)}{\left(1 + \frac{\mu_{if}\cdot V_{DS,sat}}{L \cdot v_{sat}}\right)}$$

v_{sat} → Sat. vel.

L → gate length

{only when Critical E.F. is achieved}

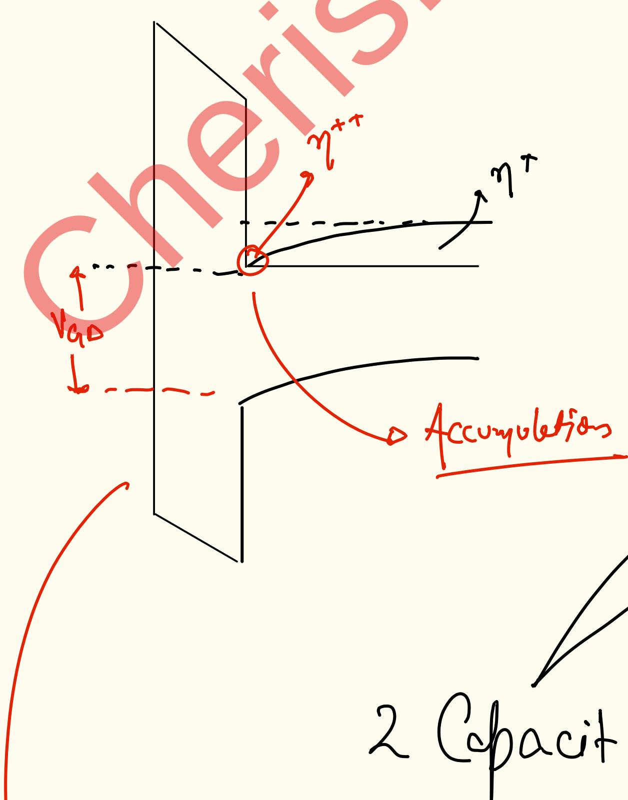
(5) Gate Induced Drain Leakage. (GIDL)



→ just to make sure overlap doesn't occur; {Engineering Safety}

if you ↓ tox very much then current starts flowing via Oxide due to Quantum effects {Quantum Tunnelling}

→ Band Diagram in overlap region



$V_{DS} = 0$

$V_{sub} = 0$

→ Accumulation

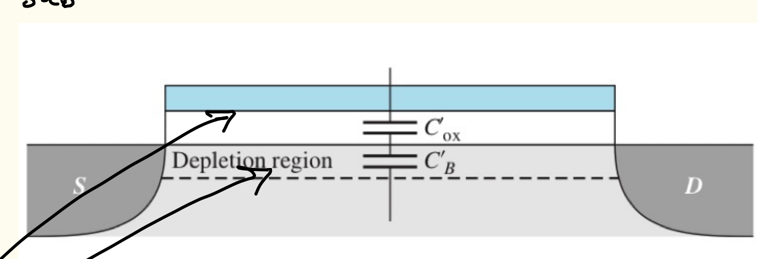
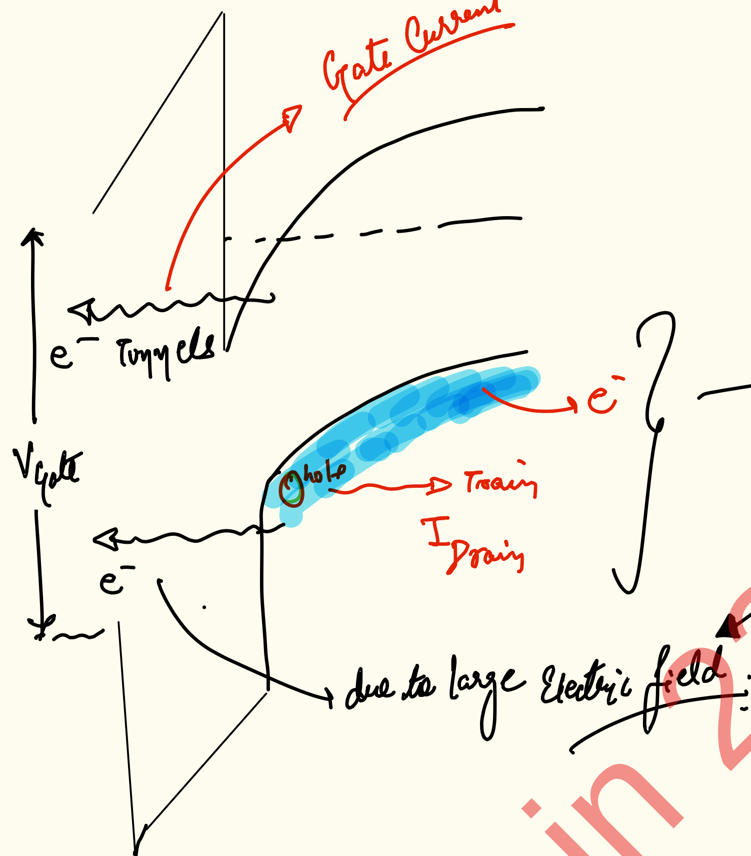


Figure 7.43 The capacitances of the MOSFET gate oxide and substrate. The substrate capacitance C_B' is the depletion layer capacitance.

2 Capacitances

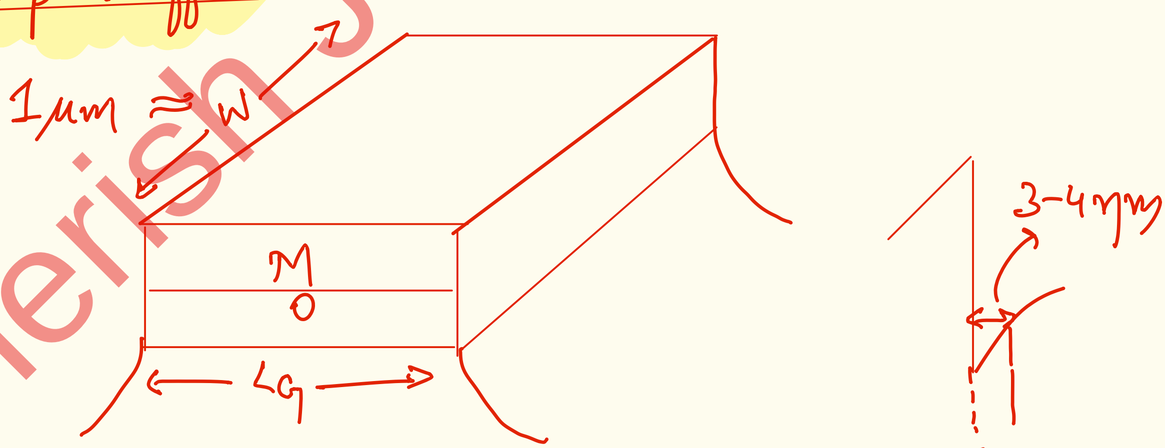
if I increase V_{GD} ;



Drain → Small
Gate → large

→ Happens in Overlap region dominantly

⑥ Discrete Dopant effect



inversion channel = t

$A = 5\times10^{-7}\times10^{-4}\ cm^2$

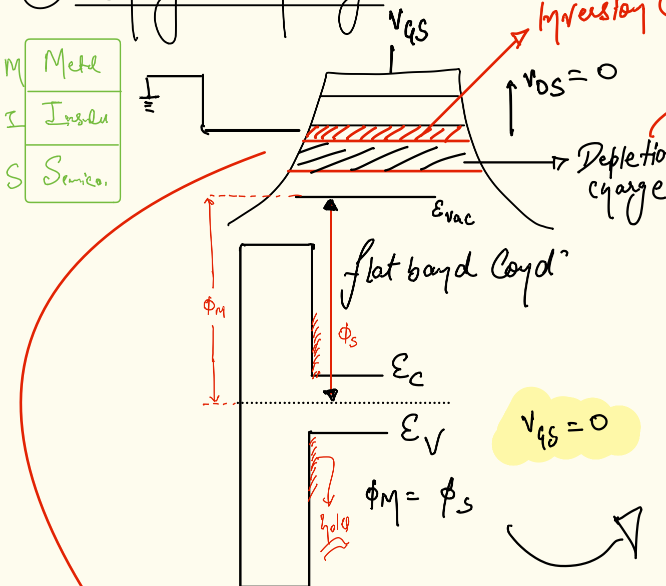
$= 5\times10^{-11}\ cm^2$

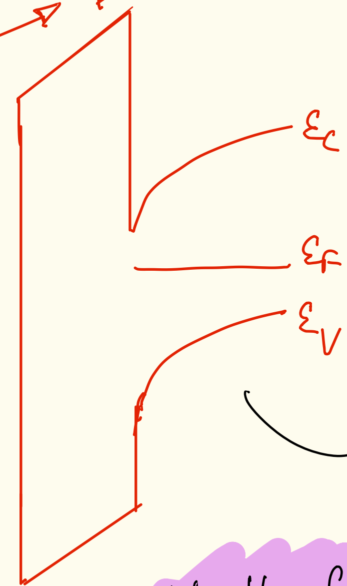
$V = W\times t = 5\times10^{-11}\times 3\times10^{-7}\ cm^3$

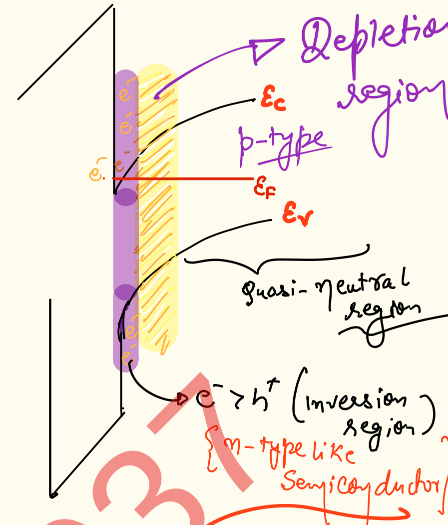
$= 15\times10^{-18} cm^3$ — volume

?

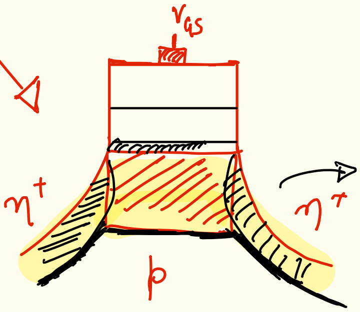
⑦ Charge Sharing







Ideally Charge should only would have taken Care by Gate



entire shaded part is Depletion region

* Centre is taken Care by Gate Voltage
* Side are taken Care by Source & Drain

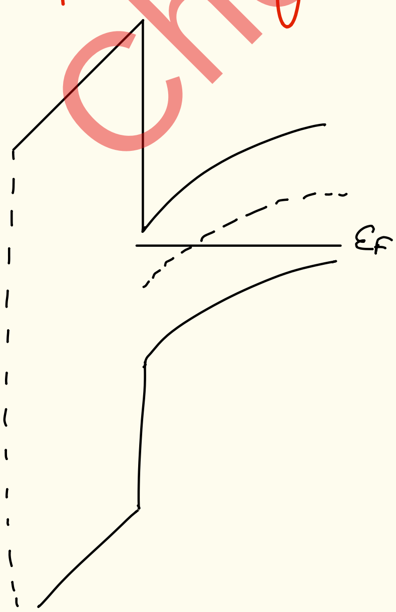
} This is CHARGE SHARING

$Q_{inv} \downarrow \rightarrow Q_{dep} \uparrow$ or $\underbrace{Q_{dep} \downarrow \rightarrow Q_{inv} \uparrow}_{V_T \downarrow}$

$Q_g = Q_{dep} \downarrow + Q_{inv} \uparrow$

$V_T \propto \left(\dfrac{Q_{dep} - Q_o}{C_{ox}} \right)$

Threshold Voltage



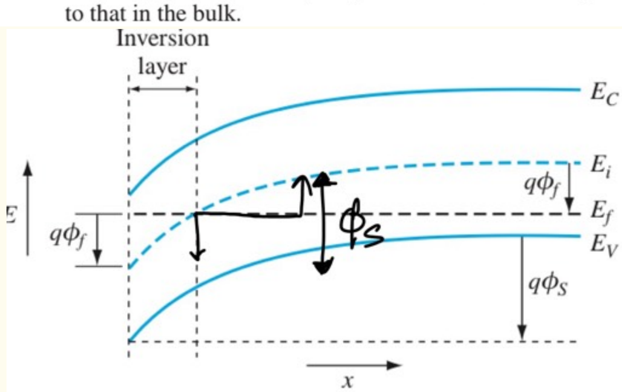
tron concentration in the semiconductor varies as

$$n = N_C e^{-(E_C - E_f)/kT} \tag{7.2}$$

The electron concentration and thus the conductance of the channel varies exponentially with $E_C - E_f$. This quantity is dependent on the gate-source voltage V_{GS}. An exponential is a smoothly (albeit rapidly) varying function, so it is not clear what value of gate-source voltage should be called *threshold*. A commonly used criterion is that the threshold voltage is the gate-source voltage required to induce an electron concentration at the Si surface that is equal to the hole concentration in the neutral substrate (N_A').[5] This is equivalent to saying that a channel exists if the Fermi level in the n channel is as far above the intrinsic level as the Fermi level in the bulk is below the intrinsic level. This condition is shown Figure 7.11. Then

$$\phi_s = 2\phi_f \tag{7.3}$$

where ϕ_s is called the *surface potential,* i.e., the voltage at the Si surface relative to that in the bulk.



* fermi level straight as long as no current is flowing

$$V_T = 2\phi_B + \frac{Q_{Dep}}{C_{ox}}$$