$$J = J_0 \left(e^{\frac{V_a - J(R_n + R_p)}{V_T}} - 1 \right)$$

$V_a - J(R_n + R_p)$ → Voltage drop across Quasi neutral region

Hard to Solve

Earlier ($V_a = 0.8$)

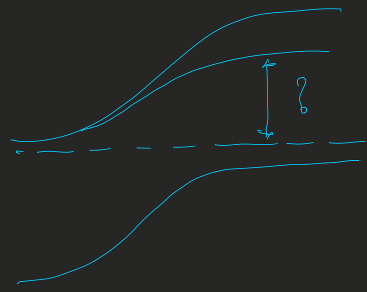
$\Delta n_p = 2.8 \times 10^{15}\ cm^{-3}$

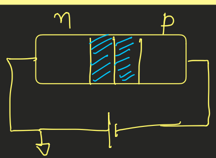
$E_{Fn}^{p} = 0.026 \ln\left(\frac{N_c}{n_p}\right)$

Quasi fermi level for e^- in p region

$= 0.026 \times \ln\left(\frac{2.8 \times 10^{19}}{2.8 \times 10^{15}}\right)$

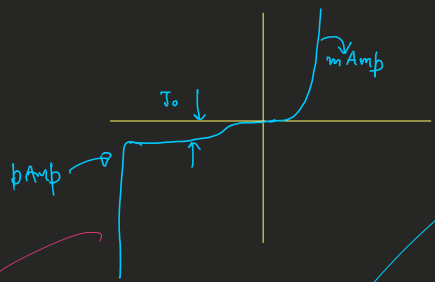
$= 0.026 \ln(10^4)$





(reverse Biased) → $J = J_0 \left(e^{V/V_T} - 1\right)$ $\approx -J_0$

V is large & −ve



Slope $\approx \frac{1}{R_n + R_p}$

as reverse Bias ↑; Depletion region gets wider

KE ↑ ; e^- Collides with Bound e^- & it Can launch a Bound e^- & thus Create a $e^- - h^+$ pair

of the very very few free mobile Carriers

$1e^-$ generate → $1e^-$, $1h^+$

$\therefore 1e^- \longrightarrow 2e^-, 1h^+$

$2e^- + h^+$ $2e^- + h^+$

$2e^-$ $1h^+$ $2e^-$ $1h^+$ $2e^-$ $1h^+$ $2e^-$ $1h^+$

This effect is k/a **Avalanche effect**

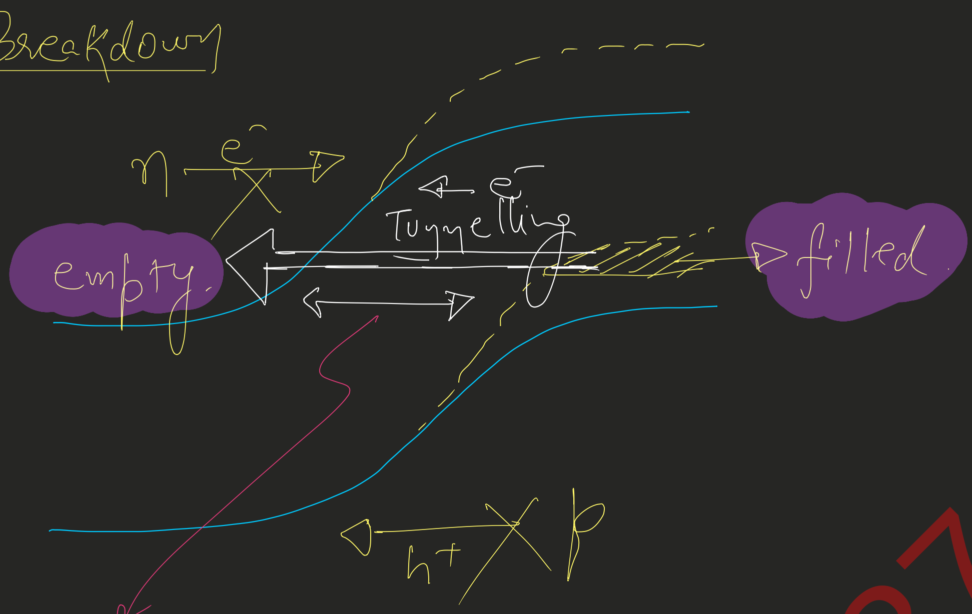
$\therefore$ Depletion region flooded with e^- & h^+ ⟹ huge Current {mostly ltd by resistance of p, n region}

✱ Each material has it's own E_{cr} — Critical Electric field

{larger bandgap → more the E_{crit}}

e^- $\frac{e^-}{h^+}$ E_g

Zener Breakdown



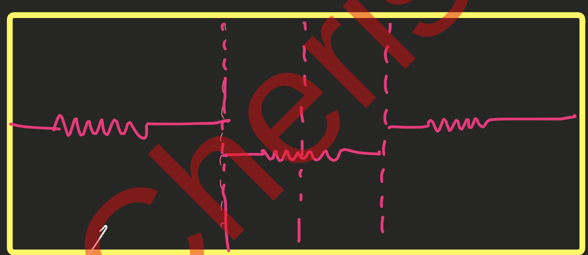
width / dist of depletion region ↓ — Tunnelling should be small

→ if doping density ↑ (N_A/N_D ↑) ⇒ Tunnelling prob ↑

↓ generally happen at relatively low bias

Hence Breakdown characteristic governed by
- → Avalanche (less doping density)
- → Zener (more doping density)

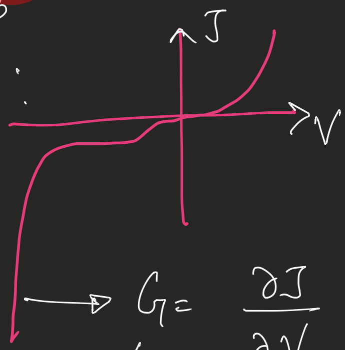
Diode



Sum of 3 Resistances.

Avalanche Diode
↓
most sensitive Photo diode.

we just keep V_a on verge of Breakdown; & then we apply $h\nu$; even when 1 photon generated → it will get detected as it will initiate Avalanche



→ $G = \frac{\partial J}{\partial V}$
Conductance

$R_{dyn} = \frac{\partial V}{\partial I}$

$G \to \infty$

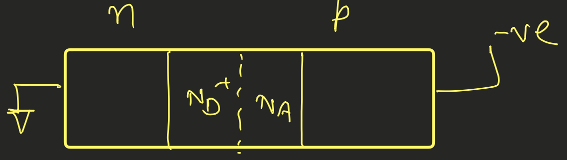
$R \to$ small

∵ Depletion region is due to lack of e^-/h^+. But in breakdown; free carriers ↑
So they try to ↓(w_n+w_p) but V_a tries to ↑(w_n+w_p). Thus they compete & ultimately J gets stabilized.

Capacitance

(for diode under Rev. bias)

①



≡ 

$$w \propto \sqrt{(V_{bi}+|V_a|)}$$

$$C_{dep} = \frac{dQ}{dV} = \left(\frac{\epsilon}{W_{dep}}\right) \text{ per-unit-area}$$

⇓

Template Capacitor

∴ Called as

Varactor Diode

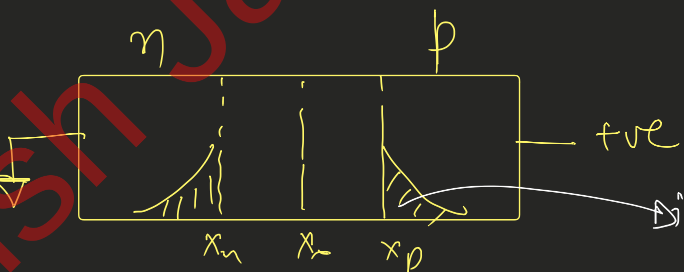
$$\simeq V^{-n}$$

for ideal Cx ; $w \propto V^{1/2}$
$n = 1/2$

$$\therefore \ C \propto \frac{\epsilon A}{w} \propto V^{-1/2} \propto V^{-n}$$

②

in forward Bias



integrate this profile to get charge here

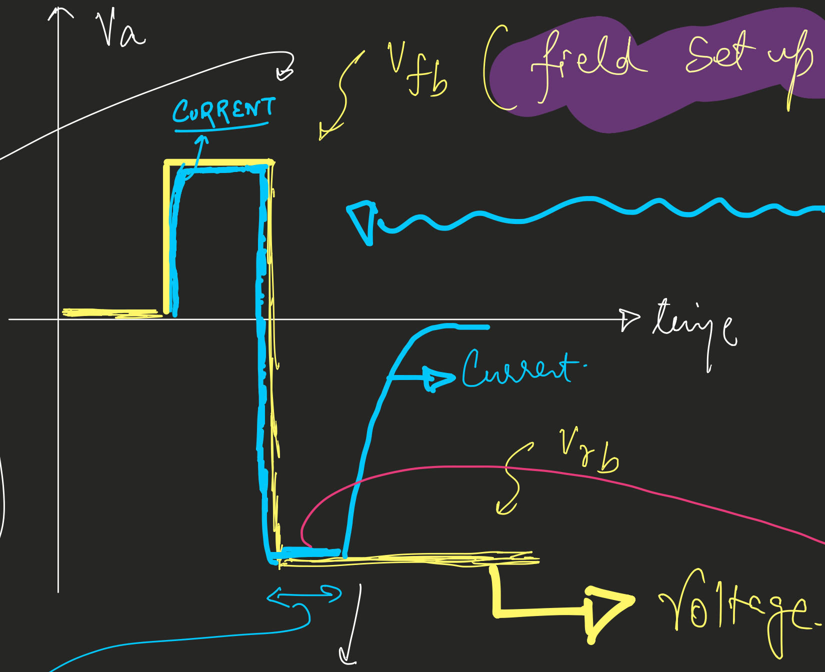
$$\Delta p_n = p_{no}\left(e^{V/V_T}-1\right)$$

$$Q_1 = \int_{x_p}^{\infty} \Delta n_p \, dx$$

$$Q_2 = \int_{-\infty}^{x_n} \Delta p_n \, dx$$

minority charges on P & n sides respectively

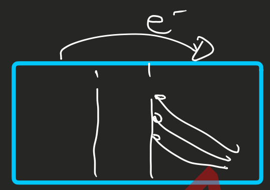
#



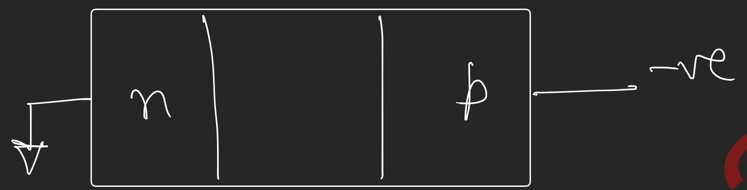
V_{fb} (field set up instantaneously)

almost there inst. (very little delay)

TURN ON TRANSIENT



this is the time when stored charges gets eliminated



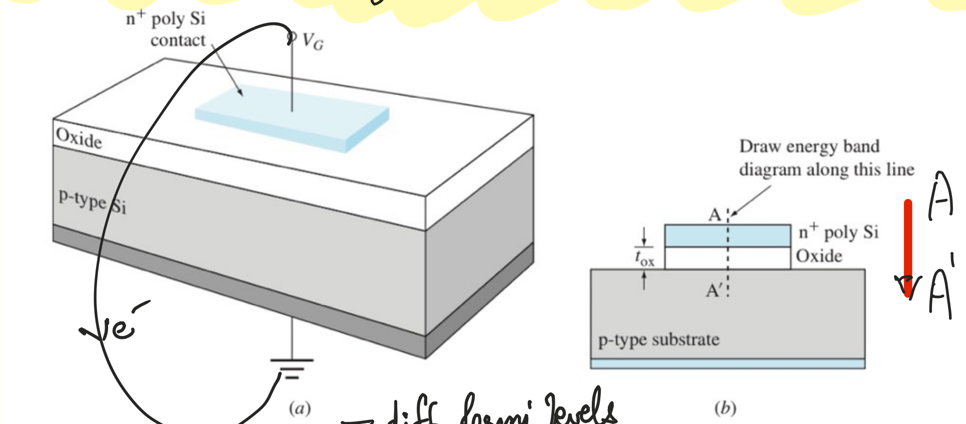
TURN OFF TRANSIENT.

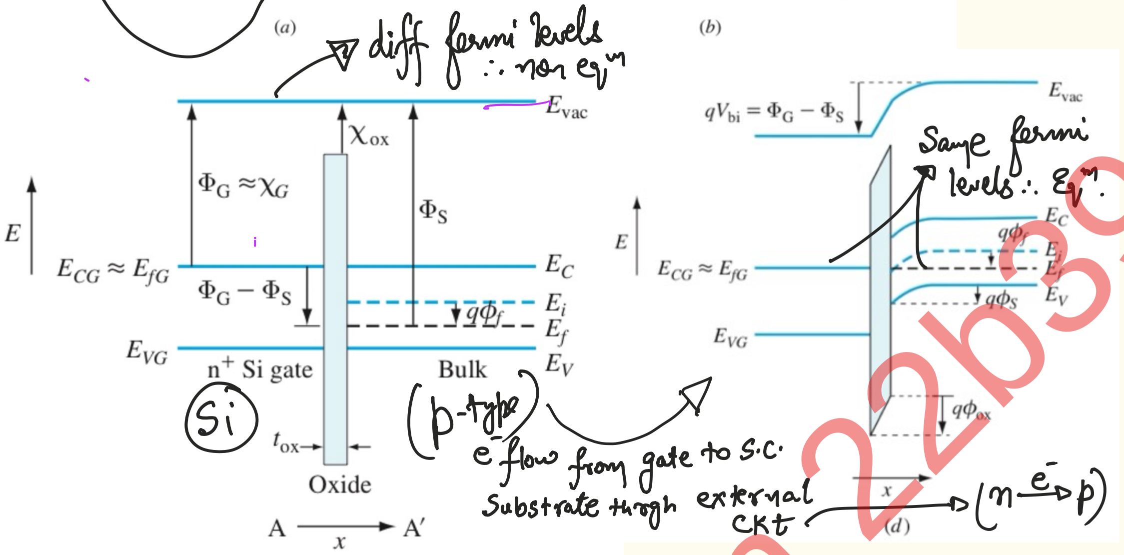
e^- & h^+ are dragged out

↳ as a large E.F. is set up due to reverse Biased

e^- : $p \to n$ } due to large EF
h^+ : $n \to p$. }

General Mosfet Structure {p-type Substrate with n-type Silicon Gate}





ϕ_f :- $|V_{fermi} - V_{intrinsic}|$

ϕ_G :- V_{gate} / V_{metal}

ϕ_S :- $V_{semiconductor}$

Energy Band diagram with Charge Neutrality | Energy Band diagram at equilibrium → no Current flow.

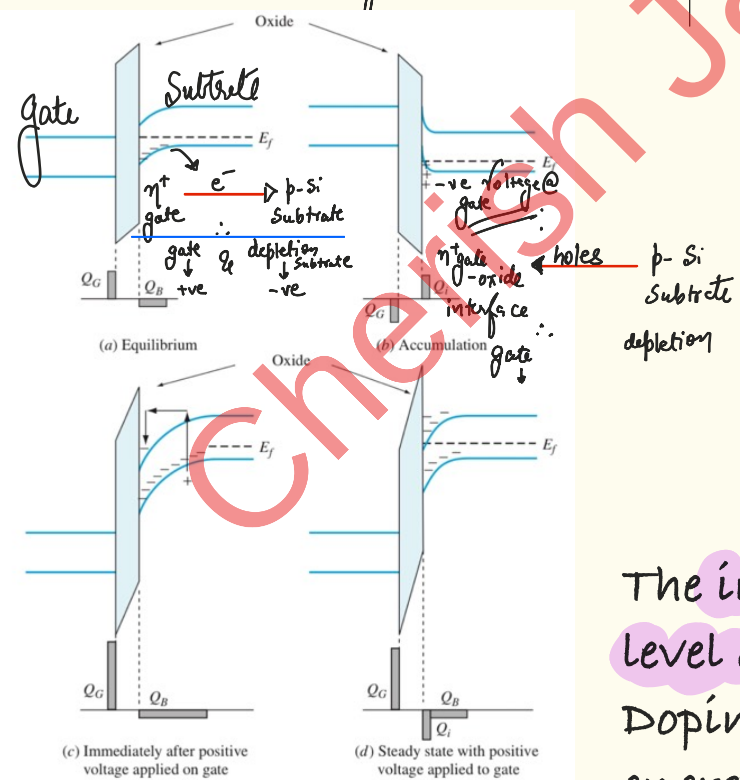


Figure 7.2 Energy band diagrams for the n^+-Si/oxide/p-Si capacitor of Figure 7.1 along with the charge distributions for three bias conditions. In (a) the case for equilibrium is indicated. Electrons from the n^+ gate transfer to the p-Si substrate, resulting in a positive gate and a negative depletion region in the substrate. The accumulation condition is indicated in (b). Here a negative voltage is applied to the gate with respect to the substrate such that holes accumulate at the silicon-to-oxide interface. The situation for a positive 2 V step voltage is shown in (c) immediately after the application of the voltage. With time, electrons generated in the transition region are trapped in the potential well at the interface until steady state is reach as indicated in (d).

Fermi level is sort of like the "sea level" of the Fermi sea which extends throughout the materials. Electrons flow when there is a difference in Fermi level between two different places, just like water flows when there is a difference in sea level. (disclaimer: limited analogy)

The intrinsic Fermi level is the Fermi level of an undoped semiconductor. Doping changes the distribution of energy states, thus the Fermi level depends on it and will generally not be the same as the intrinsic one.

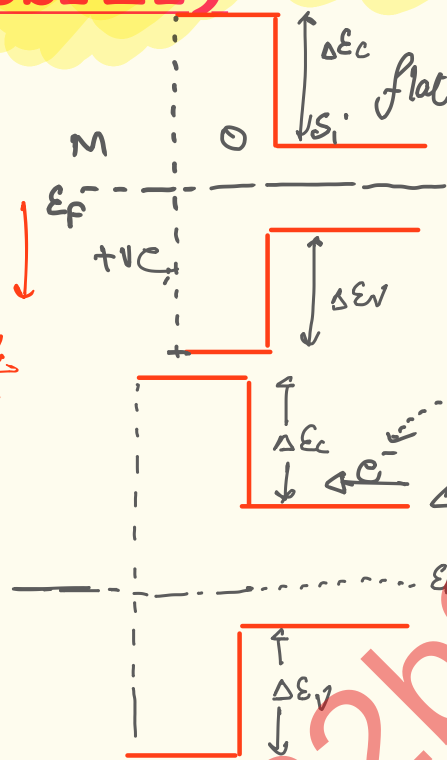
Metal oxide semiconductor field effect transistor (MOSFET)

M

SiO_2

Si

pulled down on applying +ve Bias



Flat Band Diagram

ΔE_c & ΔE_V = Const. Can't be changed

on apply +ve Bias

Silicon is p-type

On app +ve Bias ; e^- L ← R

Check Book → $\Delta E_c > \Delta E_V$.

$\Delta E_c + \Delta E_V \simeq 8eV$

$\Delta E_c = 4.5eV$

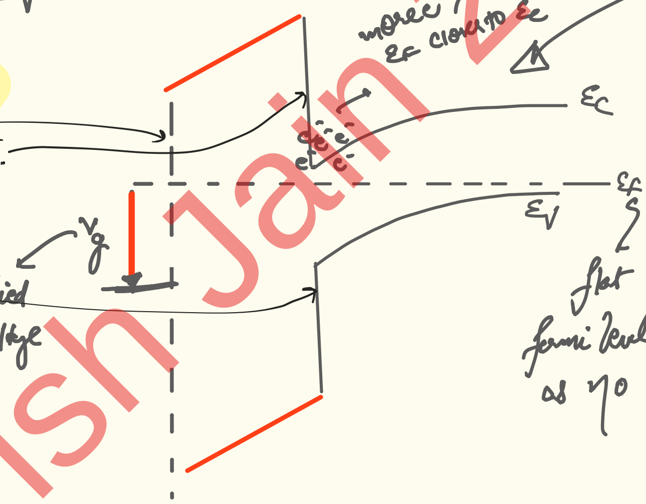
$\Delta E_V = 3.5eV$

$\Delta E_c > \Delta E_V$

V_{GS} directly applied on left so more bend on left as comp. to right. also e^- like to be near +ve V_{GS}

Hence if more e^- near this surface then it means conduction band near fermi level as compared to valence band.

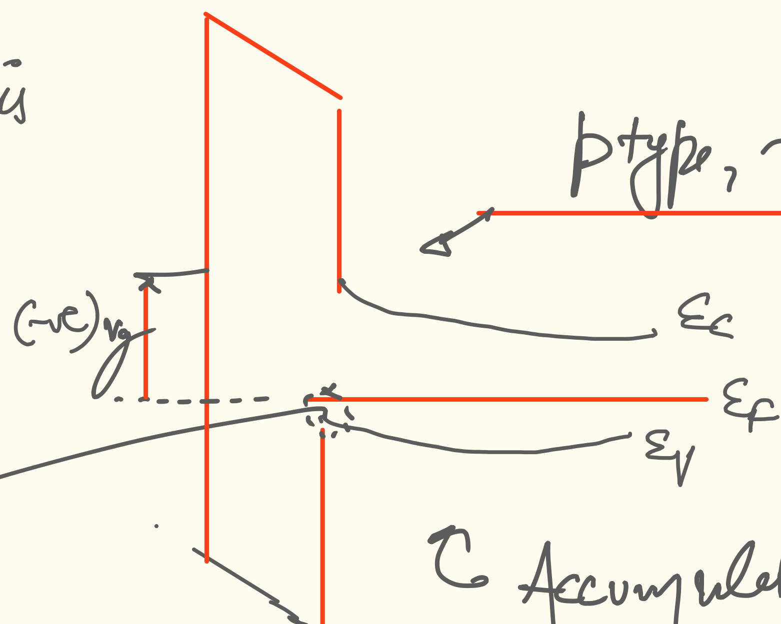
more e^-; hence E_F closer to E_c



This is k/a inversion [earlier]

flat fermi level as no current.

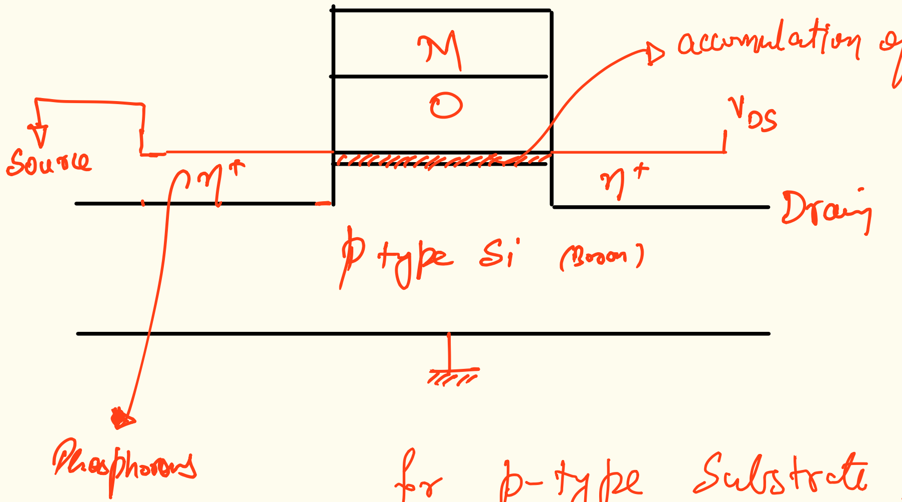
* Band Bending in accumulation is very small

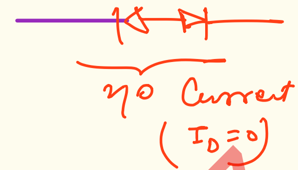


p type, -ve bias

→ Accumulation

more holes





for p-type Substrate ;

when $V_{DS} = +ve$
$V_{GS} = -ve$

then ; $I_{DS} = 0$

when $V_{DS} = +ve$
$V_{GS} = +ve$
$I_{DS} =$ finite.

for p-type ;

Accumulation (−ve) | Inversion +ve

* e^- Can Come in the Channel after a Threshold Voltage

$C_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}}$ per unit area

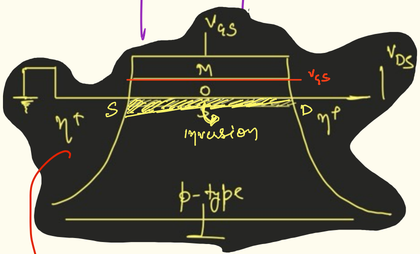
$Q = C_{ox} \cdot V_{GS}$ { assuming $V_{DS} = 0$ }

$Q_{inv} = C_{ox} \cdot (V_{GS} - V_T)$

$$\boxed{I_{DS} = f(V_{DS}, V_{GS})}$$

$Q = C_{ox} \cdot V_{GS}$

Some Characteristics of Mosfet



n- mosfet

n- FET

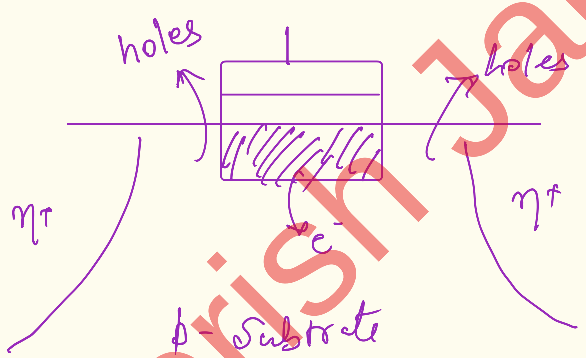
* for transistor
$n = 10^{18} cm^{-3}$
$\mu_n = 300 cm^2/V\cdot s$.

1. 4-Terminal Device
2. for n-mos; $V_S = V_{SUB} = 0$
3. V_T = Threshold Voltage = +ve
4. Enhancement mode
   $I_{DS} = 0$, $V_{GS} < V_T$
   Subthreshold region
5. $V_{GS} \geq V_T$; above threshold
   $I_{DS} > 0$
6. Source → Source the e^-
7. Drain :→ Drains the e^-
8. majority Carries Device w.r.t. S/D
9. Unipolar device
10. Heart of Device – mos Capacitor

Depletion Mode : $V_{GS} < 0$

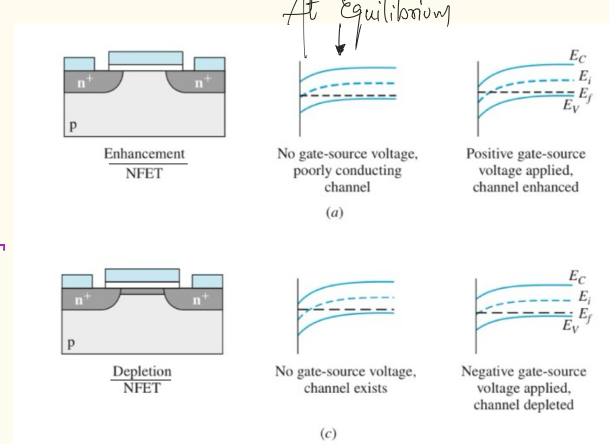
In Enhancement mode ; Current flows from Source Edge to Drain Edge

→ if it is not the Con ; then Current = 0



$n^+ - p - n - p - n^+$
Current = 0

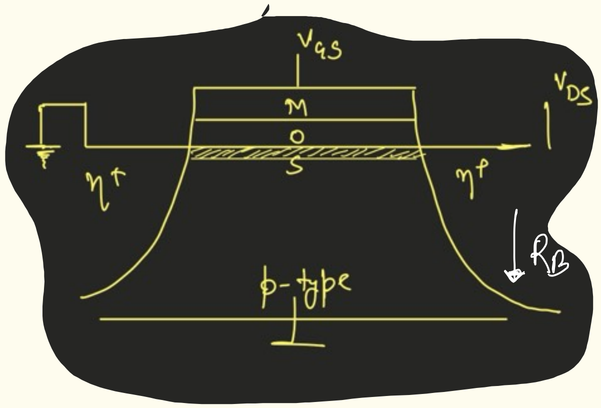
At Equilibrium



if longer gate length ;

Reverse Bias

$I_G = I_{sub} = 0$ → always due to oxide insulation irrespective of RB/FB



$I_G = 0 \ \forall \ V_{DS}$ & V_{GS} {cuz of oxide}

$I_{sub} = 0 \ \forall \ V_{DS}$ & V_{GS}

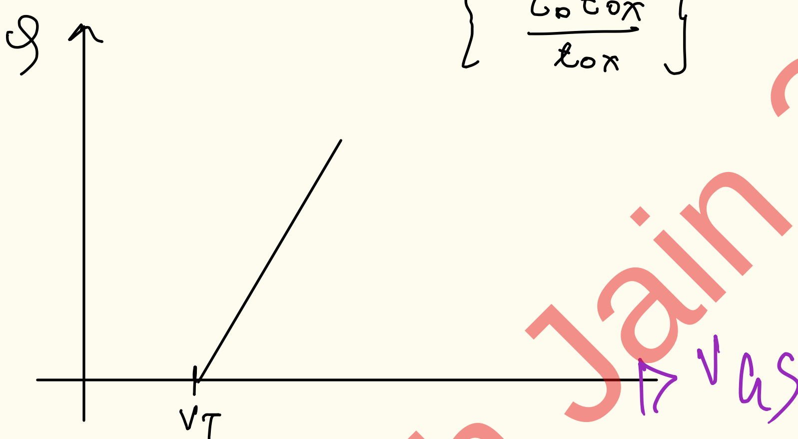
$I_{DS} = 0 \ \forall \ V_{DS}$ & $V_{GS} < V_T$

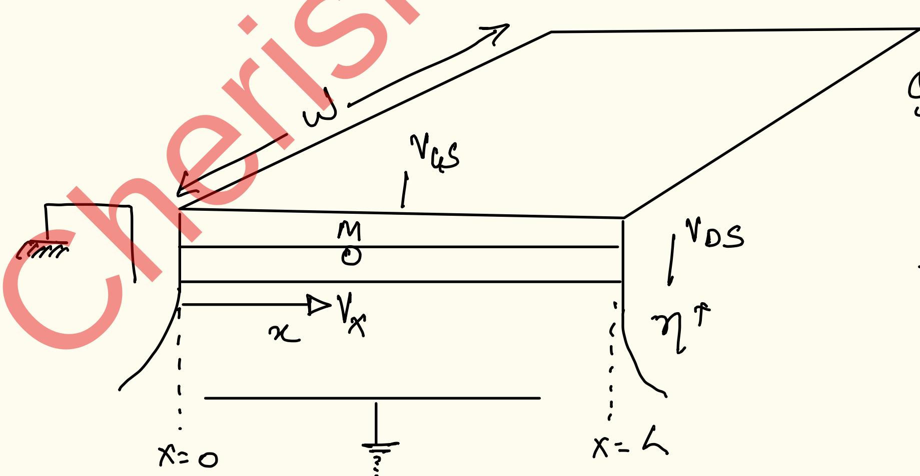
$I_{DS} \neq 0$ only when $V_{GS} > V_T$ & $V_{DS} = +ve$

* $Q = C_{ox}(V_{GS} - V_T)$ → Don't ask why V_T

↳ Capacitance/Area $\left\{ \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}} \right\}$

Overlap Capacitor





$Q = C_{ox}(V_{GS} - V_T - V_x)$

$I_{DS} = Q \, v_{el}$ —(1)

$I = \sigma E$
$= (nq\mu)E$
$= nqv$
$= Q \cdot v_{el}$ —(2)

By (1) & (2)

$$I_{DS} = Q v_{el} = \mu_n C_{ox} (V_{GS} - V_T - V_x) \cdot E$$
$$= -\mu_n C_{ox} (V_{GS} - V_T - V_x) \left(\frac{dV_x}{dx} \right)$$

$$\int_0^L I_{DS}\,dx = -\mu_n C_{ox} \int_0^{V_{DS}} (V_{GS} - V_T - V_x)\,dV_x$$

$$I_{DS} \cdot L = -\mu_n C_{ox} \left\{ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right\}$$

$$I_{DS} = -\mu_n C_{ox} \left\{ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right\}$$

now this is analysis of a 2D model; but as shown above it's a 3D model; so:-

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

So; $I_{DS} = f(V_{GS}, V_{DS})$

Valid if:-

1) $V_{GS} > V_T$ { not when $V_{GS} = V_T$ }

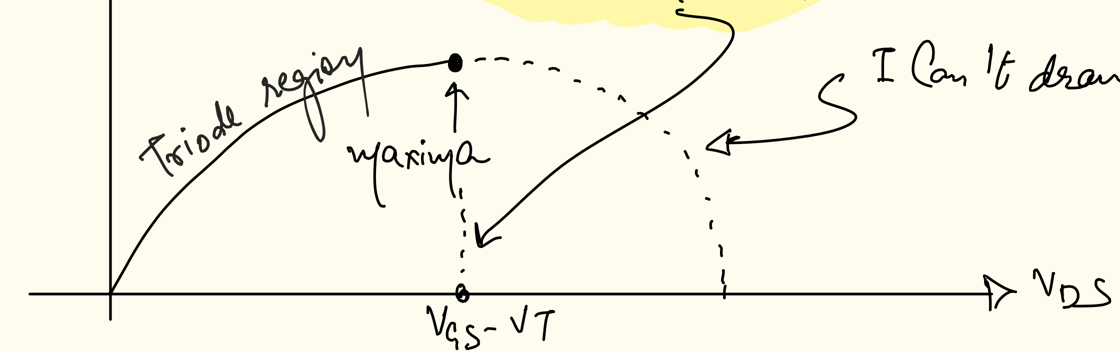
2) $V_{DS} > 0$

3) $V_{DS} < V_{GS} - V_T$

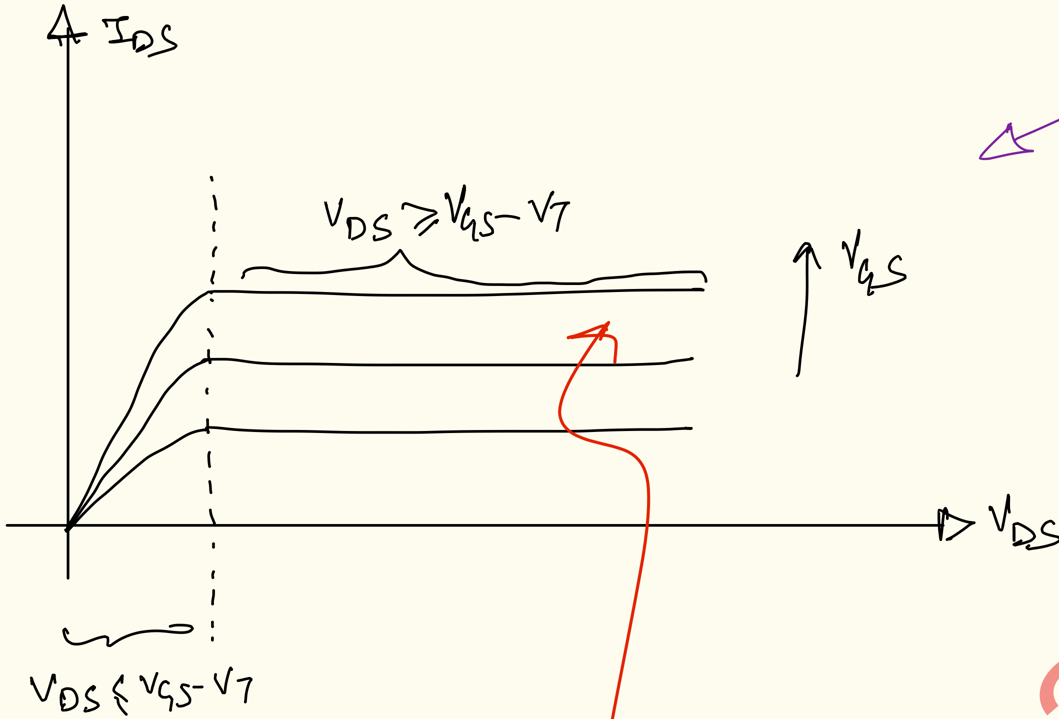
$$Q = -\underbrace{W C_{ox} (V_{GS} - V_T - V_x)}$$ → Should be +ve $\forall x$

@ $x = L$, $V_x = V_{DS}$

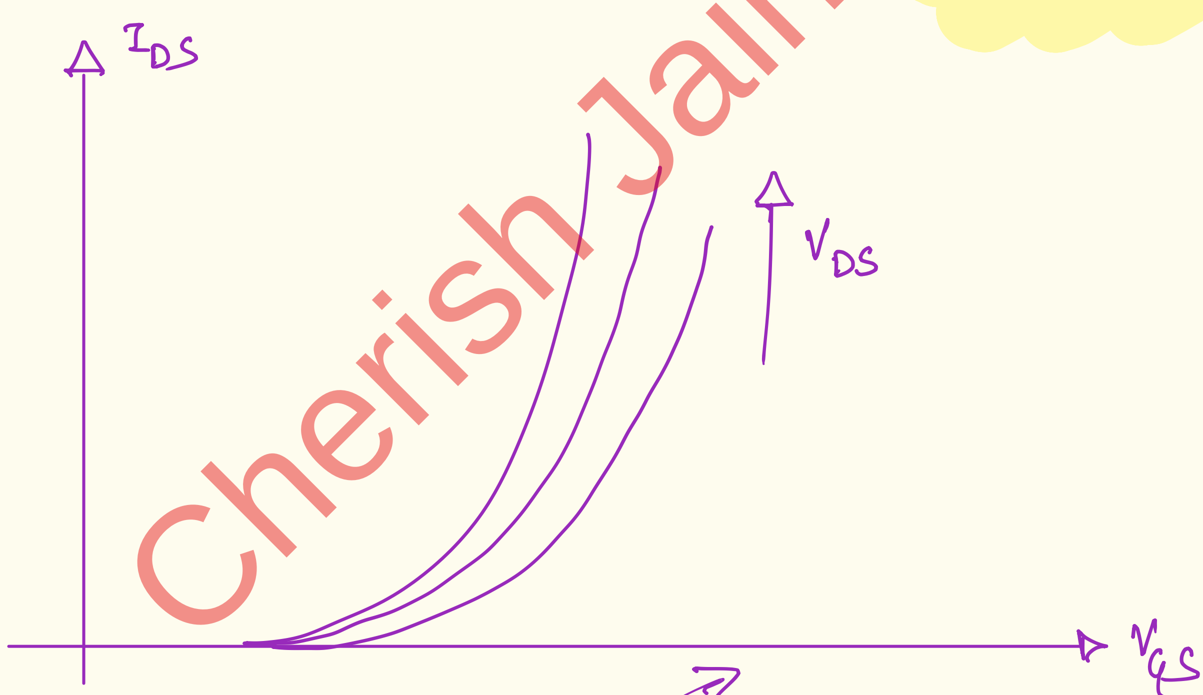
Hence $V_{DS} \leq V_{GS} - V_T$



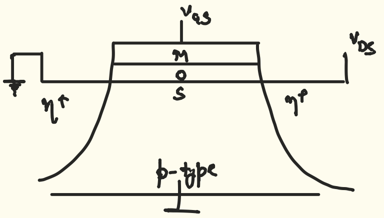
Output Characteristic



Here for Saturation region; $I_{DS} = \frac{\mu_n C_{ox} W}{2L}(V_{GS}-V_T)^2$

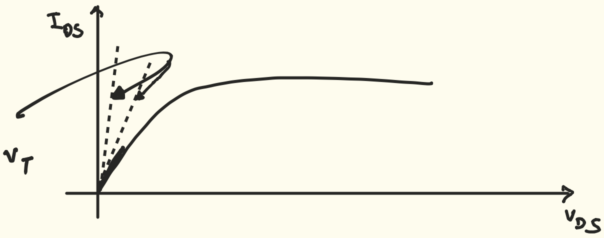


Transfer Characteristic



$$I_{DS} = \frac{\mu_n C_{ox} W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad ; \quad V_{DS} \le V_{GS}-V_T$$

$$= \frac{\mu_n C_{ox} W}{2L}\left[(V_{GS}-V_T)^2\right] \quad ; \quad V_{DS} > V_{GS}-V_T$$



Slope decided by $V_{GS}-V_T$

Case I :- $V_{DS} << V_{GS}-V_T$

$$I_{DS} \approx \frac{\mu_n C_{ox} W}{L}[V_{GS}-V_T]\, V_{DS}$$

(Linear Region)

* Voltage Variable Resistor

Case II :- $V_{DS} > V_{GS}-V_T$

$$I_{DS} = \frac{\mu_n C_{ox} W}{2L}(V_{GS}-V_T)^2$$

Independent of V_{DS}
(Saturation Region)
Also k/a Constant Current Region

Output parameters

$$\frac{\partial I_{DS}}{\partial V_{DS}} = 0$$

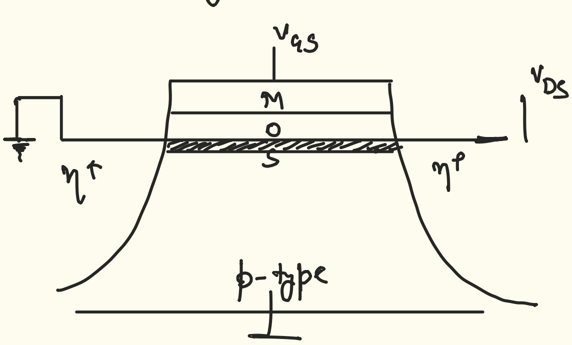
$\therefore$ Dynamic Conductance $= 0$ ~~(but $\frac{I_{DS}}{V_{DS}}$ = finite)~~

Dynamic Resistance $= \infty$

Case III :- $V_{DS} = V_{GS} - V_T$

$$\begin{cases} Q(x) = C_{ox}(V_{GS}-V_T-V_x) \\ Q(x=0) = C_{ox}(V_{GS}-V_T) & V|_{x=0} = 0 = V_S \\ Q(x=L) = 0 & V|_{x=L} = V_{DS} \end{cases}$$

\# Why Current saturates ?

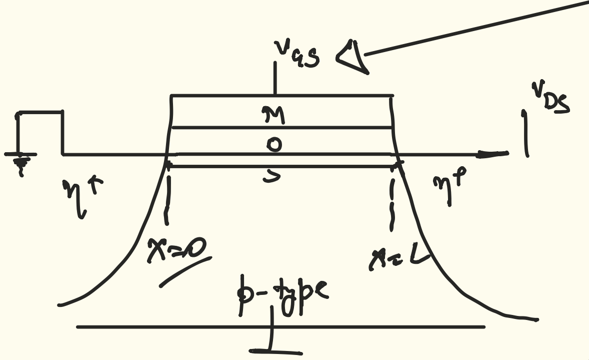


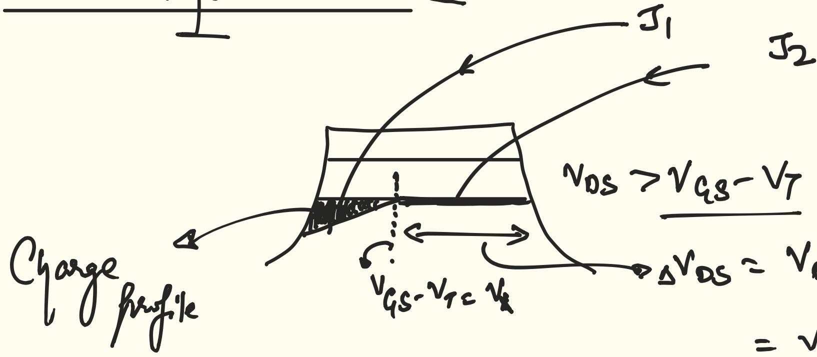
$$Q = C_{ox}(V_{GS}-V_T-V_{DS})$$

$$\Rightarrow Q > 0 \Rightarrow V_{GS}-V_T > V_{DS}$$

what happens when $V_{GS}-V_T < V_{DS}$

$$\rho(x) = C_{ox}\left(V_{GS} - V_T - V_x\right)$$



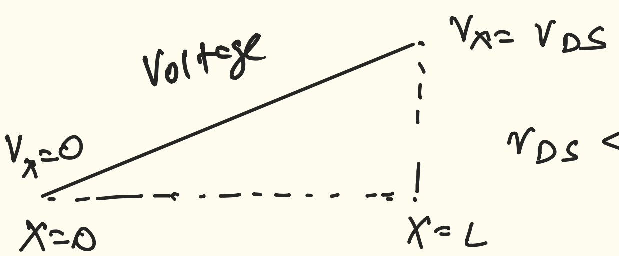


$V_{DS} > V_{GS} - V_T$

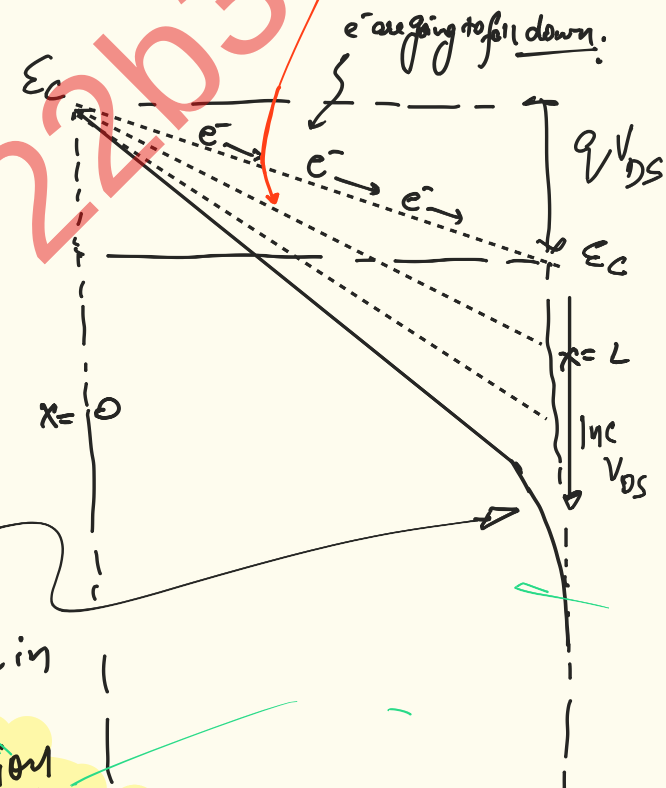
$$\Delta V_{DS} = V_{DS} - \underbrace{(V_{GS} - V_T)}$$
$$= V_{DS} - V_{DS,sat}$$

* Channel is pinched off.

E.F linear as $\left(\mathcal{E} = \frac{V_{DS}}{L}\right)$

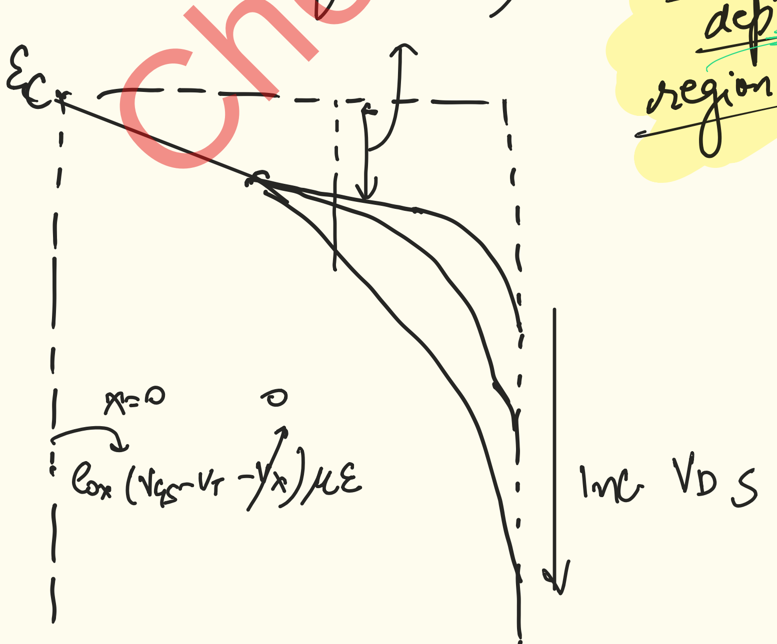


$V_{DS} \ll V_{GS} - V_T$

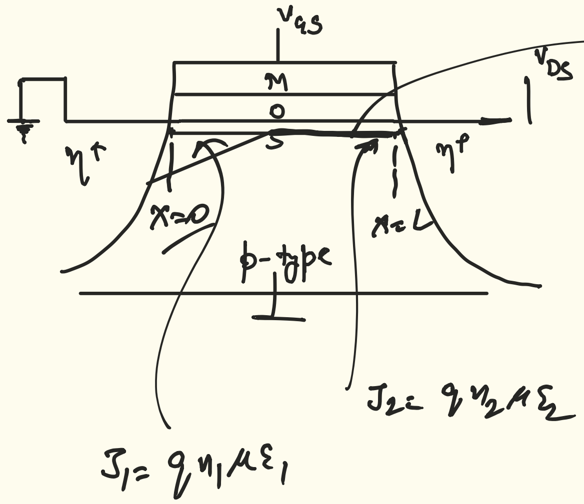


Parabolic Profile (like in a diode depletion region {Charge=0})

$q(V_{DS} - V_T)$



Beyond pinched off;
you can't change EF
or some charge

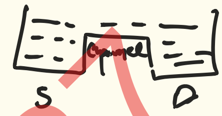


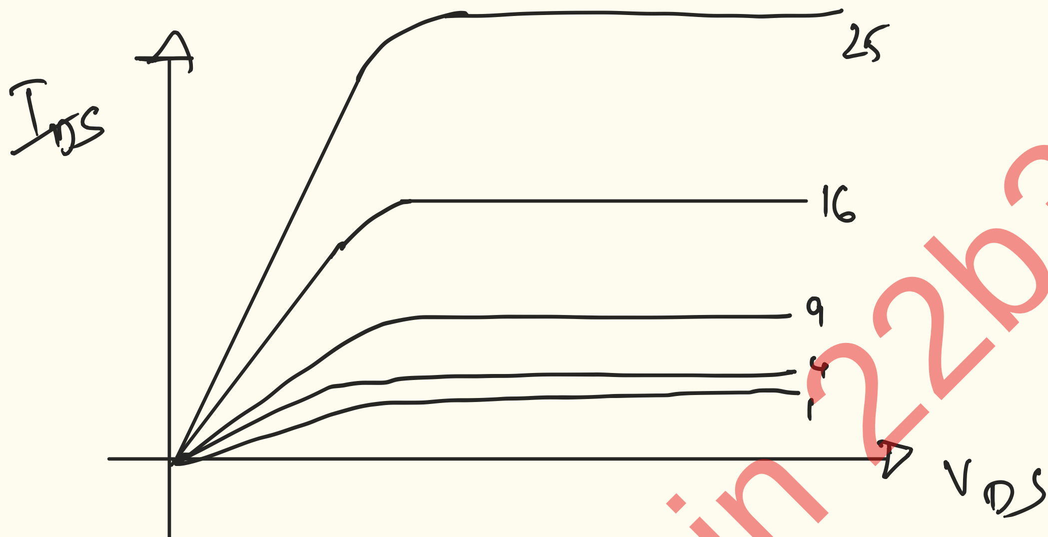
→ Current becomes Const once pinched off region starts

$n_1 >> n_2$

$E_1 << E_2$

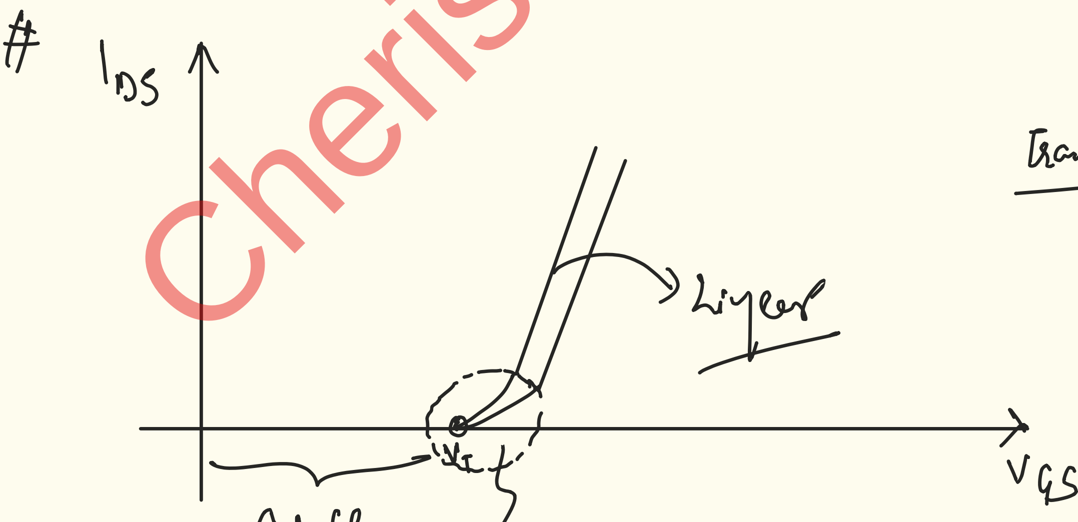
* Beyond pinchoff; Current is limited by Source injection.

{See  eg. from Book}



$$I_{DS} = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2$$

#



Transfer Characteristics

Cutoff

Saturation

$I_{DS} = 0$; $V_{GS} \le V_T$

$V_{DS} \geq V_{GS} - V_T$

Small Signal Analysis

$$I_{DS} = f(V_{DS}, V_{GS})$$

$$dI_{DS} = \frac{\partial f}{\partial V_{DS}} V_{DS} + \frac{\partial f}{\partial V_{GS}} V_{GS}$$

$V_{DS} \leftarrow$ Small Signal AC

$V_{DS} \leftarrow$ DC

$V'_{DS} \leftarrow$ DC + AC

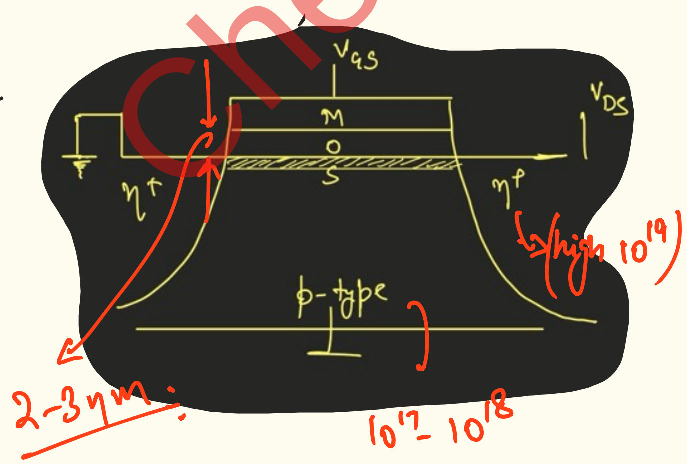
$$i_{ds} = \frac{1}{r_o} v_{ds} + g_m v_{gs}$$

level 1

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\mu_n C_{ox} W}{L}(V_{GS} - V_T)$$

$$r_o = \left[\frac{\partial I_{DS}}{\partial V_{DS}}\right]^{-1} \approx \infty$$

#



$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}}$$

we want $C_{ox} \uparrow$

C_{ox} is large

$$Q = C_{ox}(V_{GS} - V_T)$$

$$Q \uparrow \rightarrow J \uparrow$$

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$$

for SiO_2; $\epsilon_{ox} \simeq 3$