ECE 314/514 Digital VLSI Design
End Semester Exam
17-Dec-2022

Max Marks: **Duration: 90 mins**

Name _____ **Roll No.** _____

Instructions:

1. This is a closed book exam.
2. Use of calculators is allowed.
3. Question paper contains 11 questions. All questions are compulsory.
4. If you are making any assumptions, please mention them clearly in your sheet.
5. Institute plagiarism policy applies in this submission.

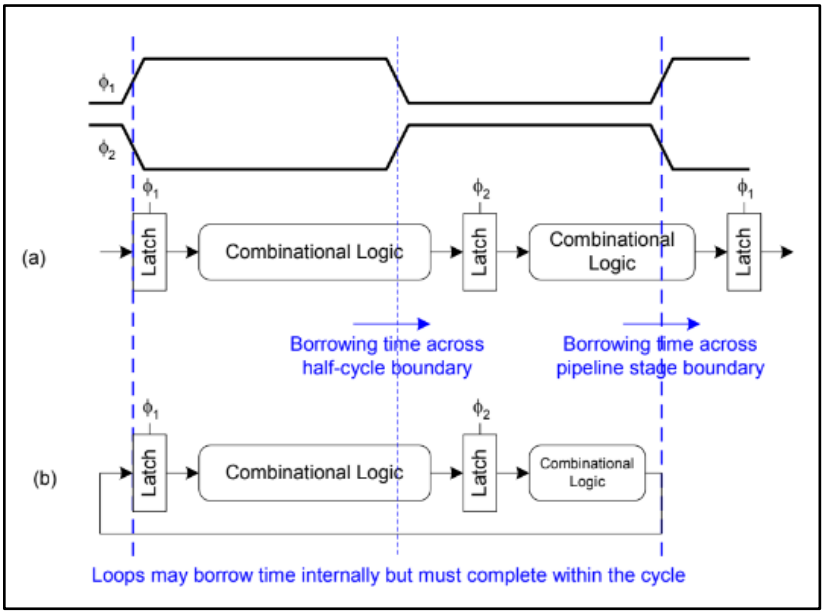
Q1.

a) What is time borrowing? What is the timing constraint in adjacent stages, so that latches can borrow time for a two-phase latch? Explain with the help of a timing diagram.
[2 Marks] (CO4)

b) How can we enable time borrowing in FF-based sequencing? [1 Marks] (CO4)

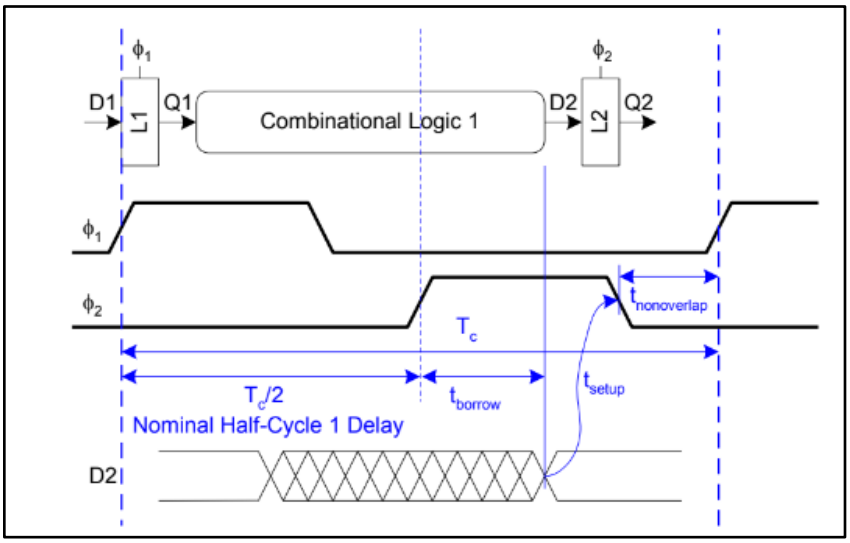
Ans a): Time borrowing is a method of gaining some extra time from the next cycle. It is used in sequencing circuits and helps satisfy the timing constraints. [0.5 Marks]

In (positive level) latches, we have “clock positive duration - setup” for sampling data. Therefore, previous stages, with long combinational paths have a larger window to satisfy the constraints of hold and setup.



[0.5 Marks]

Timing Constraint Explanation: The constraint in timing for time borrowing in latches is that the next logic will have less time as some of it's time has been borrowed by the previous stage. Hence, the next stage combinational logic block must have lesser delay.



[0.5 Marks]

The maximum amount of time that a two-phase latch-based system can borrow (beyond the Tc /2 – tpdq nominally available to each half-cycle of logic). Because data does not have to set up until the falling edge of the receiving latch's clock, one phase can borrow up to half a cycle of time from the next (less setup time and nonoverlap).

$$t_{\text{borrow}} \leq \frac{T_c}{2} - \left(t_{\text{setup}} + t_{\text{nonoverlap}}\right)$$

[0.5 Marks]

Ans b): We can enable time borrowing in FF-based sequencing with the help of useful skew. Like if the capture FF (later FF in sequence) clock (termed as capture clock) is delayed, then we will get more time for the combinational logic in between launch and capture FF, hence time borrowing in FF. [1 Marks]

Q2. Many exceptions are allowed in high density SRAM cells to recover area. List at least 2 such exceptions. Explain, why are such exceptions allowed only in memory arrays?
[2 Marks] (CO5)

Ans.

Any 2 out of the following few can be cited by the students to get required marks: [1 Marks, 0.5 per exception]

1. Long contacts are allowed to be made in memory cell layouts
2. DRC spacing between Poly and contact is violated
3. DRC spacing on minimum width of pMOS device is violated
4. DRC spacing to Nwell (from active) is violated
5. Minimum metal area (for metal-1) DRC is violated

6. Full enclosure of contacts by metal-1 (for long contact) is violated

They are allowed to be used because memory arrays are designed in a predefined pattern, and the optics can be adjusted through resolution enhancement techniques (RET). Hence, we can have predefined masks for memories allowing these violations. [1 Marks]

Q3.

a) If devices in a 6T SRAM cell are sized as follows in 65nm technology in the table below, which has better SNM, Write Margin and Leakage? [1.5 Marks] (CO5)

b) Which one of them is an overall better cell and why? [0.5 Marks] (CO5)

Cell-A	**PG = 180nm/ 65nm** **PU = 220nm/ 65nm** **PD = 100nm/ 65nm**
Cell-B	**PG = 180nm/ 70nm** **PU = 100nm/ 70 nm** **PD = 220nm/ 70nm**

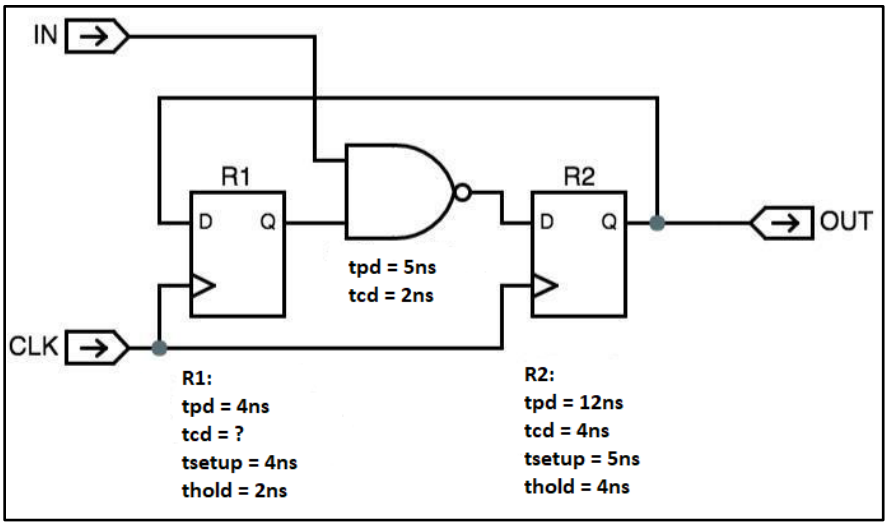
Ans.

Better SNM - Cell B [0.5 Marks]
Better WM - Cell A [0.5 Marks]
Better Leakage - Cell B [0.5 Marks]

Cell B is a better cell because it has better SNM and also lower leakage. Cell A will not even operate as a storage element because it has a worse PU ratio (>1.0), and also a bad PG-PD ratio. So, both write-ability and stability are compromised.

[0.5 Marks]

Q4. Consider the following sequential logic circuit. The timing specifications are shown below for each component.



(a) What is the value for the period of CLK (i.e., tclk) that will allow both registers in the circuit to operate correctly? [1 Marks] (CO4)

Ans.
For R1->R2: tclk>= tpd,R1 + tpd,NAND2 + tsetup,R2 = 4 + 5 + 5 = 14ns [0.25 Marks]
For R2->R1: tclk >= tpd,R2 + tsetup,R1 = 12 + 4 = 16ns [0.25 Marks]

The value for tclk : 16ns [0.5 Marks]

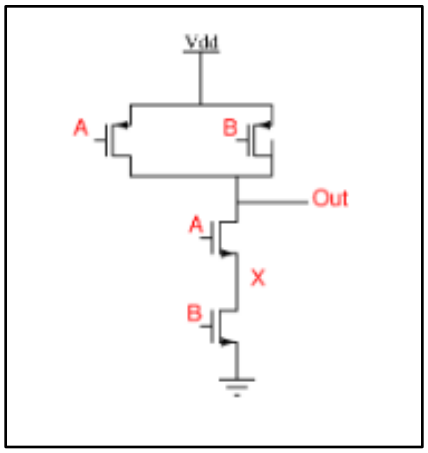
(b) What is the value for the tcd of R1 that will allow both registers in the circuit to operate correctly? [1 Marks] (CO4)

Ans.
For R1->R2: tcd,R1 + tcd,NAND2 >= thold,R2
tcd,R1 >= 4 – 2 = 2ns
The value for tcd of R1: 2ns [1 Marks]

Q5. Consider a generic two-input NAND gate. Arrange the following input sequences in the ascending order of the strength of the corresponding pull-down ability. Explain your result.

(a) A,B both shift from 0⇒1,
(b) A remains stable and B shifts,
(c) B remains stable and A shifts

[1.5 marks] (CO4)



Ans:

Consider the above schematic of a NAND gate.When both inputs shift from 0 -> 1, both the NMOS will be turned on, and a low resistance path will exist between the output node and the ground. So, this switching configuration will have the weakest pull-down network.
Next, consider the case when A is stable (at 1) and B switches later from 0 to 1. In this case, we see that node X is already at the same voltage (approximately) as the output node. Since the source node of the transistor connected to A has some voltage X, its threshold voltage changes slightly (body bias), and its current carrying capacity is slightly reduced. When B switches, there will be a low resistance path from X to GND
But, in the case when B is stable (at 1) and A switches from 0 to 1, node X is at 0, meaning that the body effect is nullified in this case, and A can more easily pass current from the output to the ground once it switches. Vt of the transistor connected to A is lesser than in the previous case; hence, it can pass more current and pull down the output quicker.

So, the pull-down abilities in increasing order are {both switching simultaneously, B switching later, A switching later} [0.5 marks for each scenario's explanation]

Q6.

a) List one advantage and a disadvantage of using a transmission gate based circuit?

[1 Marks] (CO4)

b) Draw a transmission gate/ Tri state-based positive edge triggered flip flop.

[1 Marks] (CO4)

Ans.

a) **Advantages**: (any one advantage - 0.5 Marks)

(i)Using a transmission gate instead of PMOS/NMOS in a circuit will remove the Vt drop issue.

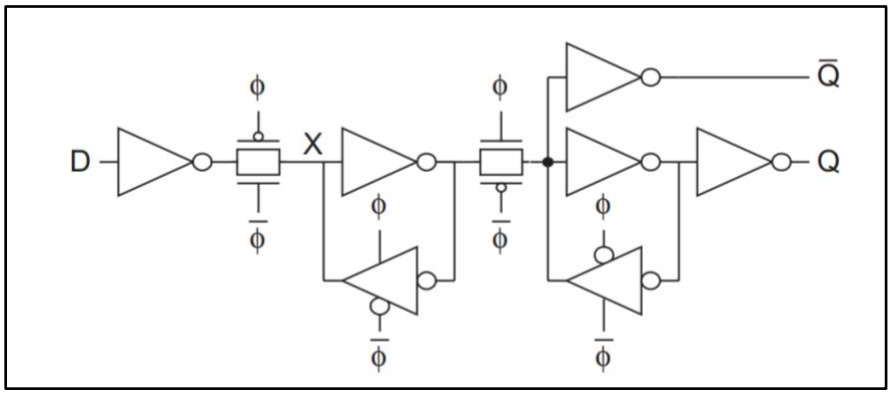
(ii)Transmission gates based circuits may be denser than static CMOS circuit

Disadvantages: (any one disadvantage - 0.5 Marks)

(i) When a long chain of transmission gates is used then this chain possesses a large RC which will increase the delay of the system and hence we use buffers in between to reduce the RC.

(ii) Transmission gates involve inputs at the S/D diffusion. This results in variable input load (as seen by the ckt driving transmission gate), and also problems of back-gate driving, etc.

b)



In both the latches lower tristate inverter can be replaced by an inverter and a transmission gate. [1 Marks]

Q7.

a) List any 2 challenges in using dynamic logic based circuits? [1 marks] (CO4)

b) How can these challenges be overcome? [1 marks] (CO4)

Ans. a) 1 mark for any two of the following

1) Charge leakage
2) Charge redistribution
3) Only 0 to 1 transitions allowed at input
4) Backgate Coupling
5) Clock Feedthrough

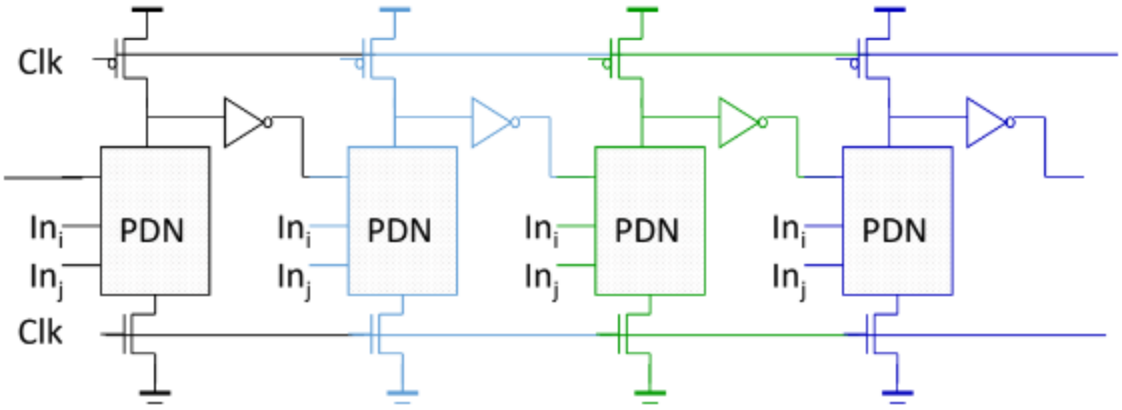
b) **1 mark for any two of the following**

1) Charge leakage can be compensated using a keeper and inverter circuitry.
2) Charge redistribution issue can be resolved by using keeper circuit at internal nodes
3) 0 to 1 transitions can be eliminated using an inverter
4) Using an inverter after the gate stack to isolate the floating node and output
5) Using an inverter after the gate stack to isolate the floating node and output

Q8.

a) Why can we remove the footer transistor in the domino logic without loss of functionality? [1 Marks] (CO4)

b) Assume that each of the following four dynamic gates shown in the figure have a delay of 100ps from input to output. Delay of the inverter is 50ps. Considering this circuit as an independent block and a clock duty cycle of 50%, what is the highest clock (CLK) frequency at which we can operate this circuit? [2 Marks] (CO4)



Ans.

(a) Since, in the domino logic, we connect the output of dynamic gates to the next stage of dynamic gate through an inverter. Therefore, the input of each stage is a rising logic which will rise only after the previous stage was evaluated. The footer is therefore not required as there is no discharge that is going to take place through the PDN before the previous stage is evaluated.

(b) As on the input stage, the inputs arriving may also be of falling nature, we cannot remove th footer.

(c) Delay from input to output: (100ps + 50ps)*4 = 600ps **[1 mark]**

Atleast this much time is required for evaluation of all the stages of this domino logic. Therefore high time of the Clk must be at least 600ps.

Time period of clock: 1200ps.

Highest frequency = (1/(1200 * e-12)) Hz = 833 MHz **[1 mark]**

Q9.

a) What is an accelerated life test? **[1 Marks] (CO5)**

b) List any 2 aging mechanisms leading to failure of chip. **[1 Marks] (CO5)**

Ans.

a) Accelerated life testing (ALT) is the process of testing a product by subjecting it to conditions (stress, strain, temperatures, voltage, vibration rate, pressure, etc.) in excess of its normal service parameters in an effort to uncover faults and potential modes of failure in a short amount of time. Applying stress speeds up ageing. ALT is done only on some samples of every lot. Health of these samples 'after ageing' determines if the other chips of the lot can be shipped to the customer. ALT accelerates age-testing and is needed because we can not afford to wait for failures to occur at their normal rate. [1 Marks]

b) Electromigration, Gate oxide breakdown, interconnect wearout, NBTI, PBTI, HCI
(Any two out of following, 0.5 Marks per mechanism)

Q10.

a) List any three sources of clock uncertainty. **[1.5 Marks] (CO4)**

b) How is clock skew different from clock jitter? **[1 Marks] (CO4)**

Ans. a) (Any 3 out of the following, 0.5 Marks for each source)

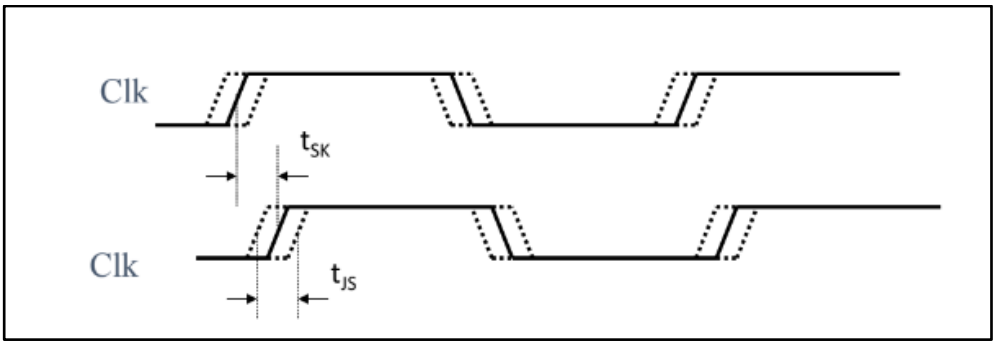
1. Clock Generation
2. Devices
3. Power Supply
4. Interconnect
5. Capacitive Load
6. Temperature
7. Couping to Adjacent Lines

b) **Clock Skew**: Skew comes from the differences in gate and wire delay. Variations in this delay cause clock to reach (arrive at) different elements at different times. Spatial variation in temporally equivalent clock edges.

In simplest words, Clock Skew is the time difference between the arrival of the same edge of a clock signal at the Clock pin of the capture flop and launch flop. Any signal takes some time to travel from one point to another. The time taken by the Clock signal to reach from the clock source to the clock pin of a particular flip-flop is called Clock latency. Clock skew can also be termed as the difference between the capture clock latency and the launch clock latency for a set of flops.

[0.5 Marks]

Clock jitter: Temporal variations in consecutive edges of the clock signal. The same flop with the same clock, but this clock acted differently over different cycles.



Here tsk is clock skew and tjs is clock jitter. [0.5 Marks]

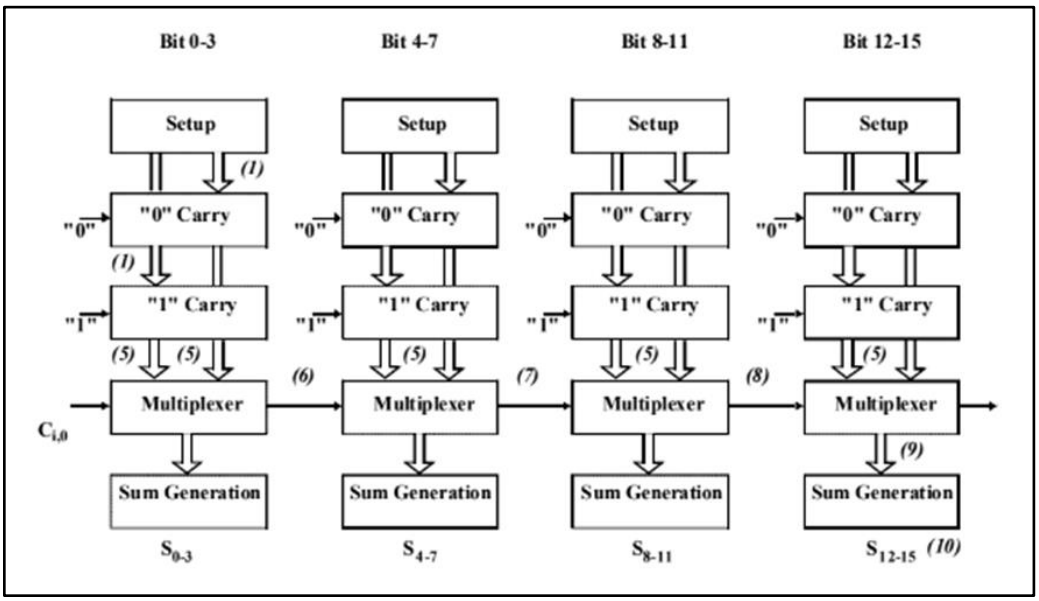
Q11.

Linear Carry Select and Square root carry select adders are shown in the figure below.

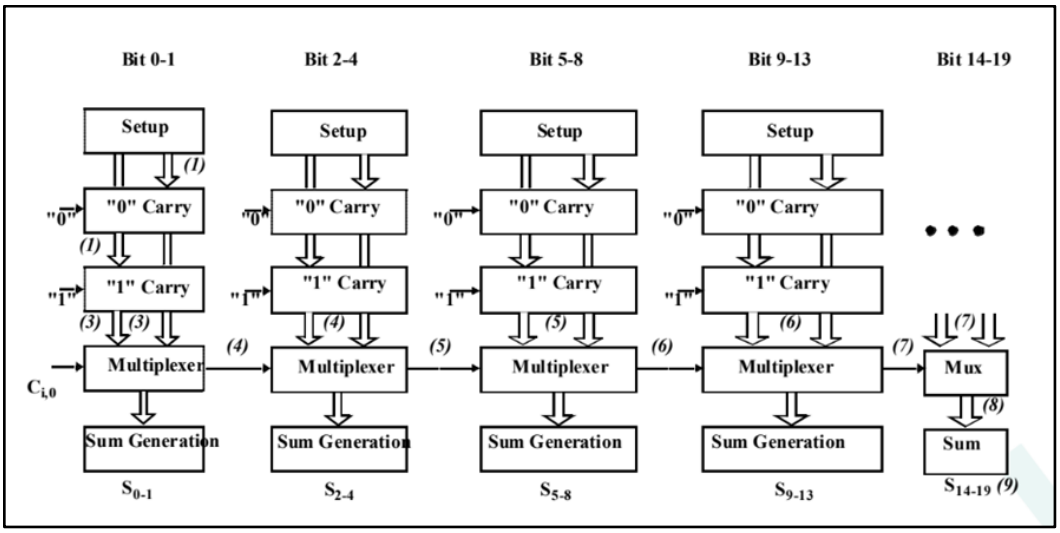
a) **Identify the critical path for the two circuits (redraw the circuit in your answer-script). [2 marks] (CO5)**

b) **Calculate the delay for both adders for 16-bits. Assume delay of Setup and sum-generation blocks to be 1 unit. Assume the delay of Multiplexer to be 0.5 units. Assume the delay of Carry per bit is 1 unit. [1 Marks] (CO5)**

Linear Carry Select Adder:



Square Root Select Adder:

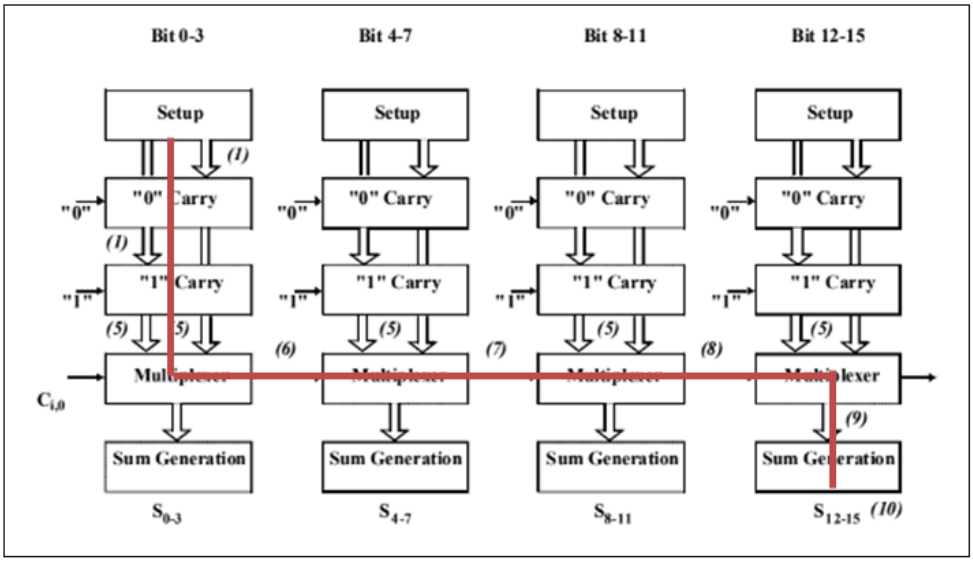


Ans a)

Linear Carry Select Adder:

In the last stage of the carry ripple adder, we have to wait for the carry to ripple through and then produce the sun outputs. So to decrease the wait time, in linear carry select adder, we double the hardware, evaluate the sum and carry for both Cin=0 and Cin=1 and keep it ready. The main idea here is to improve the performance without concern about the power consumption and area.

In every stage of the Linear Carry Select Adder 4-bits are used. For carry to propagate to the multiplexer 4 ripple adder for Cin=0 and 4 ripple adder for Cin=1 are used parallelly. So a total of (4*tcarry) units of delay will be available at the multiplexer. Red-line indicates the critical path.



[1 Marks]

For Linear Carry Select Adder, the Setup block will take 1 unit delay, and the Carry generation block will take 4 unit delay because 4-bit requires four ripple adders each of 1 unit delay, and then the multiplexer block will take 0.5 unit delay. There are 4 multiplexer blocks in the critical path so a total of (4*0.5) 2 units delay. Then finally sum generation block will take 1 unit delay.
Hence $\boldsymbol{t_{add} = 1 + 4 + 2 + 1 = \ 8\ units.}$

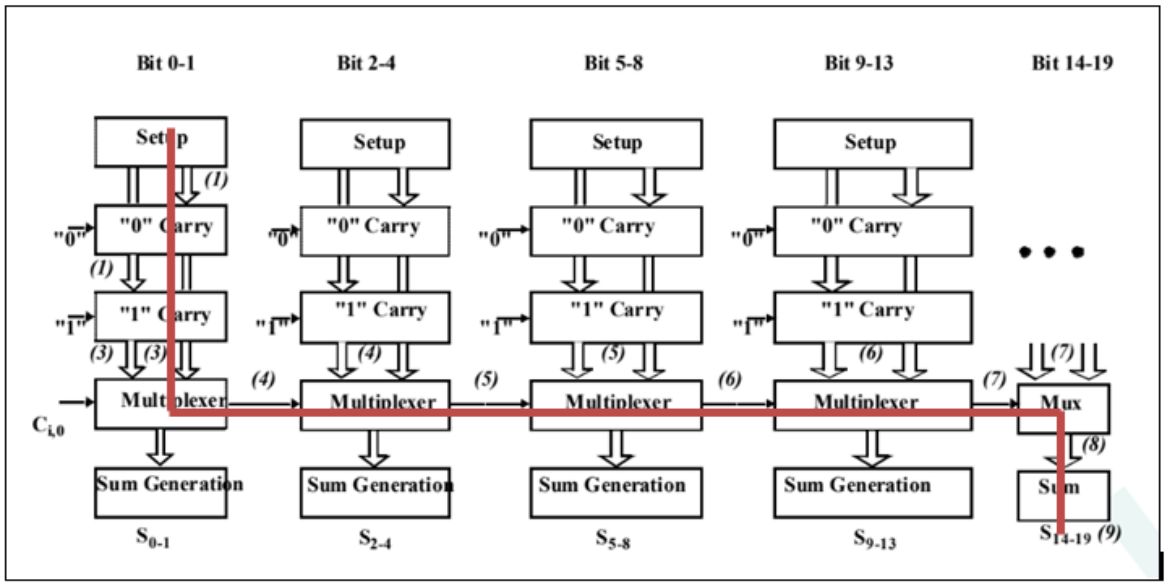
OR

General Equation:

$$\boldsymbol{t_{add} = t_{setup} + Mt_{carry} + (N/M)t_{mux} + t_{sum}}$$

$\boldsymbol{t_{add} = 1 + 4 * 1 + (16/4) * 0.5 + 1 = \ 8\ units}$ [0.5 Marks]

Square Root Carry Select Adder:
In Linear Select, the last stage would have generated, and this Carry 0, and 1 would have been ready, but for the carry to arrive it is going to take forever. The gap is linearly increasing. Therefore the signal is ready to evaluate, but it is just waiting. To overcome this problem, equalize the arrival times at the multiplexer; instead of using uniform bits, each block has increasing bits. So we are starting with the least number, which is 2 bits, and have a 2-bit ripple adder so that now after setup, ripple through only two stages (2*tcarry+tsetup) and arrival time at the multiplexer at the first stage is (t1=2*tcarry+tsetup+tmux). Similarly, the subsequent block has a 3-bit ripple adder, so after setup, ripple through only three stages (t2=3*tcarry+tsetup). The t1 and t2 times will be equal so that there is no wait time for the signal.



[1 Marks]

For Square Root Carry Select Adder, the Setup block will take 1 unit delay, and the Carry generation block will take 2 unit delay because 2-bit requires two ripple adders each of 1 unit delay, and then the multiplexer block will take 0.5 unit delay. There are 5 multiplexer blocks in the critical path so a total of (5*0.5) 2.5 units delay because for 16-bit adder we have to go till 19 bits as bits are in increasing order. Then finally sum generation block will take 1 unit delay.
Hence $\boldsymbol{t_{add} = 1 + 2 + 2.5 + 1 = 6.5\ units.}$

OR

General Approximate Equation:
Here the starting block has M bits and corresponding blocks have M+1, M+2, and … bits. Let's say there are P such stages.

$$N = M + (M+1) + (M+2) + \ldots\ldots + (M + (P-1))$$
$$N = M(P) + P((P-1)/2))$$
$$N = P(M + ((P-1)/2))$$

$N \sim P^2/2$ => $P = \sqrt{2N}$

$\boldsymbol{t_{add} = t_{setup} + Mt_{carry} + Pt_{mux} + t_{sum}\ where\ P = \sqrt{2N}}$

$\boldsymbol{t_{add} = 1 + 2 * 1 + (\sqrt{2 * 16}) * 0.5 + 1 = 6.83\ units}$ [0.5 Marks]