CSE 112: Computer Organization
Quiz 3 Rubric
Set A

Ans 1.

Register	**Instruction number that writes to the specified register**	**Instruction number that reads from the specified register**
R6	1	2
R5	2	3
R9	3	4
R1	5	6
R8	4	5

(0.4 + 0.4 + 0.4)*5 = 6 Marks

Ans 2.

a. For processor A, time required = 25 µs/instruction*8 instructions = 200 µs **(1 Mark)**
b. For processor B, clock duration= max (5,3,10,6) = 10 µs **(1 Mark)**
c.

	1	2	3	4	5	6	7	8	9	10	11
add r1, r2, r3	S1	S2	S3	S4							
sub r4, r5, r6		S1	S2	S3	S4						
add r2, r15, r3			S1	S2	S3	S4					
add r6, r3, r9				S1	S2	S3	S4				
sub r5, r7, r8					S1	S2	S3	S4			
add r15, r11,r13						S1	S2	S3	S4		
add r10, r11, r12							S1	S2	S3	S4	
sub r14, r11, r13								S1	S2	S3	S4

(1.5*8 = 12 Marks)

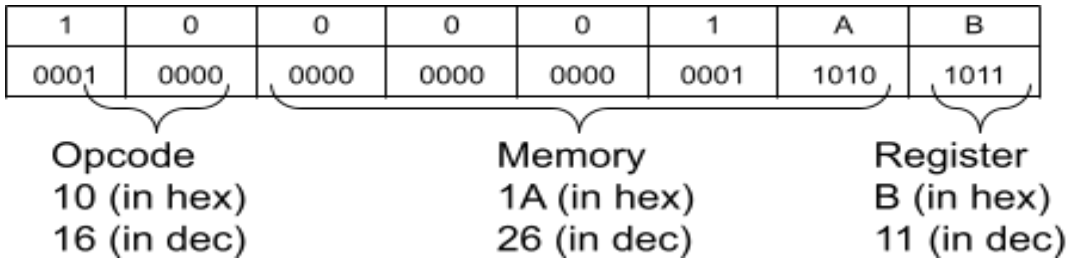
d. For processor B, time required = 11 cycles* 10 µs/cycle = 110 µs **(1 Mark)**
e. Speed up = 200/110 = 1.82 (approx.) (Accepted answer range: 1.80 to 1.84) **(1 Mark)**

Ans 3.

a. 32 unique instructions -> 5 bits to represent opcode **(1 Mark)**
b. 16 registers -> 4 bits to represent each register uniquely **(1 Mark)**
c. 1 MB -> 2^(20) locations -> 20 bits to represent each memory address uniquely
d. Filler bits for memory type = 32 - (5+ 20+4) = 3 **(0.5 Marks)**

Filler bits for register type = 32 - (5+ 4+4) = 19 **(0.5 Marks)**

e.



(1*3 = 3 Marks)

Ans 4.

Instructions	**Stack Value**	**Value of register after 'POP'**
PUSH R1	5	
PUSH R2	5,6	
POP R3	5	R3 = 6
PUSH R4	5,7	
POP R5	5	R5 = 7
POP R4		R4 = 5
PUSH R7	21	
PUSH R4	21,5	
PUSH R9	21,5,11	
POP R10	21,5	R10 = 11
POP R11	21	R11 = 5
POP R12		R12 = 21

For each value of register after POP instruction, there is one mark **(1*6 = 6 Marks)**.

Set B

Ans 1.

Register	**Instruction number that writes to the specified register**	**Instruction number that reads from the specified register**
R8	1	2
R5	2	3
R6	4	5
R4	5	6
R7	3	4

(0.4 + 0.4 + 0.4)*5 = 6 Marks

Ans 2.

a. For processor A, time required = 20 µs/instruction*8 instructions = 160 µs **(1 Mark)**
b. For processor B, clock duration= max (5,3,10,6) = 10 µs **(1 Mark)**
c.

	1	2	3	4	5	6	7	8	9	10	11
add r1, r2, r3	S1	S2	S3	S4							
sub r4, r5, r6		S1	S2	S3	S4						
add r2, r15, r3			S1	S2	S3	S4					
sub r5, r7, r8				S1	S2	S3	S4				
add r6, r3, r9					S1	S2	S3	S4			
add r10, r11, r12						S1	S2	S3	S4		
add r15, r11,r13							S1	S2	S3	S4	
sub r14, r11, r13								S1	S2	S3	S4

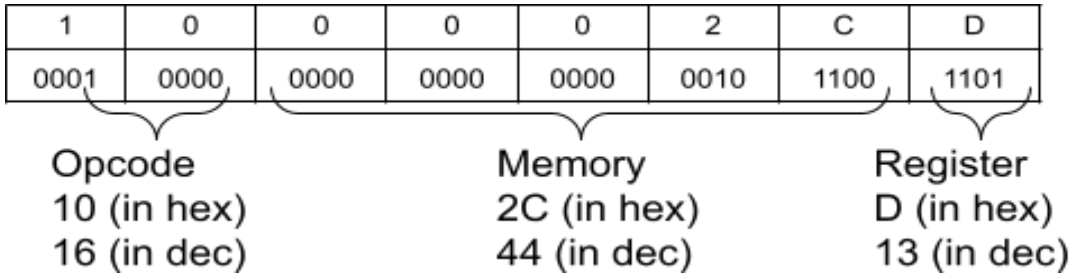
(1.5*8 = 12 Marks)

d. For processor B, time required = 11 cycles* 10 µs/cycle = 110 µs **(1 Mark)**
e. Speed up = 160/110 = 1.45 (approx.) (Accepted answer range: 1.42 to 1.48) **(1 Mark)**

Ans 3.

a. 32 unique instructions -> 5 bits to represent opcode **(1 Mark)**
b. 16 registers -> 4 bits to represent each register uniquely **(1 Mark)**
c. 1 MB -> 2^(20) locations -> 20 bits to represent each memory address uniquely
d. Filler bits for memory type = 32 - (5+ 20+4) = 3 **(0.5 Marks)**
   Filler bits for register type = 32 - (5+ 4+4) = 19 **(0.5 Marks)**

e.



(1*3 = 3 Marks)

Ans 4.

Instructions	**Stack Value**	**Value of register after 'POP'**
PUSH R1	2	
PUSH R2	2,3	
POP R3	2	R3 = 3
PUSH R4	2,5	
POP R5	2	R5 = 5
POP R4		R4 = 2
PUSH R7	21	
PUSH R4	21,2	
PUSH R9	21,2,10	
POP R10	21,2	R10 = 10
POP R11	21	R11 = 2
POP R12		R12 = 21

For each value of register after POP instruction, there is one mark **(1*6 = 6 Marks)**.