Quiz1
CSE/ECE 511 Computer Architecture

INSTRUCTIONS:

Total Marks = 20
Time Duration = 30 mins solving + 10 mins uploading

1. **The duration of the exam is 30 mins, and 10 mins for scanning and uploading the solutions. No further extension of time will be given regarding this. Any late submission will be awarded 0 marks.**
2. **The question paper will be uploaded in google classroom. Do not forget to turn it in. Solutions submitted by any other means (email etc.) won't be considered for evaluation.**
3. **Students are required to switch on their cameras and mute themselves. Make sure you are sitting in a well-lit room so that we are able to see your faces clearly. If you are not clearly visible, you will be awarded 0 marks.**
4. **The answers should be in your own handwriting and submission should be in PDF format only.**
5. **Write any assumption clearly, if any. Needless to say, only reasonable assumptions will be considered if any ambiguity is found in the question.**
6. **During the exam, if you have any queries, write them in the meet chatbox. It will be taken into notice by us. Don't unnecessarily unmute your mic for it creates a disturbance to others.**
7. **Calculators are NOT allowed during exam time. ONLY use pen and paper for writing the exam.**
8. **Students need to be present and visible for the whole exam duration (till the end of solution uploading time) even if they upload the solution before time.**
9. **NAMING CONVENTION - <Name>_<Roll number>_Q1.pdf.**
   Example Abc_Def_2020123_Q1.pdf
10. **Show your calculations and justifications in each question.**

GOOD LUCK !!

Q1.

Specifications	Processor 1	Processor 2
ISA Name	P1	P2
IPC (Instructions per cycle)	5	4
Clock rate	500MHz	300MHz

MIPS = Million Instructions per second

Based on the specifications given above, answer the following questions:

a. Find $MIPS_{(Processor\ 1)}$ and $MIPS_{(Processor\ 2)}$. Show your calculations.
b. Suppose that the number of instructions in the high level code when compiled on ISA P1 is 1000. If the high level code runs in the same amount of time in ISA P2 as well, find the number of instructions in the benchmark when it was compiled for ISA P2. **[2+3=5 Marks]**

Q2. Draw the pipeline diagram (consider a 5 stage pipeline as F, D, E, M, W) for the instructions that follow. Every stage takes 1 cycle.

A. When there is no bypassing. Also, state the total number of cycles required to execute the below code.
B. When there is a full bypassing. Also, state the total number of cycles required to execute the below code. **[5+5=10 Marks]**

1. LD R1, 1(R0)
2. ADD R4, R3, R1
3. ADD R3, R5, R1
4. SUB R0, R4, R3
5. SUB R0, R8, R1

Q3 Consider an ISA which has **32bit** long instructions. There is only one type of instruction.
Type A: **<Y bit opcode> <X bit address> <5 bit register>**
Type A instructions have 3 fields: the opcode, a memory address, and a register.
Suppose the ISA supports the address space of **4MegaBytes**, with byte addressable memory.
Given this, answer the following questions:

a. How many bits are used to represent an address in this ISA?
b. Determine **X**?
c. Determine **Y**?
d. What is the maximum number of registers that this ISA can support?
e. What is the maximum number of instructions that this ISA can support?

[1+1+1+1+1 = 5 Marks]