DVD - Monsoon 2021 - Quiz 2

92 responses

What do you mean by velocity saturation? What is the effect on drain current due to this? (2+2)

92 responses

When a charge carrier(lets say an electron) achieves maximum velocity in the presence of very high electric fields in a semiconductor, that is when it's called saturation velocity. This is described as a velocity saturation of the semiconductor.

The channel electrical field reaches a critical level when the drain to source voltage is increased, which leads to velocity saturated carriers at the drain.

Due to variation in voltage applied at the drain , and also due to the channel length , electric field gets affected , now as electric field changes , velocity of electrons increases or decreases accordingly , now when electric field is too high , velocity becomes to high , so it starts colliding with the ions and hence velocity tends to saturate eventually , after a point increasing Vds has no affect on velocity of electrons because it has saturated.

Now, in short channels due to velocity saturation Id (drain current) decreases. Because as length decreases , electric field increases , and velocity is saturated much earlier.

As we increase Vd, the electrons start moving towards quickly. After a certain velocity,

What is the benefit of using dual damascene process?

87 responses

By using dual damascene , we make metal contact as well as via both at the same time , so many steps of the process reduce, hence yield loss decreases..

It helps reduce the number of steps in the process.

Dual damascene process basically allows us to deposit via and metal in one go (both being copper). Using this process we save a step of having to separately add Aluminium and Tungsten. This allows means that we are able to get rid of the misalignment errors errors that creep in due to the earlier used 2-step procedure. Thus, it helps in preventing yield loss. It also reduces number of steps.

1. we can etch once and deposit the copper twice.and it reduces the cose significantly.2)copper is more good conductor the aluminum but just need to have a proper care to isolate from silicon

Dual damascene can be used to create copper interconnects which was earlier not possible with the traditional methods

In the C-V characteristics of a MOS capacitance, why do we obtain different capacitance value in the inversion region in the low frequency and high frequency of operation?

90 responses

Because in the higher frequency of operation, there is high resistivity, which inactive the minority carriers rapidly at the interface between oxide and semiconductor. and in low frequency the things gets reversed.

This is because at low frequency , changes in charges happen at the inversion layer , so dielectric length is tox.
Now , at high frequency , electrons are not able to leave the inversion layer , so the changes happen at the depletion layer boundary , so dielectric length is now tox+wd . Hence different capacitances.

For lower frequency, there is sufficient time for electrons to move from inversion layer to the substrate, so the effective dielectric thickness is t_ox, but in case of high frequency, the change is very quick, and electron is not able to move from the inversion layer to the substrate. Instead, electrons at the boundary of the depletion layer move to substrate, so the effective dielectric thickness becomes t_ox + Wd (maximum depletion region width) and therefore, the C-V characteristics are different for high and low frequency of operation

In the inversion region when we have high freq. this means that there is not enough

48 responses

In subthreshold conduction of MOSFET, the values of Subthreshold slope is given as 60mV/decade, 75mV/decade, 90mV/decade, 100mV/decade. Which of these is the preferred value for Subthreshold slope [1 Mark]. Explain briefly the reason behind your selection [1 Mark].

90 responses

60 mV/decade because that is ideal subthreshhold slope at room temperature

60 mV/decade is preffered.
beyond this we have bad slopes due to which , sub threshold current decreases .
hence we prefer 60mV/decade .

The preferred Subthreshold slope is 60mV/decade because we want a slope such that within 60mV, the current reduces by 1 decade

60mV/decade. This value means that for 60mV we are able to reduce the current value by one decade. So, basically we are achieving desired functionality at lesser value, means it's the better tech.

The preferred value is 60 mV per decade. The lower value of subthreshold slope means that the current in the subthreshold region (Vgs<Vt) should increase at the lowest rate possible, as the transistor is expected to behave as 'off' in the subthreshold region. Ideally, there should be a decade reduction in current for 60mV difference in voltage.