Quiz 3
CSE/ECE 511 Computer Architecture

INSTRUCTIONS:

Total Marks = 30
Time Duration = 30 mins solving + 10 mins uploading

1. **The duration of the exam is 30 mins, and 10 mins for scanning and uploading the solutions. No further extension of time will be given regarding this. Any late submission will be awarded 0 marks.**
2. **The question paper will be uploaded in google classroom. Do not forget to turn it in. Solutions submitted by any other means (email etc.) won't be considered for evaluation.**
3. **Students are required to switch on their cameras and mute themselves. Make sure you are sitting in a well-lit room so that we are able to see your faces clearly. If you are not clearly visible, you will be awarded 0 marks.**
4. **The answers should be in your own handwriting and submission should be in PDF format only.**
5. **Write any assumption clearly, if any. Needless to say, only reasonable assumptions will be considered if any ambiguity is found in the question.**
6. **During the exam, if you have any queries, write them in the meet chatbox. It will be taken into notice by us. Don't unnecessarily unmute your mic for it creates a disturbance to others.**
7. **Calculators are NOT allowed during exam time. ONLY use pen and paper for writing the exam.**
8. **Students need to be present and visible for the whole exam duration (till the end of solution uploading time) even if they upload the solution before time.**
9. **NAMING CONVENTION - <Name>_<Roll number>_Q3.pdf.**
   Example Abc_Def_2020123_Q3.pdf
10. **Show your calculations and justifications in each question.**

GOOD LUCK !!

Q1. Assume I2OI architecture with full bypassing and with in-order fetch, decode and issue; out-of-order execute and writeback; in-order commit. The pipeline has 4 functional units: ALU (1 cycle X0), Loads (2 cycles, L0 and L1), Store (2 cycle, S0 and S1) and multiply (4 cycles, Y0,Y1,Y2,Y3).

```
0: SUB    R1, R2, R3
1: SUB    R4, R1, R6
2: ST     R0, R8
3. MUL    R15, R17, R10
4: MUL    R7, R8, R15
5: LW     R18, R19
```

a)Show the pipeline diagram. [12 Marks]

b) Draw state of the scoreboard when instruction 3 and 5 are in issue stage of the pipeline. [8 Marks]

Q2 Write the MIPS instruction numbers corresponding to each VLIW instruction in the given table such that

1. Machine width is 2 i.e. can pack at most 2 RISC instructions to a single VLIW instruction.
2. You can reorder instructions as long as load and stores are not reordered relative to each other.
3. Independent loads and stores can be placed in the same VLIW instruction.
4. Pack instructions such that when more than one instruction can be placed in a given VLIW instruction, the instruction that comes first in the original RISC code is chosen. [10 Marks]

(01) SUB R1, R0, R0
(02) SUB R2, R0, R0
(03) LW R3, 0(R5)
(04) MUL R4, R2, R3
(05) MUL R6, R1, R2
(06) SUB R7, R1, R3
(07) LW R8, 0(R10)
(08) LW R9, 0(R11)
(09) SUB R15, R8, R9
(10) ADD R6, R4, R7

	MIPS Inst. No.	MIPS inst. No.
VLIW Instruction 1:		
VLIW instruction 2:		

The table is shown as a template. Expand the table if required.