ECE 314/514 Digital VLSI Design

Mid Semester Examination

3:00 PM 13-October-2020

Maximum Marks: 25 Duration: 1Hr

Instructions

1. This is a take home exam, you all should submit a single scanned pdf (high quality) in classroom, before the deadline.
2. You should definitely write your name, roll number, page number on your answer script.
3. You may choose to connect or not connect (to meeting) during the quiz.
4. If you are taking any assumptions, please mention them clearly in your sheet and must make them visible distinctively.
5. Upload the whole sheet (including the rough sheet used) to avoid any plagiarism.
6. Use of calculators is allowed.
7. Institute plagiarism policy applies in this submission.
8. There is a bonus question in the end. It is over and above 25 Marks, and it's not mandatory.
9. You can ask your doubts by joining regular class link to any of us. (Class link: https://meet.google.com/wvq-kpdv-aaw).
10. **The answer sheet must be uploaded in the classroom within 1Hr 20 Mins (before 4:20PM). 1Hr is for quiz and20 minutes for uploading.**

Q1. Answer the following **[10 Marks]**

a) Describe 2 challenges of using copper as an interconnect in advanced technology nodes. [2 Marks]

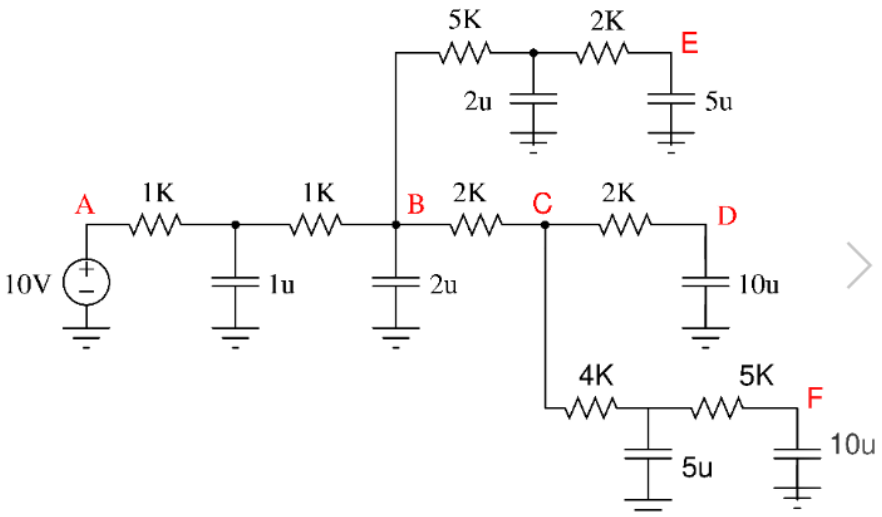
b) In a long combinational path, why do we prefer to design the combinational path in early stages and use buffers in final stages. [2 Marks]

c) Calculate the standard cell height in case of a 12-track library for a technology, where metal width is 0.18um and DRC is 0.20um. Explain with the help of a diagram. [2 Marks]

d) What is the reason behind the voltage spikes coming in inverter transient simulation when the input toggles. [Hint: You can explain using a MOSFET model] [2 Marks]

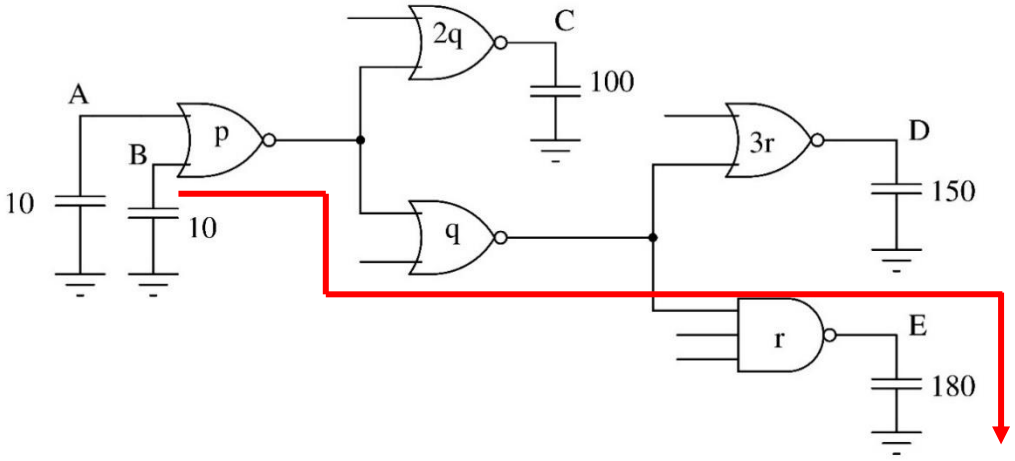
e) It is observed that after fabrication, performance yield on SS lots is very low. Describe any 2 post-fabrication steps that can be taken to recover the Yield at this lot [2 Marks]

Q2. Calculate the Elmore delay of path ABCF for the given RC network. **[2 Marks]**



Q3. For the given design. **[8 Marks]**

a) Minimum delay from B to E (Red highlighted path) [2 Marks]
b) Sizing for all the gates used p, q, r. [3 Marks]
c) Find the size (width) of NMOS and PMOS inside all the gates (in path). [3 Marks]



Q4. For a 2-input NOR gate. **[5 Marks]**

a) Size the circuit for same delay as an inverter. [1 Mark]
b) Make a stick diagram with shared diffusion. Consider, 1 finger for 2 units width of PMOS and 1 finger for 1-unit width in NMOS. [2 Marks]
c) Explain why you connected OUT, GND to specific regions in your stick diagram. [2 Marks]

[Bonus Question] - Optional

Q5. Why are substrate taps required at regular frequency in a layout [1 Mark]? Explain the consequence of not using them with the help of a diagram [2 Marks]

[3 Marks]

----------Best of Luck ----------