INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI

ECE 111 DIGITAL CIRCUITS

END-SEM EXAMINATION

Date: April 13, 2021 Max. marks: 120 Time: 11:00AM to 1:00PM

Q1. Implement the logic function F(A, B, C), characterised by truth table shown in Table 1 using minimum number of 2:1 multiplexers and logic gates.

Table 1

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Q2. For the logic circuit shown in Figures 1a and 1b, find the logical expression for outputs G and F.
The propagation delay of each gate is equal to τ. Plot the outputs G and F for both circuits, if the input is as given in Figure 1b for (a) τ = 0 and (b) τ = T s.
Do you find any difference in the outputs for the logic circuits of Figure 1a and 1b? If there is a difference, why is there a difference?

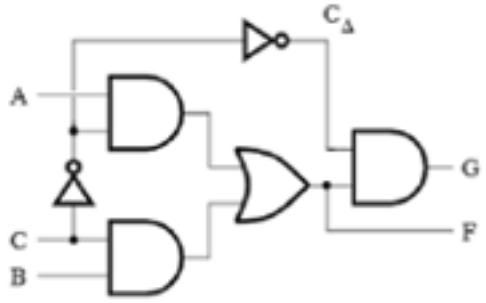

Fig. 1a

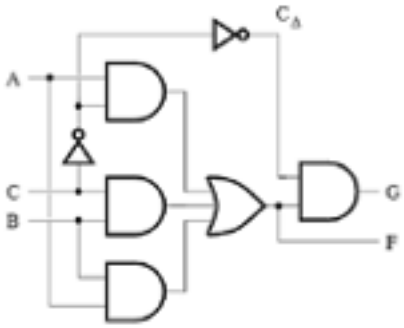

Fig. 1b

Fig. 1c

Q3. We wish to implement a 2-bit unsigned multiplier as per following specifications:

Inputs: $X = X_1 X_0$ and $Y = Y_1 Y_0$;
Output: $Z = X * Y$ where $Z = Z_3 Z_2 Z_1 Z_0$.
(a) Construct the truth table of multiplier.
(b) Determine the Boolean expressions for each output Z_i (i = 0, 1, 2, 3).
(c) Implement the multiplier using minimum number of basic logic gates.

Q4. A digital system works at a maximum frequency of 3MHz. However we have a clock signal at 18MHz. Give a circuit to generate a square wave of frequency 3MHz i.e., a wave with duty cycle 50%, from a signal of 18MHz. Identify the minimum total delay that each flip flop and the individual logic gates can have. Consider the hold time of the flip flop to be zero and the t_{setup} to be the same as $t_{clock\text{-}out}$ of the flip flop and the delay of the gates used is $0.5t_{setup}$ each. Design should avoid lock out.

Q5. A synchronous modulo 5 counter is to be designed. Assume a gate delay of τ seconds, a $t_{clk\text{-}out}$ delay of 3τ seconds, t_{setup} of 3τ seconds t_{hold} of 2τ seconds and t_{skew} of o seconds.

a) Design the counter using T-FF and gates of your choice and draw the circuit diagram.
b) Draw the timing diagram for six cycles for all the outputs and T inputs.
c) Calculate the maximum clock frequency that can be applied to this counter.

Q6. Design a synchronous circuit using $+^{ve}$ edge triggered D-FF with one external (primary) input X and one signal (primary) output Z. When X remains 1 for three successive clocks, the output Z goes to 1 on the third active clock edge. All other combinations of X and clock Z is 0 and the machine returns to the rest state. Identify, with proper justification, whether the machine will be a Moore or a Mealy machine. Draw the State Transition Diagram/Graph and design the state machine.

BEST OF LUCK