Quiz 2
CSE/ECE 511 Computer Architecture

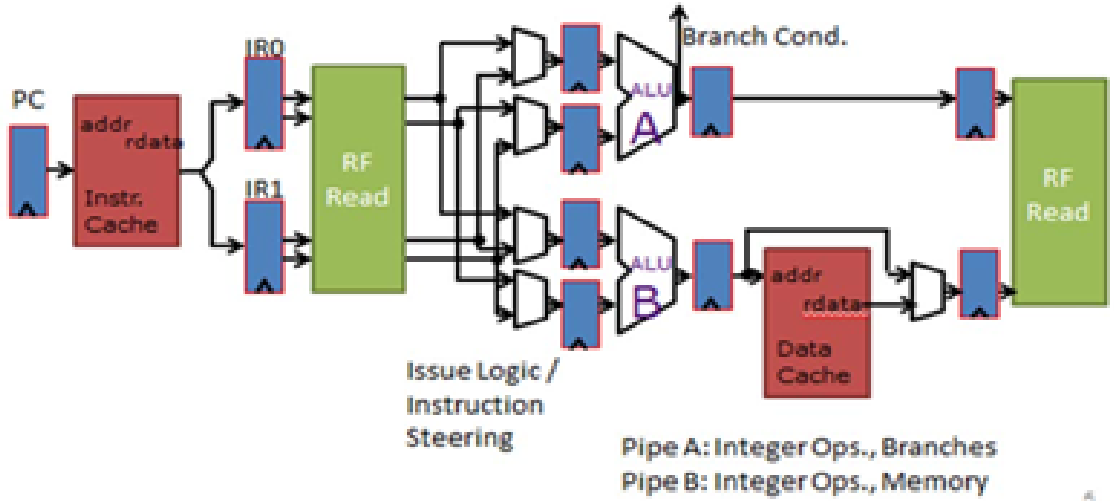
INSTRUCTIONS:

Total Marks = 30
Time Duration = 30 mins solving + 10 mins uploading

1. **The duration of the exam is 30 mins, and 10 mins for scanning and uploading the solutions. No further extension of time will be given regarding this. Any late submission will be awarded 0 marks.**
2. **The question paper will be uploaded in google classroom. Do not forget to turn it in. Solutions submitted by any other means (email etc.) won't be considered for evaluation.**
3. **Students are required to switch on their cameras and mute themselves. Make sure you are sitting in a well-lit room so that we are able to see your faces clearly. If you are not clearly visible, you will be awarded 0 marks.**
4. **The answers should be in your own handwriting and submission should be in PDF format only.**
5. **Write any assumption clearly, if any. Needless to say, only reasonable assumptions will be considered if any ambiguity is found in the question.**
6. **During the exam, if you have any queries, write them in the meet chatbox. It will be taken into notice by us. Don't unnecessarily unmute your mic for it creates a disturbance to others.**
7. **Calculators are NOT allowed during exam time. ONLY use pen and paper for writing the exam.**
8. **Students need to be present and visible for the whole exam duration (till the end of solution uploading time) even if they upload the solution before time.**
9. **NAMING CONVENTION - <Name>_<Roll number>_Q2.pdf.**
   Example Abc_Def_2020123_Q2.pdf
10. **Show your calculations and justifications in each question.**

GOOD LUCK !!

Q. Consider the in-order two-way superscalar processor in the figure. Each pipeline stage takes 1 cycle. Assume that branches execute in pipeline A, loads/stores in pipeline B. Fetch Unit can only fetch 2 instructions at a time. Means, both pipelines need to fetch simultaneously, else stalling will happen till both fetch units are free. The pipeline stages for pipeline A and B are denoted as (F, D, A0, A1, W) and (F, D, B0,B1, W) respectively. If for some reason, Writeback is stalled/delayed, then stall will be done in W stage and not in B1/A1. In case of no bypassing for RAW hazards, an extra cycle needs to be spent to decode the updated register values after the write-back stage.



[Figure of Two-Wide In-order Superscalar Processor Pipeline]

a. Draw pipeline timing diagram of the following code running on the above processor with no bypassing. Calculate how many clock cycles will be required to complete all the instructions. **[15 Marks]**

b. Draw pipeline timing diagram of the following code running on the above processor with full bypassing. Calculate how many clock cycles will be required to complete all the instructions. You are allowed to bypass between parallel pipelines. **[15 Marks]**

```
Inst1:   MUL R1   R2   R3
Inst2:   ADD  R4   R5   R6
Inst3:   ADD  R7   R4   R8
Inst4:   SUB   R9    R10 R11
Inst5:   LD     R12  0(R1)
Inst6:   LD     R13  0(R2)
Inst7:   SUB   R3    R4   R5
Inst8:   ADD  R13  R3   R6
Inst9:   LD     R7   0(R1)
Inst10: MUL  R14 R15  R7
```