DVD Quiz 3 Rubric

Q1. There are two wires with their dimensions shown in the Fig.1 below. The current direction is shown by the black arrow. If the ratio of their resistances R_Wire1 : R_Wire2 = 3:2 . Find the ratio of their sheet resistances. [1 marks]

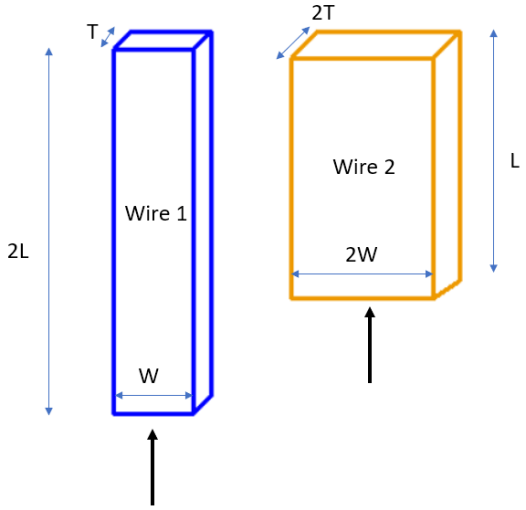


Fig. 1

Soln:

*R_Wire1 = R_sheet_Wire1 * 2L/W*

*R_Wire2 = R_sheet_Wire2 * L/2W*

R_Wire1: R_Wire = 3 : 2

R_sheet_Wire1 : R_sheet_Wire1 = 3 : 8 [binary marking 1 marks if answer is correct]

Q2. What is the height of a standard cell in a 12 track library with the following specifications. : [2 marks]

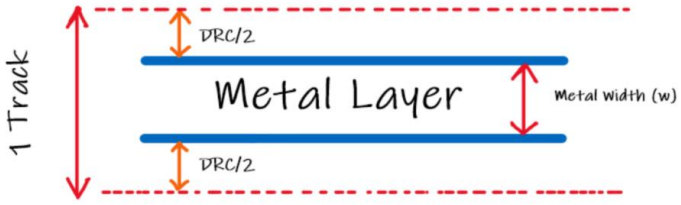
Min metal1 width = 0.09u

Min metal2 width =0.1u

Min spacing between two metal1 = 0.09u

Min spacing between two metal2 = 0.1u

Soln:



Track height is defined with respect to Metal2 layer so we have to use the Metal2 width and spacing(DRC). *[0.5 marks]*

*Track pitch = 1 Track height = Metal track width + 2 * Half DRC* *[1 marks]*

*Track pitch = 0.1u + 2 * (0.1u/2) =0.2u*

*12 track height = 12 * Track pitch = 2.4u* *[0.5 marks]*

Q3. Given below is the stick diagram(rough layout sketch) for a circuit.

Identify the circuit. How can you improve it ?(Draw the modified stick diagram). List two advantages as compared to the given stick diagram? [1 + 1.5 +1]

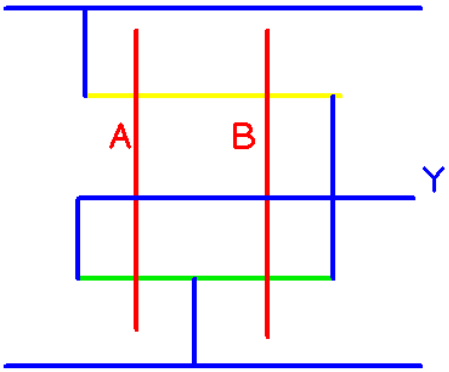
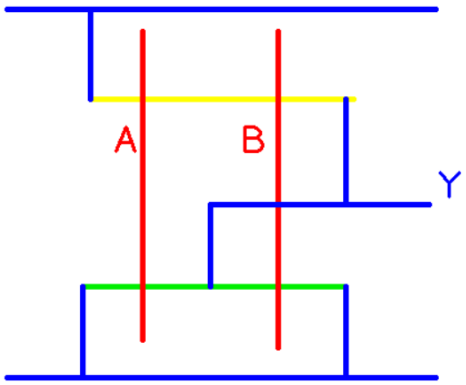


Fig.2

Soln:

The stick diagram represents the layout of a NOR gate *[1 marks]*

If the output Y is taken from the shared S/D region, then the diffusion capacitance at the output would reduce. *[1.5 marks]*



Advantages of the modified layout:

Lesser output capacitance due to sharing of the sources , so

delays are reduced *[0.5 marks]*

Lesser power (dynamic) as ½(CV^2) reduces. *[0.5 marks]*

Or any other valid reason

Q4. Given below in Fig. 4 is an NMOS with I as input and Y as output . Fig. 5 shows an unfingered NMOS version of Fig. 4 and Fig.6 shows 2- fingered version of same NMOS.

Given,

Width of the NMOS in Fig. 5, W= 0.5u

Lex = W/4

Wnew =W/2 (as the same transistor is broken in two fingers)

Lo= Lex * 1.25

Side wall capacitance of region 'A' = 0.4fF/um

Bottom capacitance of region 'A' = 0.5fF/um^2

a) Find the diffusion capacitance of region A, B , C and D [2.5 marks]
b) Where should you connect output Y in Fig 5 and Fig 6. [1 marks]

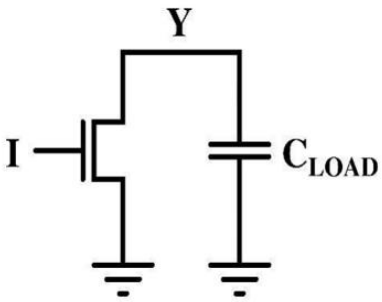


Fig. 4

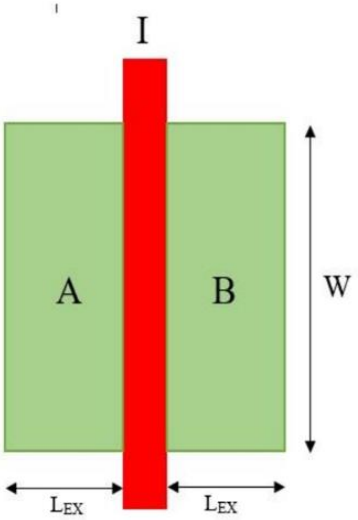


Fig. 5

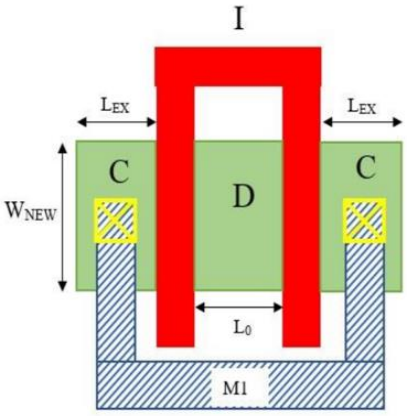


Fig. 6

Soln:

a) *Diffusion capacitance = bottom capacitance + sidewall capacitance*
For region A ,
*diffusion cap = cb *(W *Lex) + cs *(W + 2* Lex)*
*diffusion cap = 0.5 *(W *W/4) + 0.4 *(W + 2* W/4)* *[0.5 marks]*
==> 0.03125 + 0.3 = 0.33125 fF
Region A and B are symmetric so for B also 0.33125 fF

For region C,
Bottom capacitance is proportional to the bottom area
*As, area of region A= W*Lex*
*Aea of region C =2 * (W/2* Lex) = W*Lex = Area of region A*
So, bottom cap of region C = 0.03125 fF *[0.5 marks]*

Sidewall capacitance is proportional to the perimeter of the sidewall
*Perimeter of sidewall in region A = W + 2*Lex = 0.5 + 2*0.125 =0.75u*
Perimeter of sidewall in region C = 2 (W/2 + 2*Lex) = 2* (0.25 + 2*0.125) =1u*
*So, sidewall cap of region C = (1/0.75)*sidewall cap of A = 0.4 fF* *[0.5 marks]*

So, diffusion capacitance of region C= 0.4 + 0.03125 = 0.43125 fF

For region D,
Bottom capacitance is proportional to the bottom area
*As, area of region A= W*Lex*
Aea of region D = W/2 Lo = W/2 * 1.25Lex*
*So, bottom cap of region D = 0.625 * bottom cap of A= 0.0195 fF* *[0.5 marks]*

Sidewall capacitance is proportional to the perimeter of the sidewall
*Perimeter of sidewall in region A = W + 2*Lex = 0.5 + 2*0.125 =0.75u*
Perimeter of sidewall in region D = 2 Lo = 2*1.25Lex= 0.3125u*
*So, sidewall cap of region D = (0.3125/0.75)*sidewall cap of A = 0.125 fF [0.5 marks]*

So, diffusion cap of region D = 0.0195 + 0.125 = 0.1445fF

b) *In Fig.5 as A and B region is symmetric we can connect Y in either of the region*
In Fig.6 , output Y should be connected to the D region as it has less capacitance than C region. [0.5 + 0.5 marks]