CSE/ECE 511 Mid-semester Examination

Time Limit: 1 Hour **[50 Marks]**

Instructions for the examination:

1. **Mobile phones, bags, wrist watches of any kind are NOT Permitted in the examination hall.**
2. **The use of calculators is not permitted for the duration of the Examination.**
3. **Write all the assumptions, if any, clearly. *Only reasonable assumptions will be considered if any ambiguity is found in the question*.**
4. **Institute's plagiarism policy will apply in case any unfair means are observed.**

Q1. Consider an I2OI processor (In order frontend, out-of-order issue and writeback, in-order commit) executes the given program. Draw the pipeline diagram for the program. **[15 Marks]**

- Assume full bypassing; multiplication takes four clock cycles (Y0, Y1, Y2, Y3); addition and subtraction take one clock cycle (X0).
- The pipeline stages include Fetch (F), Decode (D), Issue (I), Execution (consists of multiplication and addition units in parallel), Writeback (W) and Commit (C).

1. MUL R4, R5, R6
2. ADD R1, R4, R5
3. SUB R2, R3, R15
4. MUL R1, R2, R3
5. SUB R7, R8, R9
6. ADD R12, R13, R15
7. MUL R4, R12, R11

Q2. A processor has the following specifications: Word size is 16-bits; No. of blocks in cache is 8; Cache block size is 1 word; Cache uses LRU replacement policy and Write back scheme; Main memory is word addressable; Cache is 4-way associative cache. For this cache, the following sequence of memory address access happens. **[15 Marks]**

0xF226, 0x9D97, 0x2AE5, 0xEB34, 0x48D0, 0x6B03, 0xB3A5, 0x61D6, 0x1900, 0x48D0, 0xFAE7, 0x1608

Assume that all cache lines are invalid when the sequence of operations starts.

a. List the memory addresses that are available in Set 0 and Set 1 after all memory access operations are performed. Indicate block replacements wherever applicable. **[14 Marks]**
b. At the end, which address is the Most Recently Used (MRU) in set 1? **[1 Mark]**

Q3. For all the following code and questions, follow the given **instructions**: **[20 Marks]**

1. The In-Order pipeline has 5 stages: **F**etch, **D**ecode, e**X**ecute, **M**emory and **W**riteback.
2. Each stage requires one clock cycle.
3. All memory references hit in the cache and assume that you have separate instruction and data memory.
4. L1 and L2 denote labels and are not part of instructions.
5. The branch instructions are resolved at the X stage.
6. Assume that bypassing applies to all the instructions.

The following **assumptions** are valid for the code that follows:

1. The Address of each Memory location is 8 Bits long, and the Data width is also 8 Bits long.
2. The memory location of 0x00 (0th Location) has '0' (= 0x00) stored inside it.
3. Registers R1 to R15 are initialized to the value of 0x01.
4. Register R0 always contains 0x00, and this value can not be modified by any instruction.

(PTO for 5th point)

5. Assume that if a branch is calculated (in execute stage) to be taken, PC gets updated in Execute stage only, and all the pipelines just after **this** Execute cycle will be flushed out by default. The instruction to be branched at will start **fetching** just after the execute cycle of the instruction where the branch was calculated.

Assembly Code:

```
1.  LD        R4    0(R5)
2.  LD        R2    4(R4)
3.  ADD       R15   R0    R0
4.  LD        R14   0(R0)
5.  BEQ       R14   R15   L1
6.  LWI       R10   #10
7.  ADD       R7    R8    R9
8.  SUB       R7    R3    R6
9.  L1: BNEZ  R10   L2
10. ADD       R4    R7    R10
11. L2: SUB   R10   R10   R14
```

a) Draw the pipeline diagram for the above assembly code. **[11 Marks]**

b) Report the total number of cycles required to execute the above assembly code. **[1 Mark]**

c) At which clock cycle should instruction 11 be fetched? Explain your answer. **[1 + 2 Marks]**

d) Report the value of register R10 after the code has finished its execution. Explain how you arrive at this value by indicating how the different instructions affect the final value of R10 and what all registers are responsible for this final value. **[1 + 4 Marks]**