CSE/ECE 511: Mid-Semester Rubric

Q1.

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
1	MUL R4,R5,R6	F	D	I	Y0	Y1	Y2	Y3	W	C									
2	ADD R1, R4,R5		F	D	I	I	I	I	X0	W	C								
3	SUB R2,R3,R15			F	D	D	D	D	I	X0	W	C							
4	MUL R1,R2,R3				F	F	F	F	D	I	Y0	Y1	Y2	Y3	W	C			
5	SUB R7,R8,R9								F	D	I	X0	W	r			C		
6	ADD R12, R13,R15									F	D	I	X0	W	r			C	
7	MUL R4,R12,R11										F	D	I	Y0	Y1	Y2	Y3	W	C

Marks Distribution:

1. 1.5
2. 2.5
3. 2
4. 2.5
5. 2.5
6. 2.5
7. 1.5

Q2. a.

In the given configuration, the last bit decides the set number. If it is 0, the address belongs to set 0 and if 1, to set 1.

Set 0	**Set 1**
F226	9D97
EB34	2AE5
48D0	6B03
61D6	3BA5

Till address 61D6, the cache line status is given above. **(1*8 = 8 marks)**

Set 0	**Set 1**
~~F226~~ 1900	~~9D97~~ FAE7
~~EB34~~ 1608	2AE5
48D0 (hit)	6B03
61D6	3BA5

The above table shows the cache line status after 61D6 memory access. **(1.5*4 = 6)**

b. MRU address in set 1 = FAE7 **(1 mark)**

Q3.

<u>Note</u>: In case the points mentioned in rubric of parts (c) and (b) do not exactly match with response in the answer sheets, the marks have been awarded on the basis of understanding on a case to case basis and will not be changed.

a)

		<— Clock Cycles —>																
	Instructions	**C1**	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**	**C11**	**C12**	**C13**	**C14**	**C15**	**C16**	**C17**
1	LD R4 0(R5)	F	D	X	M	W												
2	LD R2 4(R4)		F	D	D	X	M	W										
3	ADD R15 R0 R0			F	F	D	X	M	W									
4	LD R14 0(R0)					F	D	X	M	W								
5	BEQ R14 R15 L1						F	D	D	X	M	W						
6	LWI R10 #10							F	F	D	-	-						
7	ADD R7 R8 R9									F	-	-						
8	SUB R7 R3 R6									-	-	-						
9	L1: BNEZ R10 L2										F	D	X	M	W			
10	ADD R4 R7 R10											F	D	-	-			
11	L2: SUB R10 R10 R14												F	-	-			
11	L2: SUB R10 R10 R14													F	D	X	M	W

Marks for each instruction with correct pipeline are as follows:

1. **0.25**
2. **0.25**
3. **0.5**
4. **0.75**
5. **2**
6. **1**
7. **1**
8. **1**
9. **2**
10. **0.25**
11. **2**

b) Total Number of Cycles are = 17 → **1 Mark**
Total cycles = 16 or 18 → **0.5 Marks**

c) Instruction 11 is finally fetched at C13 → **1 Marks**

1. Instruction 11 should be fetched firstly at C12 by the virtue of normal pipeline operation where the processor fetches the next instruction by default as the PC value keeps getting updated with each instruction
2. But, since the branch is calculated only at C12, it will update the PC and this updated PC happens to be the same value as the address of instruction 11 only.
3. So, in cycle C13, Branch instruction does two things, 1st, flushes the pipeline of instruction 10 and 11 from cycle C13 onwards and 2nd, again fetches the instruction at updated value of PC (containing the address to be branched to), which happens to be the same instruction 11 which is just flushed out of pipeline. Hence, it gets re-fetched in C13.

2 Marks= 0.5 Marks (I11 got fetched at C12) + 0.5 Marks (Writing about PC) + 1 Mark (Writing what happens in C13)

d) Final value of R10 = 0x01 = 1 (in decimal) → **1 Mark**

Explanation:

- It is given that registers R1 to R15 are initialized to value 0x01 = 1 in decimal
- Initial value of R10 = 0x01
- Instruction 4: R14 = Value stored at address = 0 + address in R0 = 0x00 + 0x00
    - Value stored at address 0x00 = 0x00 (assumption 4)
- Instruction 6: Value ‘10’ does not get loaded to R10 due to pipeline flushing as soon as branch is calculated to be taken by instruction 5’s X (Execute) stage.
- Instruction 9: Branch gets taken as R10 is still = 0x01 != 0x00
- Instruction 11: R10 = R10 - R14 = 0x01 - 0x00 = 0x01 = 1 in decimal

2 Marks → For writing correct instructions responsible : 4, 5, 6, 9, 11

2 Marks → 1Mark For writing R14’s contribution + 1 Mark for correct value of R14