DVD Quiz 7

Total marks =10

Instructions

1. This is a take-home quiz, with no compulsion to join the meeting, but please ask your doubts in the meeting itself.

*2. The quiz duration is **25 mins and 10 mins** extra given to upload your scanned PDFs (high quality) on the google classroom. Upload answer PDF on classroom*

*3. The quiz starts at **8:00 PM** sharp and ends at 8:20 PM. 10 minutes are reserved for scanning and uploading the quiz to Google Classroom, any submission after **8:35 PM** will attract a penalty*

4. Meeting link for doubts: https://meet.google.com/gyd-cecr-tez

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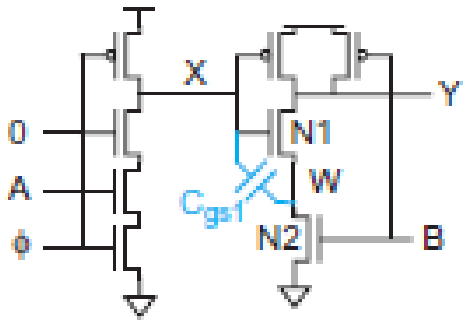
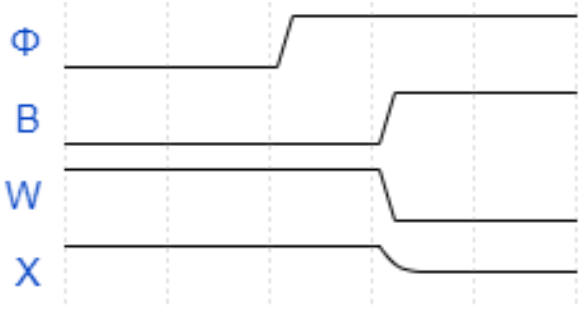
Q1. Explain back gate coupling using the below circuit (2 marks) with waveform (1 mark), and how it can be avoided (1 mark)? (4 marks)



ANS.

In the above circuit, a dynamic NAND gate drives a static NAND gate. The gate-to-source capacitance Cgs1 of N1 is shown explicitly. Suppose that the dynamic gate is in the evaluation and its output X is floating high. The other input B to the static NAND gate is initially low. Therefore, the NAND output Y is high and the internal node W is charged up to $V_{DD} - V_{tn}$. At some time B rises, discharging Y and W through transistor N2. The source of N1 falls. This tends to bring the gate along for the ride because of the Cgs1 capacitance, resulting in a drop on the dynamic node X. As with charge sharing, the magnitude of the drop depends on the ratio of Cgs1 to the total capacitance on node X. **(2 marks)**



(1 mark)

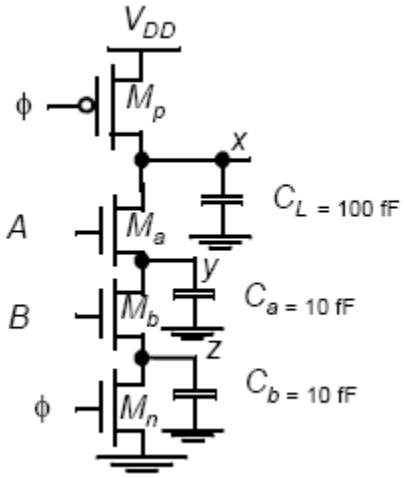
Back-gate coupling is eliminated by driving the input closer to the rail. For example, if X drove N2 instead of N1, the problem would be avoided. Otherwise, the back-gate coupling noise must be included in the dynamic noise budget. **(1 mark)**

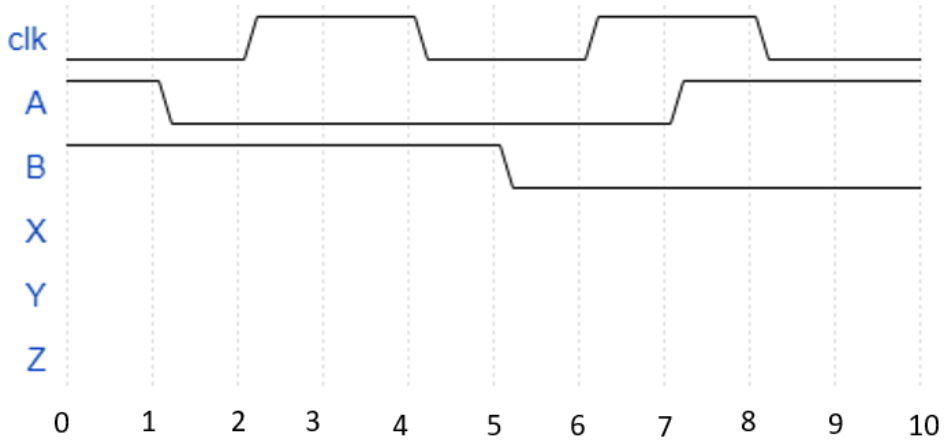
Q2. One of the partitions on SoC is operating at high frequency (>Mhz) while another partition is working on very low frequency, you have to design a circuit for the same. Explain briefly where you use dynamic logic style and why? (2 mark)

ANS- we use dynamic logic for high-frequency partition because..**.**

During the evaluation phase, when the pull-down network is not ON, then leakage current exists in the form of the reverse-biased diode and subthreshold leakage, if the frequency is high then the output node discharges less compared to when the frequency is low if the change in Vout is larger than the $|Vtp|$ of static inverter following the dynamic gate, there exists a short circuit current in the static inverter which further increases the power consumption. That's why we avoid using dynamic gates in low-frequency operations.

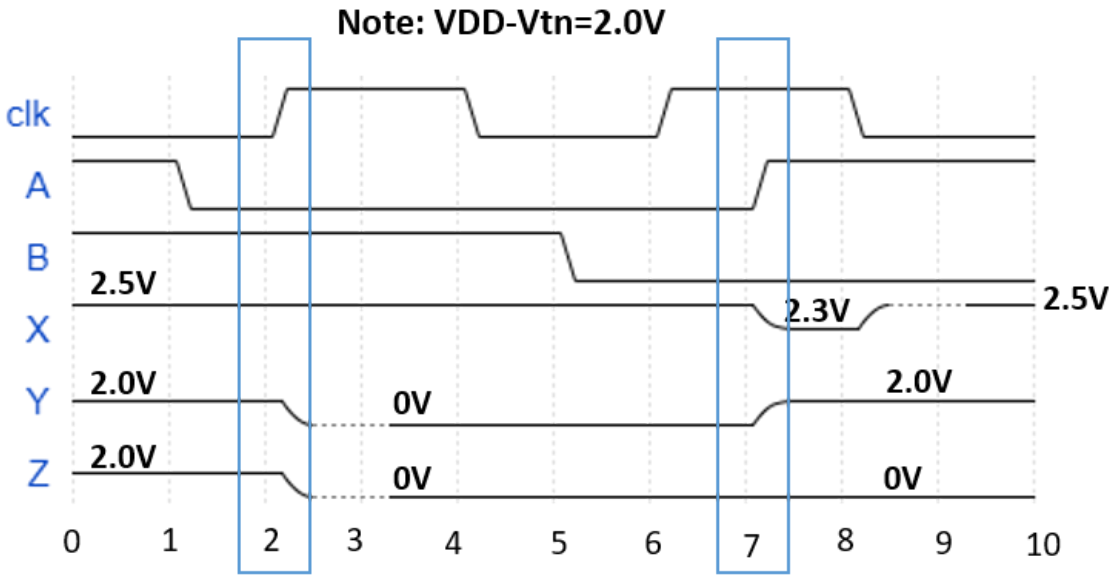
Q3. If Vtn=|Vtp|=0.5V and V_{DD} is 2.5 V then complete the waveform of the X, Y and Z node for the below circuit (2 marks)and verify it mathematically (2 marks) {overall 4 marks}





ANS:

The waveform of the desired node is shown below. **(2 marks)**



Mathematical explanation (2 marks)

At time t=0

A=B=2.5V

Along with node X, internal nodes Y and Z will be precharged to (V_{DD}-V_{tn})

At time t=2

A=0V B=2.5V

VY remains at 2.5V while internal nodes discharge to 0V.

At time t=7

For the case when Vx is at VDD while Vy is at zero and input A is "2.5V" and B=0V , there are two possibilities.

1) When $\Delta V_{out} < V_{tn}$

   $Vy = (V_{DD}-V_{tn})$

   $\Delta V_{out} = - (C_a/C_L)*\{V_{DD}-V_{tn}\}$ -----(1)

2) When $\Delta V_{out} > V_{tn}$

   $\Delta V_{out} = - \{C_a/(C_a +C_L)\}*V_{DD}$ -------(2)

Which of the above scenario is valid is determined by the capacitance ratio, boundary condition between two cases can be determined by setting ΔV_{out} equals to V_{tn}, putting $\Delta V_{out} = V_{tn}$ in any of the above equations gives you.

$$C_a/C_L = V_{tn}/(V_{DD}-V_{tn}) \quad \text{------(3)}$$

If $C_a/C_L < V_{tn}/(V_{DD}-V_{tn})$ then equation 1 holds while if $C_a/C_L > V_{tn}/(V_{DD}-V_{tn})$ then equation 2 holds.

Now,

C_a/C_L =0.1

$V_{tn}/(V_{DD}-V_{tn}) = 0.5/2 = 0.25$

Since $C_a/C_L < V_{tn}/(V_{DD}-V_{tn})$ **,**Therefore equation 1 hold true.

$V_Y=V_{DD}-V_{tn}= 2.0V$

While

$\Delta V_{out} = - (C_a/C_L)*\{V_{DD}-V_{tn}\} = - 2.0/10= -0.2V$

V_Y=2.3V