ECE-314/514 Digital VLSI Design
End-Semester Exam
17-Dec-2022

Max Marks: 25 Duration: 90 mins

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Instructions:

1. This is a closed book exam
2. Use of calculators is allowed.
3. Question paper contains 11 questions. All questions are compulsory.
4. If you are making any assumptions, please mention them clearly in your sheet.
5. Institute plagiarism policy applies in this submission.

Q1.

a) What is time borrowing? What is the timing constraint in adjacent stages, so that latches can borrow time for a two-phase latch? Explain with the help of a timing diagram. [2 Marks] (CO4)

b) How can we enable time borrowing in FF-based sequencing? [1 Marks] (CO4)

Q2. Many exceptions are allowed in high density SRAM cells to recover area. List at least 2 such exceptions. Explain, why are such exceptions allowed only in memory arrays? [2 Marks] (CO5)

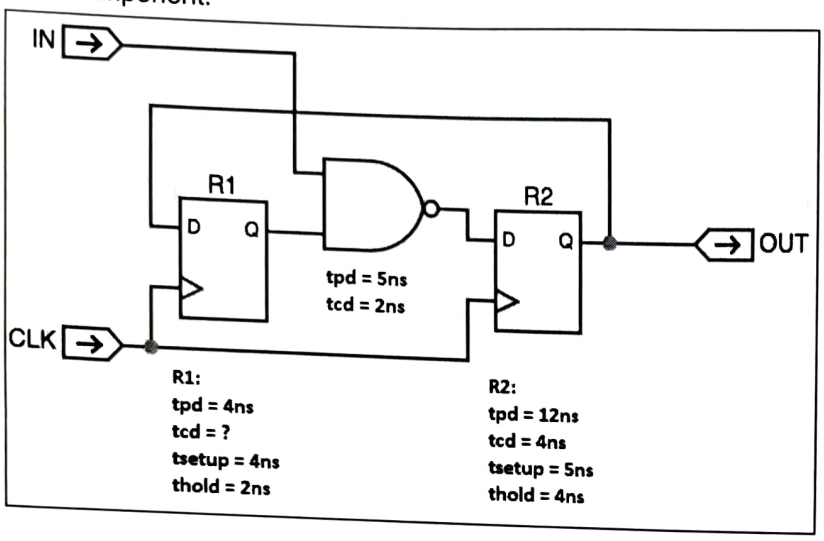
Q3.

a) If devices in a 6T SRAM cell are sized as follows in 65nm technology in the table below, which has better SNM, Write Margin and Leakage? [1.5 Marks] (CO5)

b) Which one of them is an overall better cell and why? [0.5 Marks] (CO5)

Cell-A	PG = 180nm/ 65nm PU = 220nm/ 65nm PD = 100nm/ 65nm
Cell-B	PG = 180nm/ 70nm PU = 100nm/ 70 nm PD = 220nm/ 70nm

Q4. Consider the following sequential logic circuit. The timing specifications are shown below for each component.



(a) What is the value for the period of CLK (i.e., tclk) that will allow both registers in the circuit to operate correctly?

[1 Marks] (CO4)

(b) What is the value for the tcd of R1 that will allow both registers in the circuit to operate correctly?

[1 Marks] (CO4)

Q5.

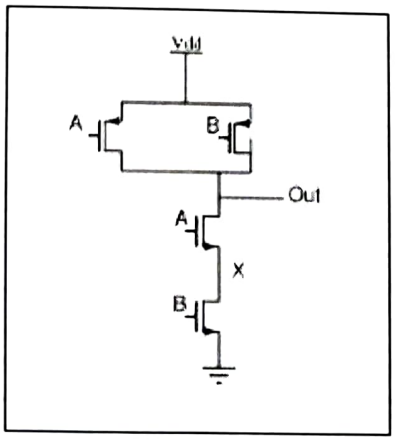
Consider a generic two-input NAND gate. Arrange the following input sequences in the ascending order of the strength of the corresponding pull-down ability. Explain your result.

(a) A,B both shift from 0⇒1,

(b) A remains stable and B shifts, 0 → 1

(c) B remains stable and A shifts 0 → 1

[1.5 marks] (CO4)



Q6.

a) List one advantage and a disadvantage of using a transmission gate based circuit? [1 Marks] (CO4)

b) Draw a transmission gate/ Tri state-based positive edge triggered flip flop. [1 Marks] (CO4)

Q7.

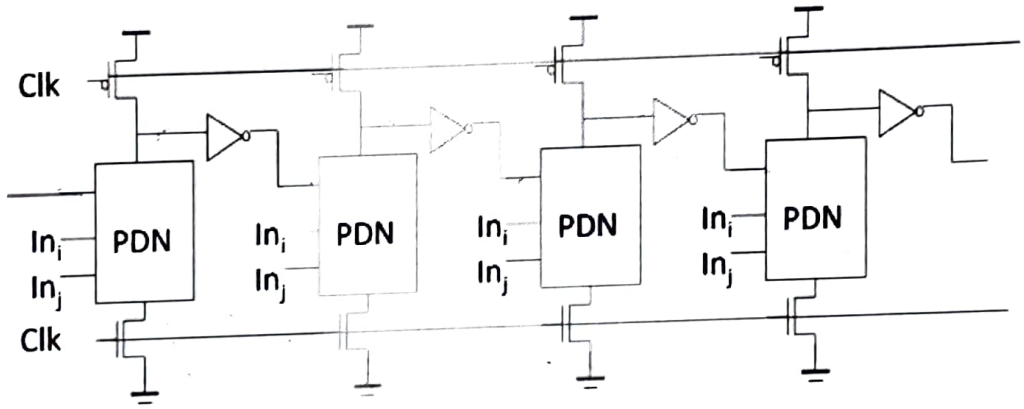
a) List any 2 challenges in using dynamic logic based circuits? [1 marks] (CO4)

b) How can these challenges be overcome? [1 marks] (CO4)

Q8.

a) Why can we remove the footer transistor in the domino logic without loss of functionality? [1 Marks] (CO4)

b) Assume that each of the following four dynamic gates shown in the figure have a delay of 100ps from input to output. Delay of the inverter is 50ps. Considering this circuit as an independent block and a clock duty cycle of 50%, what is the highest clock (CLK) frequency at which we can operate this circuit? [2 Marks] (CO4)



Q9.

a) What is an accelerated life test? [1 Marks] (CO5)

b) List any 2 aging mechanisms leading to failure of chip [1 Marks] (CO5)

Q10.

a) List any three sources of clock uncertainty. [1.5 Marks] (CO4)

b) How is clock skew different from clock jitter? [1 Marks] (CO4)

Q11.

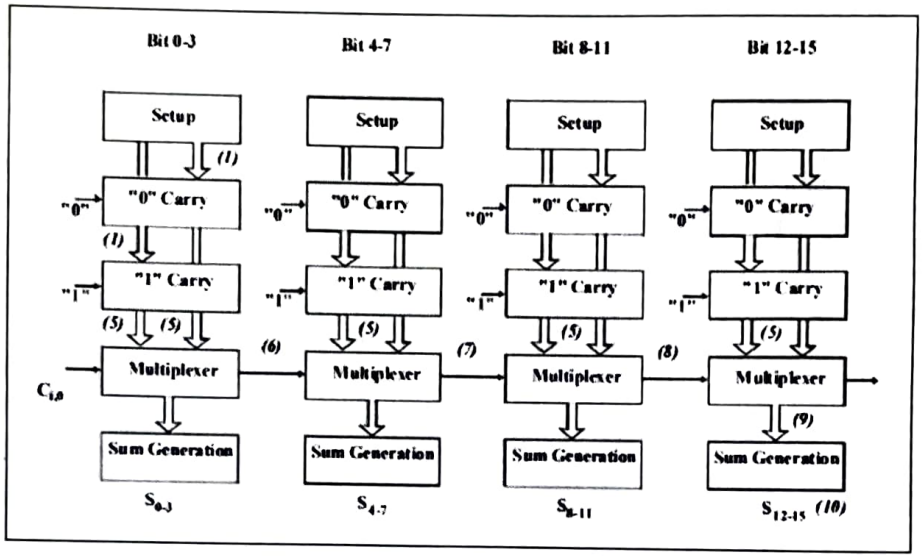
Linear Carry Select and Square root carry select adders are shown in the figure below.

a) Identify the critical path for the two circuits (redraw the circuit in your answer-script). [2 marks] (CO5)

b) Calculate the delay for both adders for 16-bits. Assume delay of Setup, ~~Carry~~, and sum-generation blocks to be 1 unit. Assume the delay of Multiplexer to be 0.5 units. [1 Marks] (CO5)

Assume delay of carry 1 unit

Linear Carry Select Adder:



Square Root Select Adder: