DVD Quiz 7

Total marks =10

Instructions

1. This is a take-home quiz, with no compulsion to join the meeting, but please ask your doubts in the meeting itself.

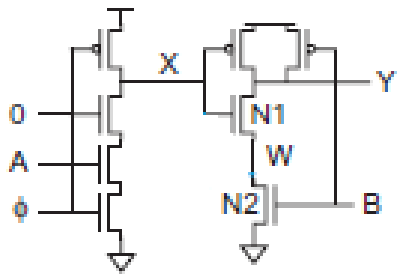
*2. The quiz duration is **25 mins and 10 mins** extra given to upload your scanned PDFs (high quality) on the google classroom. Upload answer PDF on classroom*

*3. The quiz starts at **8:00 PM** sharp and ends at 8:25 PM. 10 minutes are reserved for scanning and uploading the quiz to Google Classroom, any submission after **8:35 PM** will attract a penalty*

4. Meeting link for doubts: https://meet.google.com/gyd-cecr-tez

---

Q1. Explain back gate coupling using the below circuit (2 marks) with waveform (1 mark), and how it can be avoided (1 mark)? (4 marks)



Q2. One of the partitions on SoC is operating at high frequency (>Mhz) while another partition is working on very low frequency, you have to design a circuit for the same. Explain briefly where you use dynamic logic style and why? (2 mark)

Q3. If Vtn=$|Vtp|$=0.5V and V_{DD} is 2.5 V then complete the waveform of the X, Y and Z node in the below circuit (2 marks)and verify it mathematically (2 marks) {overall 4 marks}