VLSI Design Flow

End Semester Exam (12th May 2022)

Time allowed: 2 hours

Maximum Marks: 50

Note:

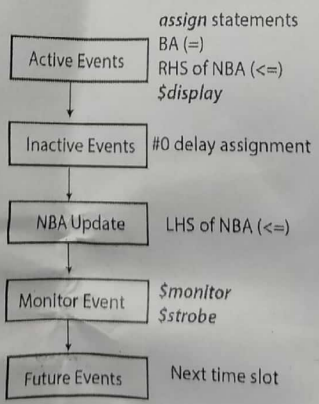
I. *There are 3 questions (each of them has sub-parts). All questions are compulsory.*
II. *Marks are indicated in bold at the end of each question.*
III. *Be crisp and precise in your answer so that you can complete the answers in 2 hours.*
IV. *Use the marks allotted to each question as an indicator of how elaborate you need to answer.*
V. *Use of any communication device is prohibited during examination.*
VI. *Cheating or use of unfair means will be dealt with as per institute policy.*

1.

a. Consider the following piece of Verilog code.

```
assign p = q;
initial
 begin
    q = 1;
    #1 q = 0;
    $display(p);
end
```

What will be displayed by $display statement above? Explain your answer. The stratified Verilog event queue is shown below (You may use it if you want).



(1+3 Marks)

p=1

b. Consider the following Verilog code.

```
module top(a, b, c, s, en, out1, out2);
    input a, b, c, s, en;
    output out1, out2;
    reg out1, out2;

    always @(*) begin
        if (s==1'b0)
            out1 = a;
        else
            out1 = b;
    end

    always @(*) begin
        if (en==1'b1)
            out2 = c;
    end
endmodule
```

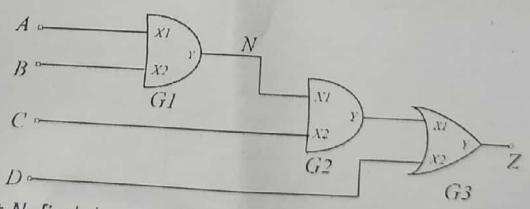
Predict and draw the schematic of the synthesized netlist (mark the circuit elements properly). **(4 Marks)**

c. Consider an FSM with five states $Q = \{s0, s1, s2, s3, s4\}$. Let the states be represented by three state bits a, b, c, and encode the states as bit sequence (abc). Let the encoding be $\{000, 001, 010, 011, 100\}$ for the states $Q = \{s0, s1, s2, s3, s4\}$, respectively. For this encoding, find the characteristic function of the subset of states $\{s0, s2, s4\}$ (a characteristic function of a set indicates whether an element belongs to that set or not). Draw the ROBDD for this function with the variable order a, b, c. **(2+3 Marks)**

d. How can increasing the size of a cell in the critical path improve the worst setup slack? **(2 Marks)**

2.

a. Consider the circuit shown below.



i. For the net N, find the set of test pattern(s) that will make it 0.

ii. Find the set of test pattern(s) that will detect SA0 at the net N.

iii. Choose an appropriate pattern P1 from (i) above and pattern P2 from (ii) above such that if we apply P1 and then P2, we will be able to observe the effect of a rise transition occurring at the net N at the output Z.

iv. Explain how does the pattern chosen in (iii) able to detect a slow-to-rise transition fault at the net N. [A slow-to-rise transition fault is manifested as a signal rising very slowly from the 0 state].

[1+1+1+2 Marks]

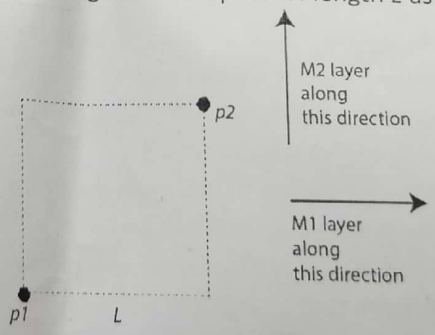
b. There were two chips fabricated: 'chip-A' and 'chip-B,' both fabricated for a frequency of 1 GHz. However, due to human error, 'chip-A' had **setup violations** at 100 different flip-flops and was erroneously ignored by the designer. The correct slacks for setup checks at these flip-flops were -20 ps.
Similarly, due to human error, 'chip-B' had **hold violations** at 100 different flip-flops and was ignored by the designer. The correct slacks for hold check at these flip-flops were -20 ps.
Which of the two chips can be given to a customer who does not require to run the chip at a very high frequency and which cannot be given? Explain both your answers.

(1+2 Marks)

c. Consider a sub-circuit with three nets *N1*, *N2*, and *N3*.
The net *N1* has 3 pins *p1*, *p2*, and *p3* with locations (0,0), (1,5), and (4,3), respectively.
The net *N2* has 4 pins *p4*, *p5*, *p6*, and *p7* with locations (3,4), (2,5), (4,4), and (2,9), respectively.
The net *N3* has 2 pins *p8* and *p9* with locations (7,7) and (9,16), respectively.
Estimate the total wirelength using Half-perimeter Wire length (HPWL) measure.

(4 Marks)

d. Two pins *p1* and *p2* are at the diagonal of a square of length *L* as shown below.

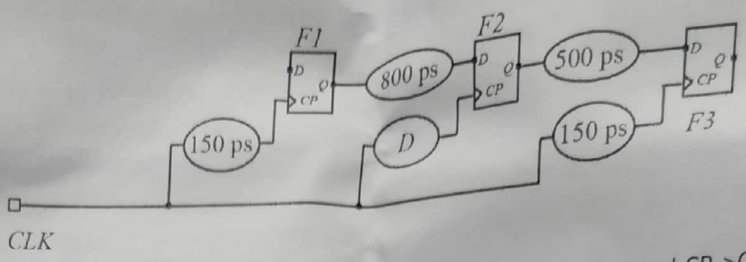


Determine the percentage reduction in the optimum wirelength connecting *p1* to *p2* if the routing along the diagonal (45° orientation) is allowed compared to the traditional Manhattan orientation.

(3 Marks)

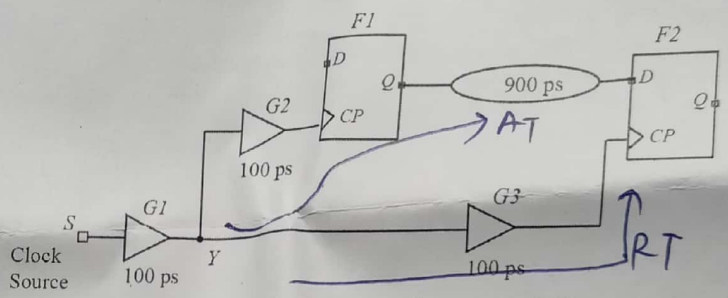
3.

a. The critical portion of a circuit is shown below.



Assume that all the flip-flops are ideal (setup time, hold time, and CP->Q delay are zero). Find the delay D of the element in the clock path such that the circuit operates at the maximum clock frequency satisfying the setup constraint. Ignore the delay of the wires and the hold constraints. Find the corresponding clock period. **(4+1 mark)**

b. A portion of a sequential synchronous circuit is shown in below.



The following attributes are valid for both the flip-flops *F1* and *F2*: setup time=25 ps and CP->Q delay=25 ps. The delay of the combinational block in the data path is 900 ps. The frequency of the Clock is 1 GHz. Ignore the delay of all the wires. Find the setup slack under the following conditions:

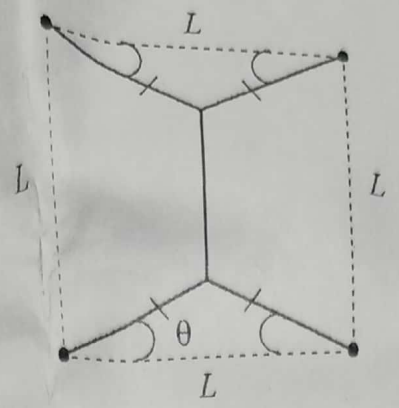
i. Nominal delays, as shown in the figure, are considered.

ii. Assume that an OCV derate factor of 1.1 is added to the delay for the late paths, and 0.9 is added to the delay for the early paths.

iii. Assume that an OCV derate factor of 1.1 is added to the delay for the late paths, and 0.9 is added to the delay for the early paths (same as in part (ii) above). Furthermore, consider Common Path Pessimism Removal (CPPR) in the computation.

(2+4+4 Marks)

c. Four pins are placed at the corner of a square of length *L*, as shown on the next page. We want to connect them using wire segments of total minimum length. The solution is given by the Steiner Minimum Tree shown in the figure (All four angles/segments marked in the figure are equal).



Derive the value of θ such that total wire length is minimum. No marks for just writing the answer, you need to derive it. **(5 Marks)**