QUIZ-8

Duration: 15 mins

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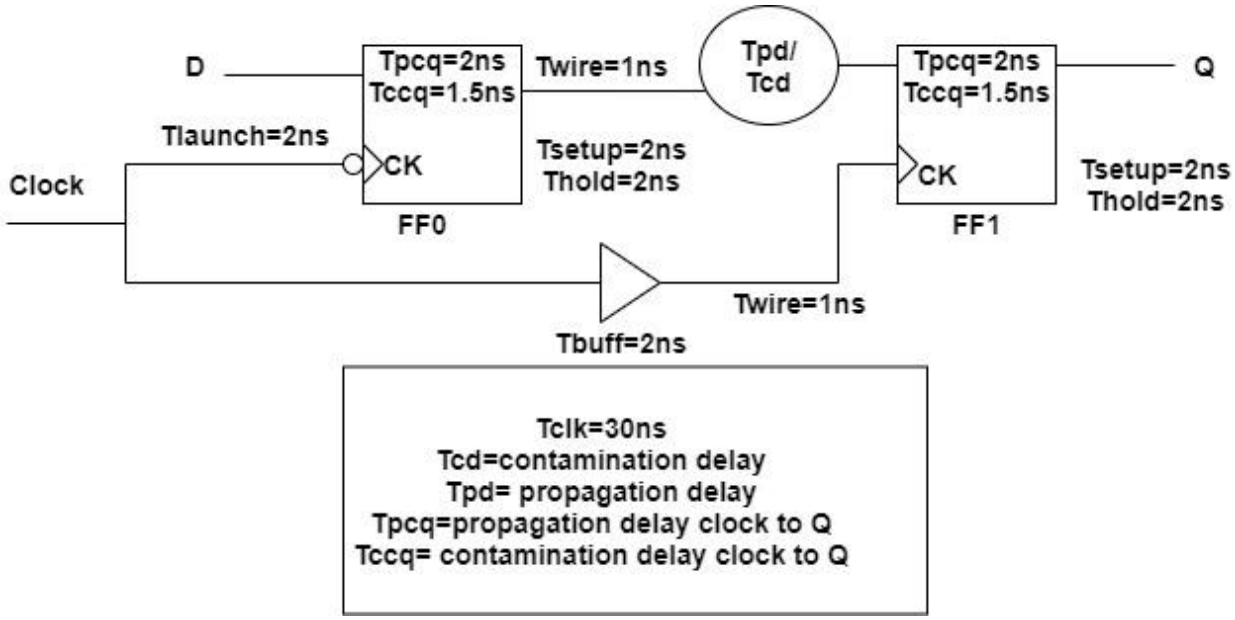
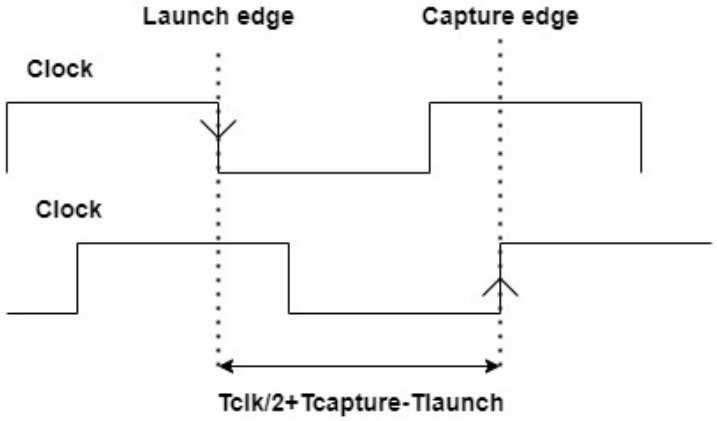
1. **Determine the value of Tpd and Tcd in order to satisfy the setup time and hold time constraints . (5+5)**



Ans:



Since the launch flop is negative edge triggered and the capture flop is positive edge triggered,

the effective time between the launch edge and capture edge are:

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RT= Tclk/2 + Tcapture -Tlaunch-Tsetup [2 marks]

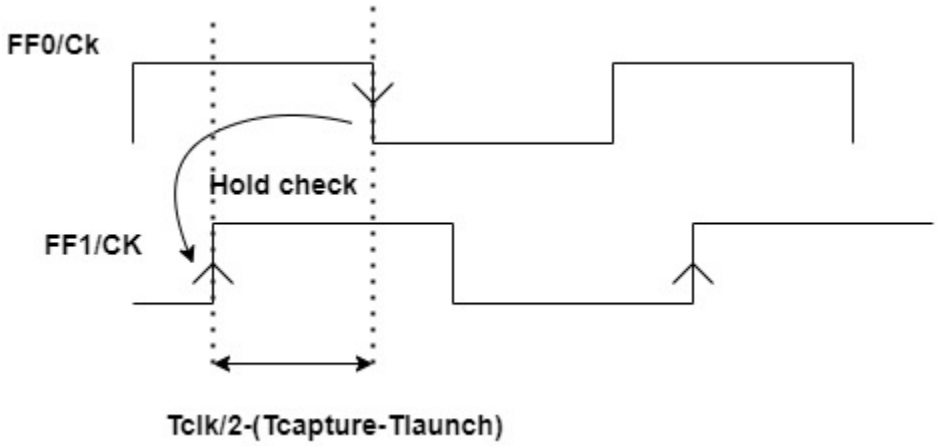
Here Tcapture = (Tbuff+ Twire)
Tlaunch = 2ns
Data arrival time (AT)= Tpcq+ Twire+ Tpd [2 marks]

Therefore, in order to satisfy max time constraint,
RT>=AT

Tclk/2 + (Tbuff+ Twire) -Tlaunch-Tsetup >= Tpcq+Twire+Tpd

=> 30/2 + (2+1)-2-2 >= 2+1+Tpd
=> Tpd <= 11ns [1 mark]

Hold condition is checked prior to the capture edge.



Here Required time (RT)=Thold - (Tclk/2- Tcapture+Tlaunch) [2 marks]
Data Arrival Time (AT)= Tccq+ Twire+ Tcd [2 marks]

In order to satisfy hold time constraints AT>=RT

Tccq+ Twire+ Tcd > =Thold - (Tclk/2- Tcapture+Tlaunch)

=> 1.5 + 1 + Tcd >= 2-(30/2- (2+1)+2))
=> Tcd>= -14.5ns
Since the delay can't be negative. This circuit will always satisfy the hold time constraint for any Tcd. [1 mark]

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