INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI
ECE 111 DIGITAL CIRCUITS
MID-SEM SOLUTIONS

Q1. a) For the function f(w,x,y,z) given in the K-map, identify the Prime Implicants (minterms) and Essential Prime Implicants (minterms). Also obtain the minimized SOP term for the same. [4 + 4]

b) For the function in Fig. Q1, give a realization using only 2-input NOR gate. [6]

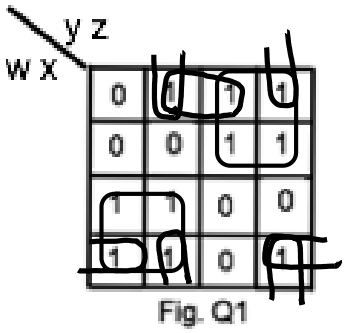


Fig. Q1

a)

Prime Implicants: $w\overline{y}$; $\overline{w}\,y$; $\overline{x}\,y\overline{z}$; $\overline{x}\,\overline{y}\,z$; $w\overline{x}\,\overline{z}$; $\overline{w}\,\overline{x}\,z$

Essential Prime Implicants: $w\overline{y}$; $\overline{w}\,y$

Minimum SOP form:

- $f(w,x,y,z) = w\overline{y} + \overline{w}\,y + w\overline{x}\,\overline{z} + \overline{w}\,\overline{x}\,z$

or

$f(w,x,y,z) = w\overline{y} + \overline{w}\,y + \overline{x}\,y\overline{z} + \overline{w}\,\overline{x}\,z$

or

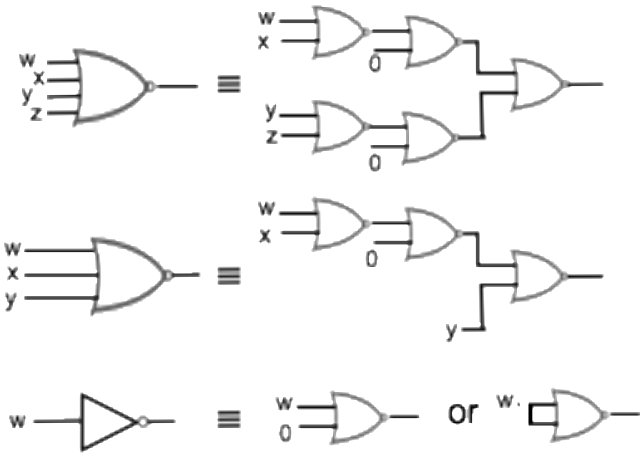
$f(w,x,y,z) = w\overline{y} + \overline{w}\,y + \overline{x}\,y\overline{z} + \overline{x}\,\overline{y}\,z$

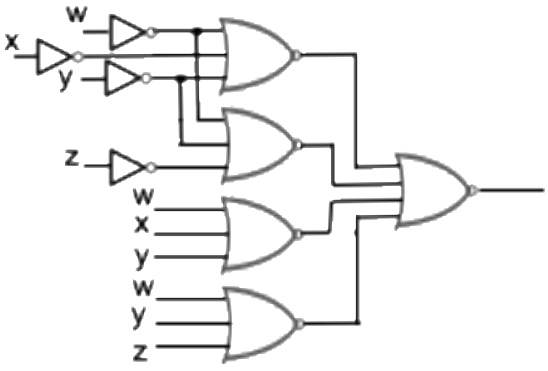
or

$f(w,x,y,z) = w\overline{y} + \overline{w}\,y + w\overline{x}\,\overline{z} + \overline{x}\,\overline{y}\,z$

b) For realization with NOR gates we require POS form which from the K-map can be obtained as,

$$f(w,x,y,z) = (\overline{w} + \overline{x} + \overline{y})(\overline{w} + \overline{y} + \overline{z})(w + x + y)(w + y + z)$$





Q2. Decimal numbers can be coded in various binary codes. The excess-3 BCD and the 5-4-2-1 codes for the decimal digits 0-1-2-3-4-5-6-7-8-9 are as follows.

Excess-3 ($E_3\ E_2\ E_1\ E_0$) : 0011-0100-0101-0110-0111-1000-1001-1010-1011-1100,

5-4-2-1: ($C_3\ C_2\ C_1C_0$) : 0000-0001-0010-0011-0100-1000-1001-1010-1011-1100.

(a) Construct Karnaugh maps for the two output variables ***C_1 and C_0*** in terms of the four input variables ***$E_3\ E_2\ E_1\ E_0$***, marking as "don't care" (***X or ϕ***) the combinations that do not correspond to any decimal digit. [4]

(b) Read the K-maps to obtain minimal SOP expressions for the output variables ***C_1 and C_0***. [4]

(c) Find the number of NAND chips required for implementing the logic, given quad 2-input NAND Gates. [4]

E_3E_2 \ E_1E_0	00	01	11	10
00	ϕ	ϕ	0	ϕ
01	0	1	0	1
11	0	ϕ	ϕ	ϕ
10	0	0	1	1

$$C_1 = E_3E_1 + E_1\overline{E_0} + \overline{E_3}\ \overline{E_1}\ E_0$$

or

$$C_1 = E_3E_1 + E_1\overline{E_0} + E_2\ \overline{E_1}\ E_0$$

E_3E_2 \ E_1E_0	00	01	11	10
00	ϕ	ϕ	0	ϕ
01	1	0	0	1
11	0	ϕ	ϕ	ϕ
10	0	1	1	0

$$C_0 = \overline{E_3}\ \overline{E_0} + E_3E_0$$

To realize C_1 as $C_1 = E_3E_1 + E_1\overline{E_0} + E_2\ \overline{E_1}\ E_0$ we would require 3 chips (10 NAND gates) and for C_0 we would require 2 chips (5 NAND gates). Together we would only require 4 chips as 3 of the unused NAND from C_1 realization can be used for C_0.If the student gives only the underlined answer give full marks.

or

To realize C_1 as $C_1 = E_3E_1 + E_1\overline{E_0} + \overline{E_3}\ \overline{E_1}\ E_0$ we would require 3 chips (11 NAND gates) and for C_0 we would require 2 chips (5 NAND gates). Together we would only require 4 chips as 2 of the unused NAND from C_1 realization can be used for C_0. If the student gives only the underlined answer give full marks.

or

To realize C_1 as $C_1 = E_1(E_3 + \overline{E_0}) + \overline{E_3}\ \overline{E_1}\ E_0$ (not a minimized SOP form but a mix of SOP and POS) we would require 2 chips (8 NAND gates) and for C_0 we would require 2 chips (5 NAND gates).

All the three answers given are acceptable.

Q3. A computer, using 3-digit radix complement arithmetic with an unknown radix *r*, gives the following results expressed in radix complement form:

$$(m+n)_r = (087)_r; \quad (m-n)_r = (005)_r; \quad (n-m)_r = (184)_r$$

Identify the radix r and the decimal values of m and n. [4 + 4]

Using decimal representation, m + n = 8r + 7, m - n = 5 and n-m = $-r^2 + 8r + 4$

(i) (m – n) + (n – m) = 5 + ($-r^2 + 8r + 4$) = 0 i.e. ($r^2 - 8r - 9$) = 0 = (r – 9)) (r + 1)
Taking only the positive value, we get r = 9.

(ii) Solving we get m = $(42)_{10}$ and n = $(37)_{10}$

Q4. A robot has **four** permitted directions of movement and **three** possible speed settings. Let the direction control and the speed control be applied through two bits each:

D_1D_0 = 00(forward) / 11(reverse) / 01(right) / 10(left), and

S_1S_0 = 00(zero, no movement) / 01(low) / 10(medium) / 11(high).

It is desired to have an electronic protection system to ensure that the robot can move at high speed for forward movement only and reverse only at low speed. This will have to be achieved by generating an output bit **P** which should go HIGH if any of these two conditions is violated, and then using **P** to shut off the power to the robot. Write down the Boolean expression for the output pin the sum of products form in terms of **D_1**, **D_0**, **S_1**, **S_0**. [6]

D_1D_0 \ S_1S_0	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	0	0	1	1
10	0	0	1	0

$$P = D_1 D_0 S_1 + D_1 S_1 S_0 + D_0 S_1 S_0$$

The Karnaugh Map is not necessary for the solution. The expression alone would do.