DVD Quiz 9

Total marks =10

Instructions

1. This is a take-home quiz, with no compulsion to join the meeting, but please ask your doubts in the meeting itself.

*2. The quiz duration is **25 mins and 10 mins** extra given to upload your scanned PDFs (high quality) on the google classroom. Upload answer PDF on classroom*

*3. The quiz starts at **8:00 PM** sharp and ends at 8:25 PM. 10 minutes are reserved for scanning and uploading the quiz to Google Classroom, any submission after **8:35 PM** will attract a penalty*

4. Meeting link for doubts: https://meet.google.com/pec-rvha-whi

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Q1. Suppose you have designed a chip and after fabrication it fails to meet either setup time requirement or hold time requirement. Which failure is more crucial and why. Give reasons?

[0.5 +1.5]

Q2. Why is Adaptive sequencing used in circuit design? Give a scenario to show how can adaptive sequencing reduce power consumption.

[1 +1]

Q3. You are given a pipeline stage as shown in fig 1. The clock frequency is 20ns and the setup ,hold and clock to Q time of all the flops are 3ns, 2ns and 1ns respectively. The combinational circuit has propagation delay of 10ns and contamination delay of 6ns.

(i) Does the circuit if fig 1 meet the setup and hold requirements?

[1]

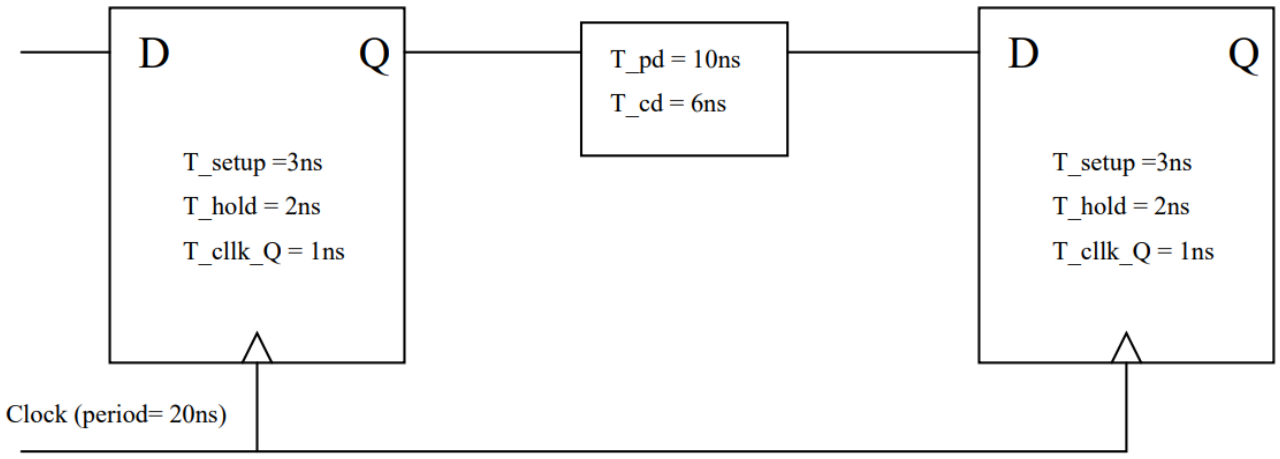

Fig 1

(ii) Now you want to break the pipeline stage into two stages so that you can double the clock frequency(clock period =10ns) , but at best you can break the combinational block into two blocks of propagation delays 7ns and 3ns and contamination delays of 3ns and 2 ns respectively as shown in the fig 2. Does this circuit meet the timing constraints? Show the violations (if any).

[1]

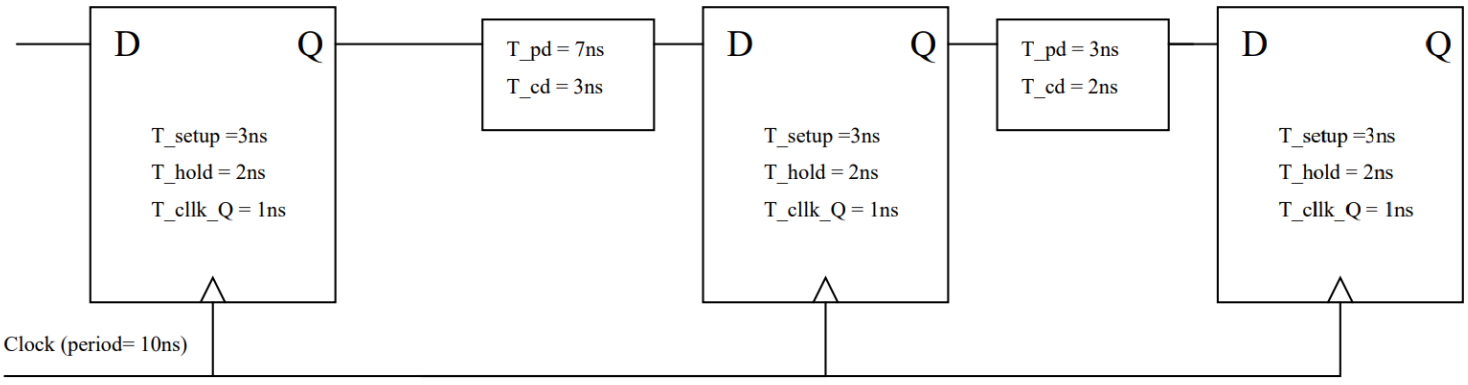

Fig 2

(iii) How can you remove the violations keeping the clock period 10ns only. (Hint : Use time borrowing)

[3]