INDRAPRASHTHA INSTITIUTE OF INFORMATION TECHNOLOGY DELHI

ECE 111 DIGITAL CIRCUITS

QUIZ NO. 4

1. How many FFs will be required to design following counters:
   a. Modulo 33 up/down counter
   b. Modulo 4096 up counter
   c. Modulo 64 binary counter
   d. Counter to count a sequence 2, 7, 9,17

   Justify your answers.

2. You are given a clock signal of 700 kHz. It is desired to obtain a 100 kHz clock signal with 50% duty cycle from given clock signal. Design the circuit to obtain the desired output.