DVD Quiz 4 Rubric

Question 1: Today's Markets are flooded with CMOS based devices. Considering a simplest CMOS circuit i.e. Inverter. State one advantage of CMOS inverter over BJT inverter.

Answer 1 [1 Mark]

a) Static Power dissipation is very less as compared to BJT Inverter.

b) The Output Swing of CMOS inverter is full rail to rail (VDD->GND).

Question 2: Explain the purpose of using strap cells in the design at regular intervals? What will happen if we will not provide the strap cells?

Answer 2

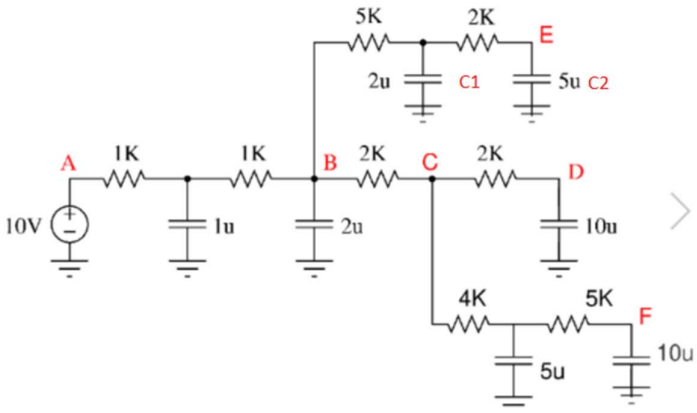
1. Strap cells are used to provide the VDD & GND connections to the substrate. By putting substrate taps at regular intervals (20um specifically for 65nm CMOS), Rsub (Substrate Resistance) is maintained to be low to prevent Latch up.

[1 Mark]

2.If we do not provide substrate connections problem of Latch Up will appear.

[1 Mark]

Question 3: Calculate the Elmore delay of path ABCF for the given RC network.



If the capacitances C1 & C2 are made double of their present values. Will it change the Elmore delay of the path ABCF? If Yes calculate the new delay.

Answer 3

The Elmore delay for a path takes into account

• All the resistances in the path

• And for each resistance taken, those capacitances which can be discharged or charged from current through resistor are only used

Hence, It will affect the Elmore delay of path ABCF.

Delay = 1K (1u+2u+2u+5u+10u+5u+10u) + 1K (2u+2u+5u+10u+5u+10u) + 2K(10u+5u+10u) + 4K (5u+10u) + 5K (10u) [1 Mark]

Delay = 1K(35u) + 1K(34u) + 2K(25u) + 4K(15u) + 5K(10u)

Delay = 35m + 34m + 50m + 60m + 50m

Delay = 229ms [2 Marks , 1 Mark deducted if unit not mentioned or wrong]

Yes, It will change the Elmore delay of the path [1 Mark]

New Delay = 243ms [2 Marks, 1 Mark deducted if unit not mentioned or wrong]

Question 4: List any 2 ways to alleviate crosstalk

Answer 4

Ways to decrease crosstalk are: (Any 2) – 0.5 Mark each

1. Use of low K dielectrics in inter-metal and intra-metal dielectrics, as capacitance reduces the cross talk reduces.

2. Shielding - Using a static voltage (like power supply) in between the transitioning signal lines decrease the crosstalk.

3. By increasing the spacing between the interconnects in the same layer and also between interconnects in different layers. As, the spacing increases, the capacitance associated with them decreases, and hence crosstalk decreases.