DVD Quiz 5

Rubrics

Q.1 A digital designer has been asked to improve the dynamic power consumption by reducing the activity factor of the circuit. Explain 2 ways in 30-40 words the designer can use to achieve this? **[2 Marks]**

Ans:

1. **Prevent Glitches:** Gates sometimes make spurious/erroneous transitions when inputs do not arrive simultaneously. These can lead to activity factor exceeding 1 and hence increase power dissipation. They can be avoided by proper timing of the signals during simulations. **[1 Mark]**
2. **Clock Gating:** It ANDs the clock signal with an enable to turn off the clock going into blocks which are idle in the system. Clock already has a high activity factor in an IC, so this method significantly reduces the overall dynamic power due to unwanted switching activity. **[1 Mark]**

If reason not explained clearly or only the methods are listed, deducted 0.5 marks each. Marks given for stating use of AND/OR gates also.

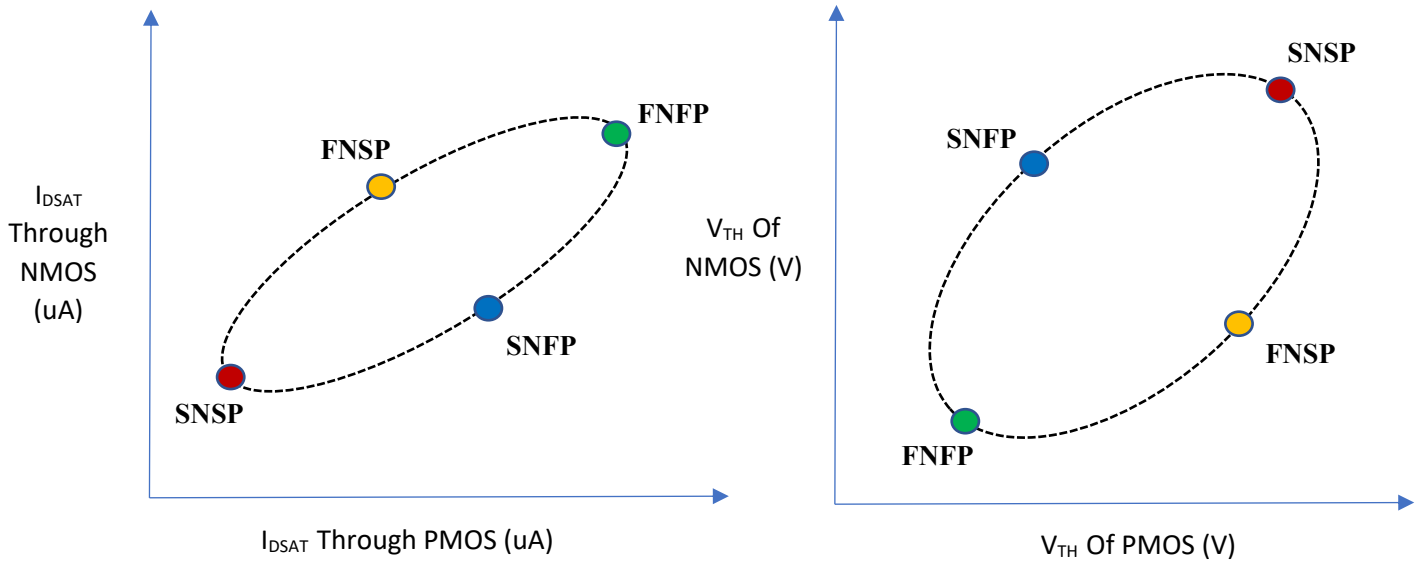
Q.2 Rahul, is a design engineer at a company X. While performing the verification process of a digital circuit at high voltage and low temperature, the delay specification is met. He expects the specification to be met at low voltage and low temperature also. But it is achieved at a higher temperature now. Explain the reason behind this? **[2 Marks]**

Ans: At high voltages, as temperature increases, scattering increases so mobility decreases, hence lower current flow. But at lower voltages temperature inversion sets in. The number of carriers in the conduction band are not sufficient. But now at higher temperature carriers have higher energy and they move faster. This effect dominates over the scattering effect which causes increased current and therefore faster corner.

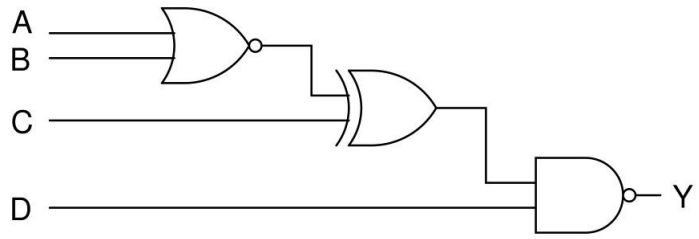
If temperature inversion is only mentioned (not mentioned) then 1 mark awarded (0.5 marks deducted).

Q3. Identify the location of SNSP, SNFP, FNSP, FNFP process corners on the curve for the given 2 distributions? **[2 Marks]**

Ans: 1 mark for each curve. 0.25 marks for each of the 4 corners identified.



Q4. a). Calculate the activity factor of the output node Y of the circuit given below. Show all the intermediate steps? It is given that the probabilities of inputs being high are P(A)=0.2, P(B)=0.3, P(C)=0.7, P(D)=0.4 **[3 Marks]**



b). The circuit shown above sees a total load capacitance of 20fF and is operated at 0.8V. The time period of the system clock is 1ns. Find the switching power of the circuit? **[1 Marks]**

Ans:

1 mark for finding probabilities at output of each of the 3 gates in part a).

0.5 marks for correct formula but wrong calculations in part b). 0.5 marks deducted if unit of power is not mentioned.