ECE 314/514 Digital VLSI Design
End Semester Examination
10:00 AM 09-December-2021

Maximum Marks: 30 Duration: 1Hr 45 Mins

Instructions

1. This is a take-home exam, you all should submit a single scanned pdf (high quality) in the classroom, before the deadline.
2. You need to mention your name, roll number, on your answer script.
3. You may choose to connect or not connect (to meeting) during the exam.
4. If you are taking any assumptions, please mention them clearly in your sheet and must make them visible distinctively.
5. Upload the whole sheet (including the rough sheet used) to avoid any plagiarism.
6. Use of calculators is allowed.
7. Institute plagiarism policy applies in this submission.
8. There is a **bonus question** in the question paper. It is over and above 30 Marks, and it's not mandatory to attempt it.
9. You can ask your doubts to any of us. Link is: https://meet.google.com/ksz-iumo-ugh
10. The answer sheet must be uploaded in the classroom within 1Hr 45 Mins (before 11:45 AM). **1Hr 30 Mins is for the exam and 15 minutes for uploading.**
11. There are a total of **9 questions** in the paper including the bonus.

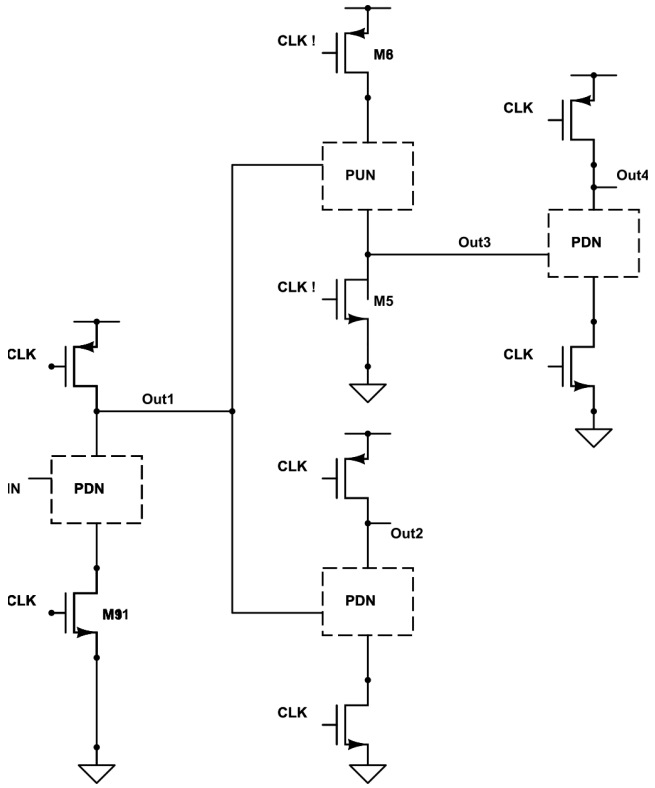
Q1. Give reasons for the following questions briefly: (**1*3 = 3 Marks**)

a). Use of strap cells for making layouts?
b). Leaving ½ DRC spacing while designing layouts in standard cell topology?
c). Width of the standard cell is a multiple of 0.2 in the 12T library?

Q2. **Fill in the Table:** Explain the impact of the following manufacturing events on drain current for a given gate-source voltage of an N-MOSFET? **(1*4 = 4 Marks)**

Events	Impact on I_{DS}	Explanation
Growth of thicker gate oxide	_____	_____
Extra poly etching	_____	_____
Extra etching of oxide when creating windows for source/drain implants	_____	_____
HfO_2 is used as dielectric rather than SiO_2	_____	_____

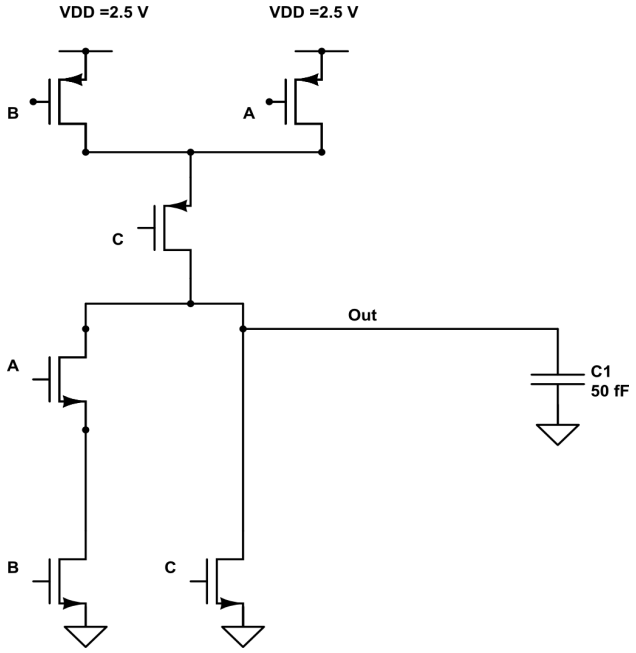
Q3. Consider the circuit given below. Pull-down/Pull Up network can be considered as a single NMOS/PMOS device. Assume that evaluation time, precharge time & propagation delay all are T/2. (Note: CLK! is inverted of CLK) (**6 Marks**)



a). Detect the problems (if any) in the circuit during the 1→0 & 0→1 transition. If any problem exists, how do you resolve it by inserting one inverter somewhere in the circuit? **(2 Marks)**

b). For the corrected circuit draw the timing diagram for Out1, Out2, Out3, Out4. Assume a clock period of 10T and the IN signal going high before the rising edge of CLK. **(4 Marks)**

Q4. Consider the circuit as shown below: **(5 Marks)**



a) What is the logic function implemented by the circuit? **(1 Marks)**

b) What input vectors will cause the worst leakage power for both HIGH & LOW output values? **(1 Marks)**

c) Consider the probability of each input being high = 0.5 and every input is independent. What will be the activity factor of the output of the circuit? **(2 Marks)**

d) Calculate the dynamic power of the circuit if the inputs switch at a frequency of 100MHz? **(1 Marks)**

Q5. Which circuit (between fig1 and fig2) will you prefer for designing the latch and why? If you use a tristate buffer, which input (CLK or OUT) will you apply as the inner input and why? **(2+2 = 4 Marks)**

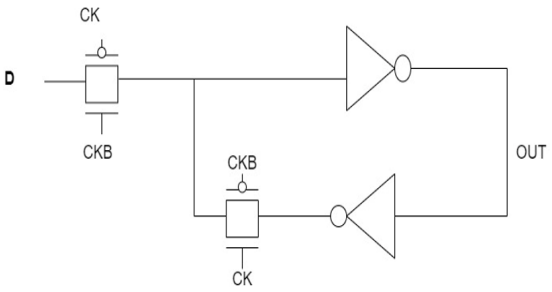


Fig 1

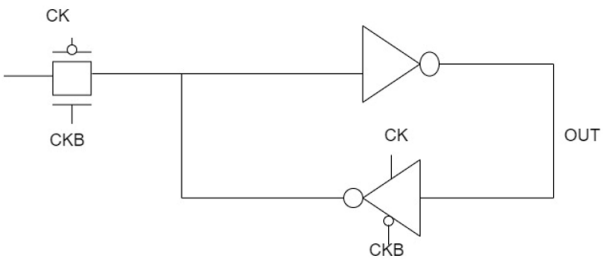
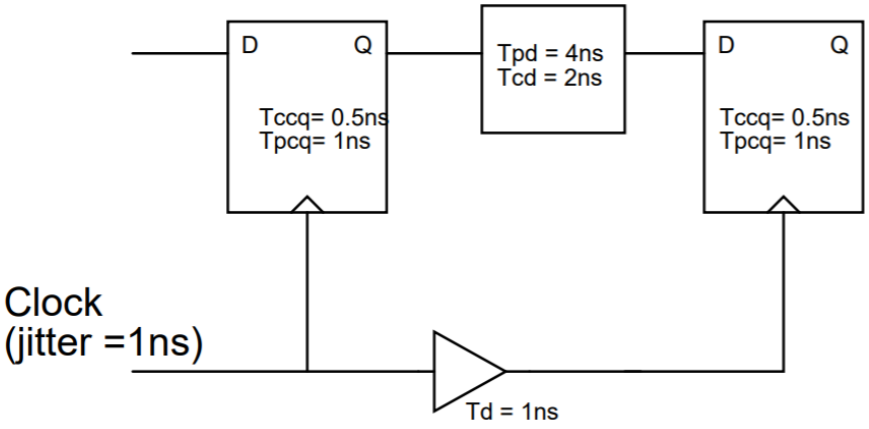


Fig 2

Q6. What do you mean by sequencing overhead? Why does a FF need to satisfy setup time and hold time constraints? Explain in detail. **(1+2 = 3 Marks)**

Q7. For the circuit shown below calculate the setup and hold slack for a clock period of 10ns. Both the flops have setup and hold time of 2ns and 1 ns respectively? Note: Slack is the extra time/margin available after meeting the setup or hold requirement. **(2 Marks)**



Q8. It is given that the **Kill** signal = **A'.B'** and the **Propagate** signal = **A xor B** for a full adder. Represent Sum and Carry-out in terms of Kill & Propagate (instead of Generate & Propagate)? **(3 Marks)**

(Bonus Question - Optional)

Q9. Electromigration (EM) is a failure mode in which high current density could lead to defects, voids in metal interconnects. Since the thickness of wires is already fixed for a given technology, a designer can only change the width of the wire to reduce current density and prevent EM. Assume that the EM limit is J_{AL} = 1.0 mA/um (J_{AL} should not be higher than this, o/w failure would occur) and VDD = 1.8 V **(3 Marks)**

a). Find the required widths of power and ground wires connected to a 500 MHz clock buffer that drives 5pF on-chip capacitance? **(2 Marks)**

b). Suppose that the clock buffer is 400um away from both the power and ground pads. The rise and fall times of the clock are the same and equal to 200 ps. What is the ground bounce with the chosen size of wire? Assume wire resistance to be 57 mOhm/square. **(1 Marks)**

----------BEST OF LUCK----------