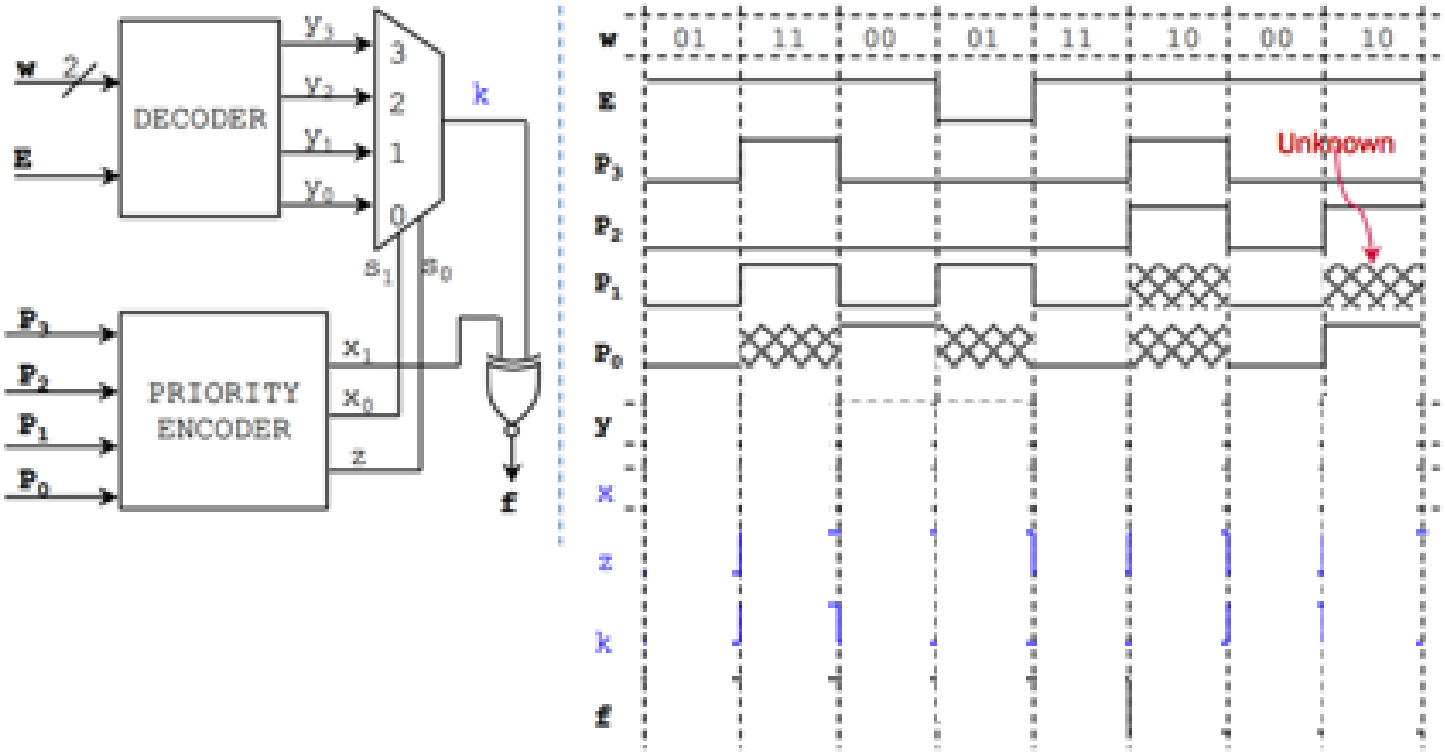
ECE111: Digital Circuits Quiz 3

Date: March 20, 2021

- Duration: **30 minutes**
- Cheating: Action as per recent Institute policy
- There are two questions spread over two pages.

1. Complete the timing diagram of the circuit shown below. The output z of the priority encoder is the valid bit indicator. The signal x and y is to be represented compactly as x_1x_0 and $y_3y_2y_1y_0$, respectively. **[5 Marks]**



Note: In the slots allotted to y and x write the values in binary format, as is given for w, not as a waveform, while f or z k and f draw the waveform, as is given for e, P_3, P_2, P_0.

2. Consider the circuit shown below where the output of a 3-bit adder needs to be displayed on the two digits of the 7-segment display. For example, if the adder output is 9, then circuit should display 09 where 0 should be displayed on left display and 9 on right display. Existing BCD-to-7 segment decoder works only when input number is between 0 and 9 and we have to use it since it has been hardwired to 7-segment display board. You need to design combinational circuit between Adder and 7-segment decoder (shown as question mark in the Figure below) so that the adder output is correctly displayed on the 7-segment display. **[5 Marks]**