DVD MIDSEM RUBRICS 2021

Q1.

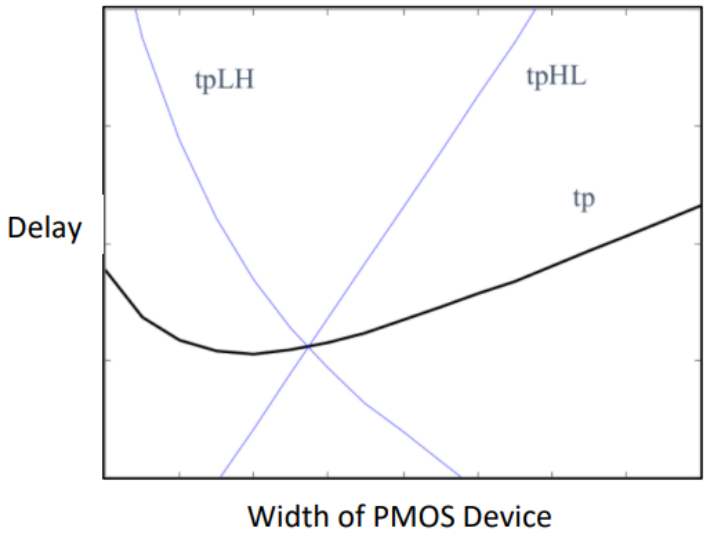
a) Give reason as to why Tungsten is used in making contacts during fabrication and not Copper? And why Copper is used in making wires, but not Tungsten? **(2 Marks)**

Solution: **Contacts** are made only of Tungsten and not copper because copper can readily diffuse into the silicon lattice and create intermediate energy states in the band gap of silicon. Hence silicon may no longer behave as a semiconductor **(1 marks).** For making **wires**, copper is preferred because of its lower resistivity and high ductility **(1 marks).**

b) While making the layout, why NP/PP layer is drawn over the Poly (PO) layer to cover it? **(2 Marks)**

Solution: By using NP/PP layer we dope the Poly layer and deposit the Salicide layer over polysilicon to reduce its resistivity. *Additionally, by doping the Poly layer (doping of gate), we keep the Vth of the device under control.*

c) Explain the trend of tpLH & tpHL from the graph shown below, considering the case of a simple CMOS inverter. Elaborate, why the overall propagation delay rises after falling initially? **(2 Marks)**



Solution: Increasing the size of the PMOS device lowers the ON resistance of the MOS, allowing for larger current to flow, which charges the load capacitor quicker, hence reducing the time for output to rise from 0 to Vdd, hence rise delay is lesser. The fall delay increases as though the ON resistance of the PMOS decreases, the larger

diffusion capacitance of the increased PMOS dominates the overall RC delay as more time is required to discharge a larger cap to GND.
Note: The reduced-ON resistance of the PMOS doesn't show in tpHL path of Elmore model. Initially as the size of PMOS increases the overall current driving capability increases, hence propagation delay decreases. However, when the size of devices is increased, further incremental reduction in resistivity is less. But the diffusion capacitances increase due to larger size, and the Self-Loading effect starts to dominate the overall delay of the gate.

d) It is required to increase the propagation delay of a CMOS inverter. Without adding more stages or changing the sizes of the transistors , suggest how the delay can be increased. You can use additional NMOS/PMOS's? **(2 Marks)**

Solution: We can make a stacked inverter by adding one nmos to the pulldown stack and one pmos to the pullup stack. (Show in schematic required)

Q2. Answer the following questions:

i. Draw schematic for the CMOS logic given by $\overline{(A+B).(C+D)}$ **[1 marks]**

ii. Size the transistors to match the resistance of a unit inverter and show on the schematic.

[1 marks]

iii. Draw the stick diagram considering appropriate sharing of source and drain regions.

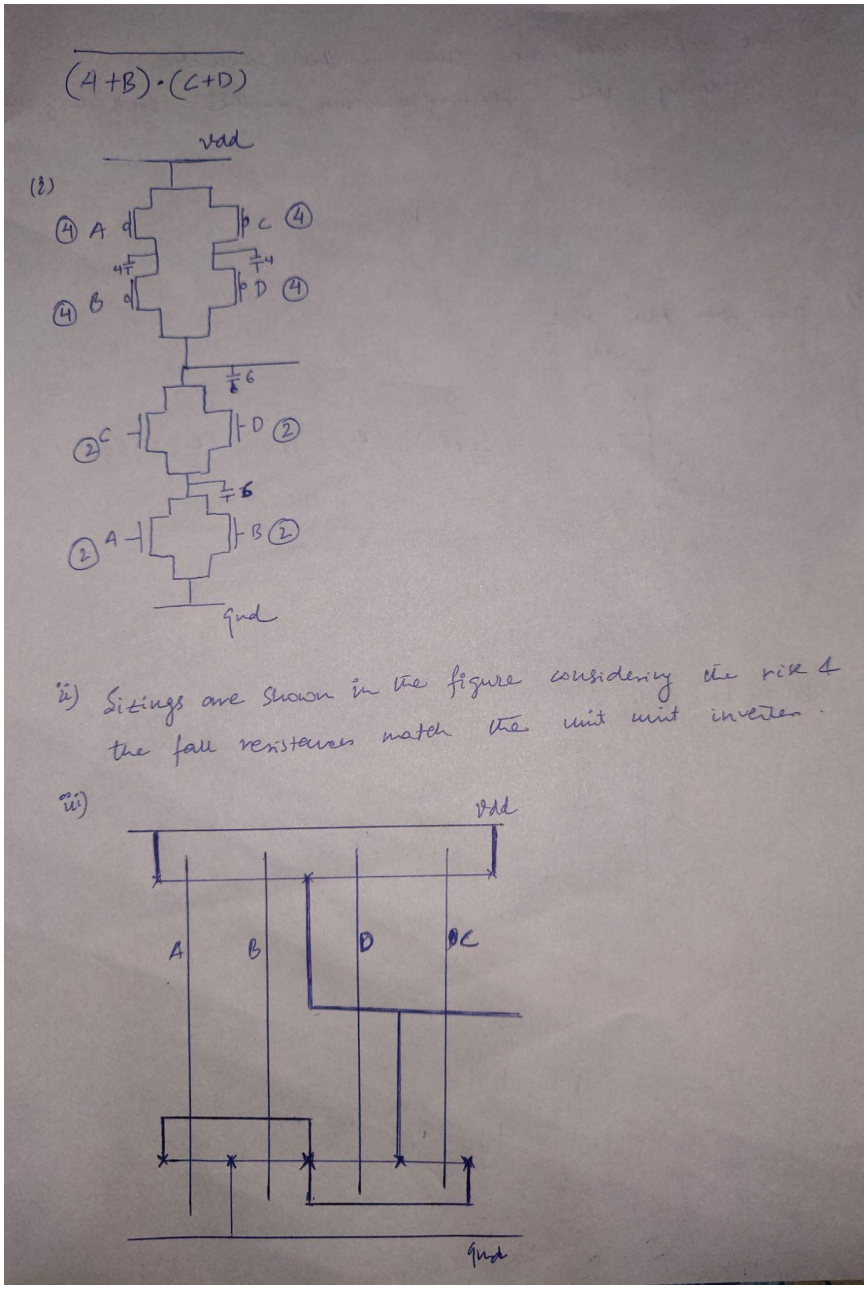
[3 marks]

iv. Show the capacitances of all the nodes in the schematic **[1 marks]**

v. Estimate the propagation delay for rise and fall in terms of RC. **[2 marks]**

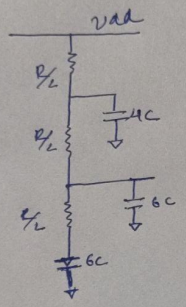
vi. Estimate the contamination delay for rise and fall in terms of RC **[2 marks]**

Solution:


$\overline{(A+B)\cdot(C+D)}$
(i)
Vdd
A
B
C
D
gnd
(ii) Sizings are shown in the figure considering the risk & the fall resistances match the unit unit inverter.
(iii)
Vdd
A
B
D
C
gnd

iv) The capacitances are shown in the schematic considering the sharing as shown in the stick diagram

v) Propagation delay rise

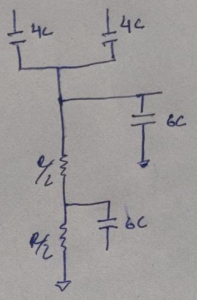


$$\left(\frac{R}{2}\times 4C\right)+\left(\frac{R}{2}+\frac{R}{2}\right)6C+\left(\frac{R}{2}+\frac{R}{2}\right)6C$$

$$= 2RC + 6RC + 6RC$$

$$= 14RC$$

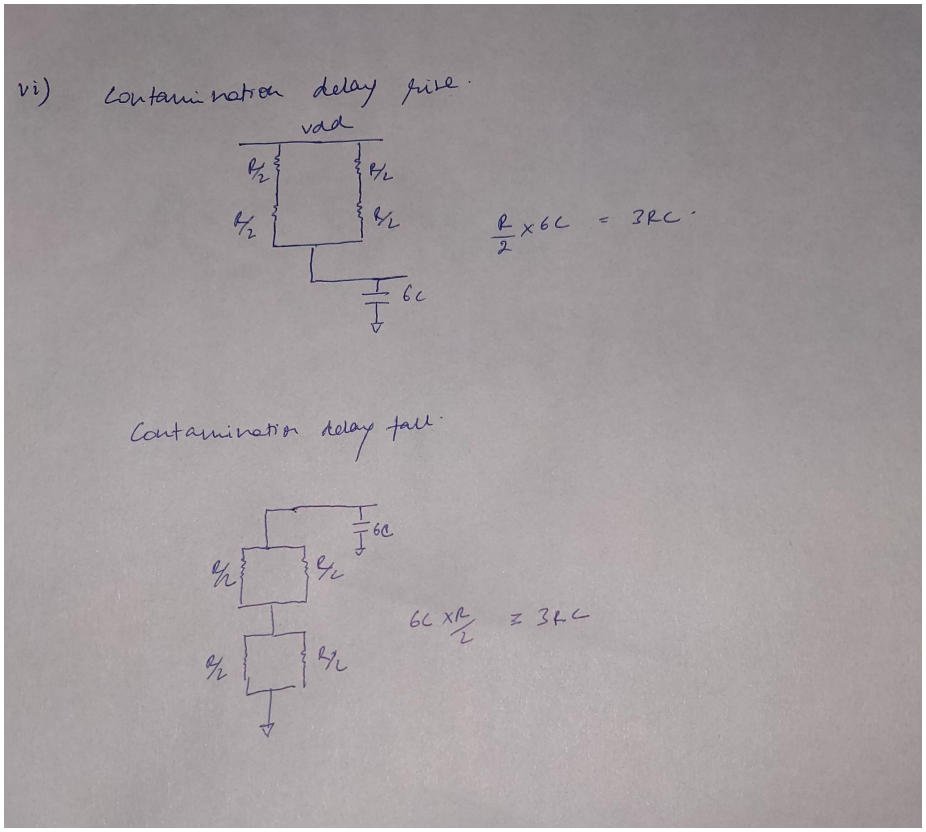
Propagation delay fall



$$\left(\frac{R}{2}\times 6C\right)+\left(\frac{R}{2}+\frac{R}{2}\right)6C+\left(\frac{R}{2}+\frac{R}{2}\right)8C$$

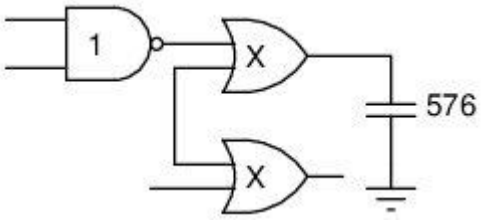
$$3RC + 6RC + 8RC$$

$$= 17RC$$



Propagation delay	**rise**	14RC
	fall	17RC
Contamination delay	**rise**	3RC
	fall	3RC

Q3. Consider a combinational logic driving a 576 unit load (H=576) as shown below.

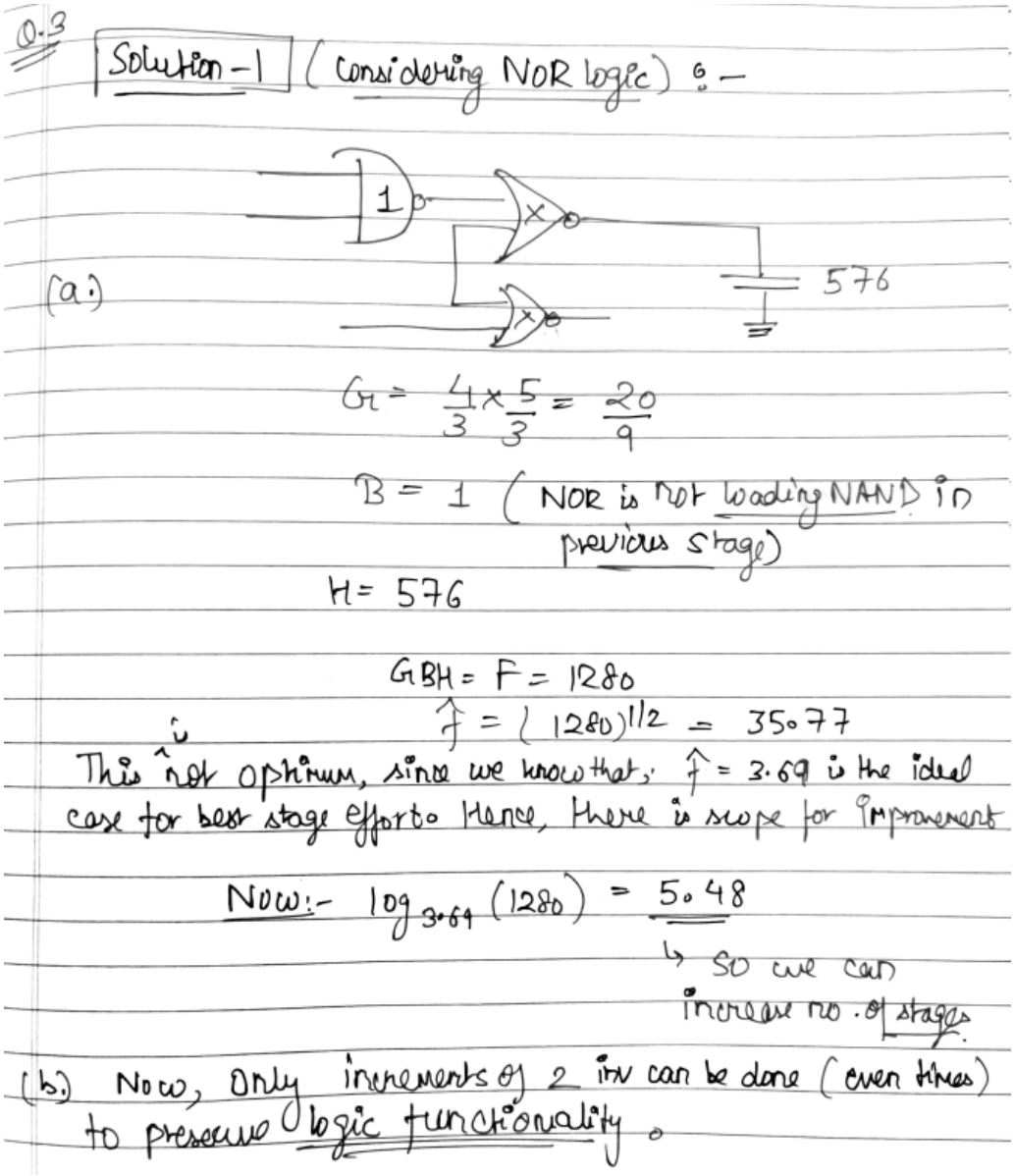


a). Is this implementation of the circuit optimum in terms of delay? Support your answer with a suitable explanation briefly. **[2 Marks]**

b). Propose different topologies and calculate the least possible path delay. Hint: You have to ensure that overall logic functionality should be well preserved. **[5 Marks]**

Solution:

Marks are awarded if you had chosen to use either NOR or OR logic in the second stage.



Let N = 4 (i.e add 2 inverters)

$$\text{Delay} = 4 \times (1280)^{1/4} + 6$$

$$= 38.92 \text{ units}$$

Let N = 6 (i.e add 4 inverters).

$$\text{Delay} = 6 \times (1280)^{1/6} + 8$$

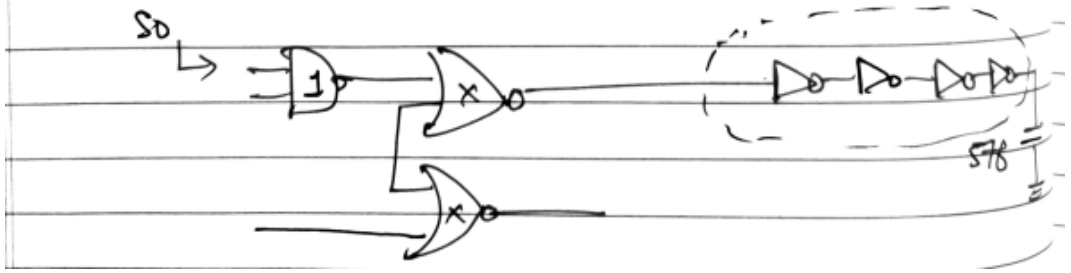
$$= 27.81 \text{ units}$$

Let N = 8 (i.e add 6 inverters)

$$\text{Delay} = 8 \times (1280)^{1/8} + 10$$

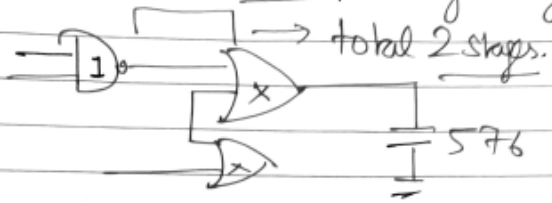
$$= 29.56 \text{ units}$$

Best delay when N = 6 i.e 27.81 units



Solution-2 :→ (OR logic)

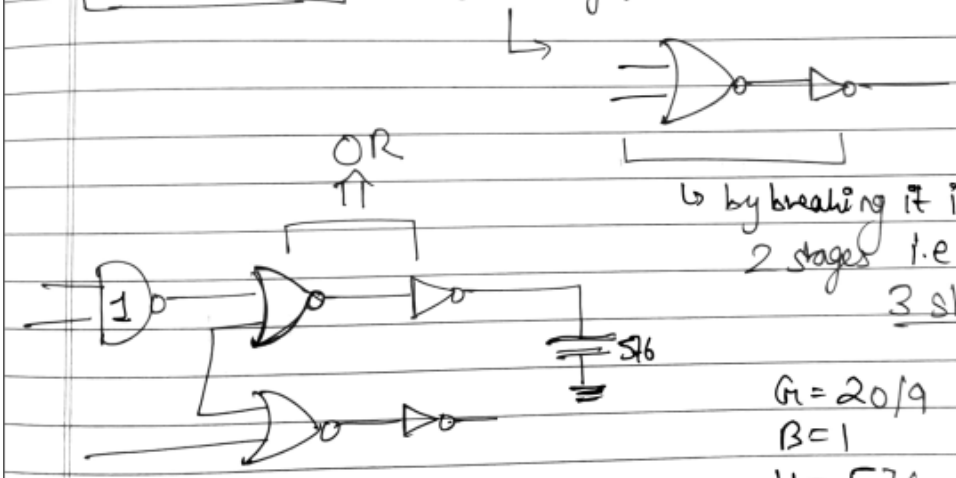
→ If someone has considered OR in a single stage i.e



→ total 2 stages.

→ Then also Marks awarded → same answer as that in Solution-1.

Solution-3 :→ (OR logic)



↳ by breaking it into 2 stages i.e total 3 stages.

G = 20/9
B = 1
H = 576

(a.) F ⇒ GBH = 1280

$\uparrow = (1280)^{1/3} = 10.85$

* N=3

Again, this not optimum since ideally best stage effort can be 3.69.

As seen in soln.1 → ideal stages = 5.48

(b.) Again, only increments of 2 INV can be done to preserve logic.

∴, Check at N = 5 (i.e add 2 inverters)

$$D = 5 \times (1280)^{1/5} + 7$$

$$= 27.91 \text{ units}$$

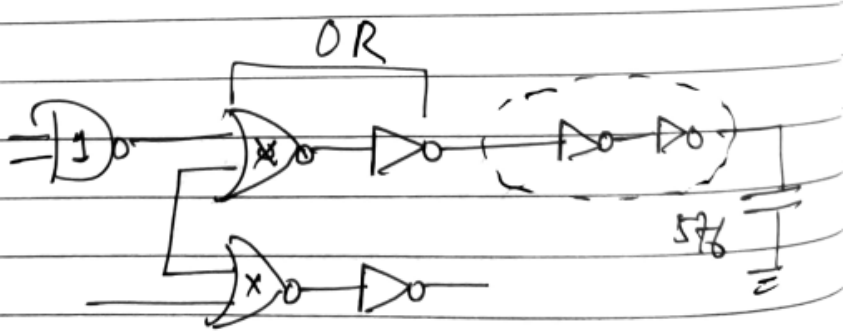
Also, check at N = 7 (i.e add 4 inverters)

$$D = 7 \times (280)^{1/7} + 9$$

$$= 28.44 \text{ units}$$

Best delay when N = 5 i.e 27.91 units

So,



Q4. [Bonus Question - Optional]
A product is designed in 90nm technology and takes up 100mm2 area. Its Yield is 56%. It is sold for Rs. 100/-, at a profit of Rs.10. The designers use a denser version of libraries to reduce the area to 80mm2. What is the new expected Yield? **[1 mark]**. The product is still sold for Rs.100/-. How much profit does the company make now per product sold? **[2 marks]**.

Solution:1
Assume that 100 dies were manufactured per wafer.
At 56% yield, every wafer earns Rs.5600/-

At this sale price, profit is Rs.560/- (Rs. 10/- per die sold).

Yield is inversely dependent on Area. When Area reduces to 80mm2. Yield changes to 56/(0.8) = 70% **[1 mark]**

Total dies made now = (100/80)*100=125
Therefore no of non-defective dies are= 125*0.7=87.5 which is equivalent to 87.

So, now 31 extra dies can be sold at Rs.100/-

Extra profit = Rs. 3100/-

Total profit = Rs. 3660/-
Profit per die = 3660 / 87 = Rs. 42 (approx) **[2 marks]**