DVD Quiz 5

Duration: 25 Mins **Marks: 10**

Instructions

1. This is a take home quiz, no compulsion to join the meeting, but please ask your doubts in the meeting itself.

2. The quiz duration is 25 mins and 10 mins extra is given to upload your scanned PDFs (high quality) on the classroom. Upload answer PDF on classroom.

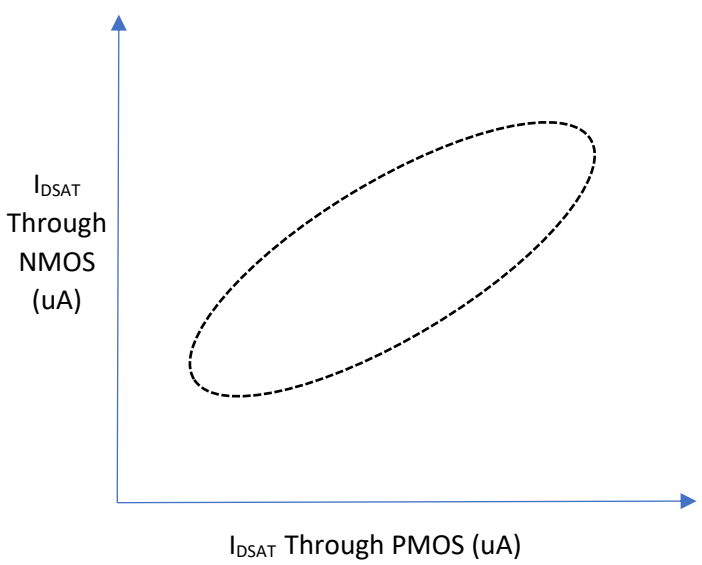
3. Quiz starts at 8:00PM sharp and ends at 8:35PM. Late submission will attract a penalty of 1 mark deduction every minute.

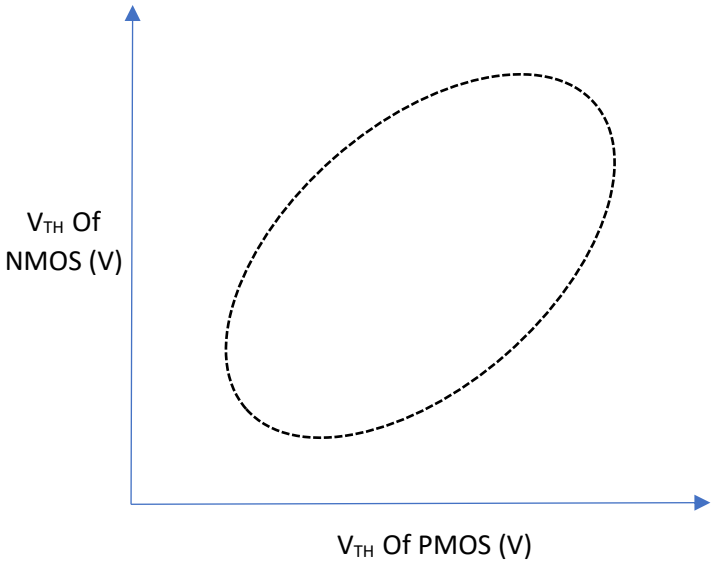
4. Meeting link for doubts: https://meet.google.com/yyv-ixnb-ztu

Q.1 A digital designer has been asked to improve the dynamic power consumption by reducing the activity factor of the circuit. Explain 2 ways in 30-40 words the designer can use to achieve this? **[2 Marks]**

Q2. Rahul, is a design engineer at a company X. While performing the verification process of a digital circuit at high voltage and low temperature, the delay specification is met. He expects the specification to be met at low voltage and low temperature also. But it is achieved at a higher temperature now. Explain the reason behind this? **[2 Marks]**

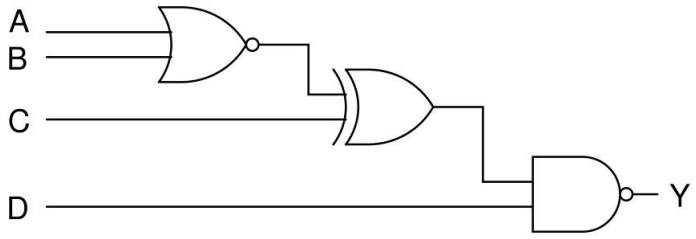
Q3. Identify the location of SNSP, SNFP, FNSP, FNFP process corners on the curve for the given 2 distributions? **[2 Marks]**





Q4.

a). Calculate the activity factor of the output node Y of the circuit given below. Show all the intermediate steps? It is given that the probabilities of inputs being high are P(A)=0.2, P(B)=0.3, P(C)=0.7, P(D)=0.4 **[3 Marks]**



b). The circuit shown above sees a total load capacitance of 20fF and is operated at 0.8V. The time period of the system clock is 1ns. Find the switching power of the circuit? **[1 Marks]**

----------BEST OF LUCK----------