ECE-314/514 - DVD End Semester Examination

Marks: 25 **Duration: 1 Hr 20Mins**

Submission on Classroom: 4:40 PM **Date: 12-Dec-2020**

Instructions for evaluation:

1. Similar to previous evaluations, this is a take home examination.
2. There is no compulsion to join the meeting, but join in case you have any doubts or any other issue.
3. The exam will commence will start sharply by 3 PM, the duration is of **1 Hr 20 mins**, and extra 20 mins are given to upload the **high-quality scanned pdf** on classroom by **4:40 PM**. Late submissions will be penalized.
4. Institute plagiarism policies strictly applies in this submission.
5. Please include steps in all the answers, which have numerical calculation. Also, explain with help of circuit diagram, where ever required. No marks will be awarded in absence of steps.
6. Please take assumptions wherever necessary and state your assumptions distinctly.
7. There is a Bonus que in Q1 of 2 marks and in Q3 of 1 mark. Bonus in Q1 is if all 5 are answered.
8. The meeting link for doubts is: https://meet.google.com/oeo-oouc-tme

Que 1. Given below are some design failures/challenges, given the design and the causes of failure, identify the cause of failure [1 Mark] and give suggestions to prevent/rectify them [1 Mark].
(Solve any 4). Solve all 5 for BONUS 2 Marks. **[8 Marks+2 BONUS]**

a. When a design was fabricated and tested, it was observed to fail at 900MHz, though the sign-off was done at 1GHz? This happened often for Slow lots, while Typical and Fast lots were functional at 1GHz also. What failure does it point to? [2 Marks]

b. A design was found to do incorrect computations when operated at high voltage. At lower voltages, such failures disappeared. Changing the frequency of operation did not help. What failure does this point to? [2 Marks]

c. A very high-speed processor was designed using Dynamic gates. It operates perfectly initially. However, after some time of operation, some computations start to be erroneous. This happens more in summers. Switching OFF and ON quickly doesn't help. But waiting for a few minutes lets it operate normally. Also, when the load on the processor is less, this problem doesn't appear. What could be the reason? [2 Marks]

d. Sometimes, at power-ON, a processor consumes a lot of power. When RESET pin is asserted, power consumption reduces to normal. This design used a new architecture of sequential elements. What could be the problem? [2 Marks]

e. Jaduguda is the oldest Uranium mine in the country. When you visit the villages nearby, you will notice that many people have physical abnormalities. Incidentally, your phone also behaves very quirky there. What could be the reason? [2 Marks]

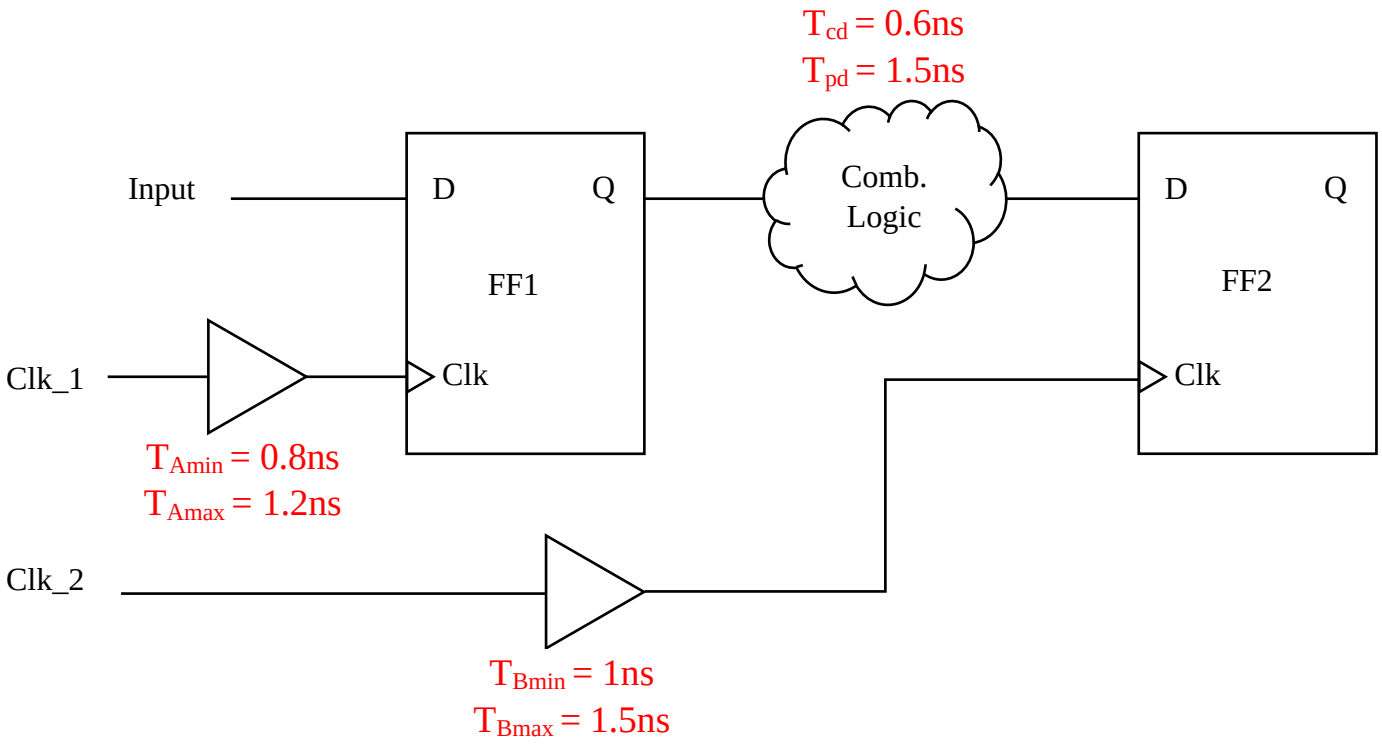
Que 2. For the given circuit, assume both the clocks have same time periods. Show all the steps, else no marks would be awarded. Given, for both the FFs, Tcq_{min} = 0.4ns, Tcq_{max} = 1ns, T_{setup} = 0.5ns, T_{hold} = 0.5ns. Calculate the following: **[7 Marks]**

a. Calculate minimum time period for operation. [1 Mark]

b. If the both the clocks have a jitter of 100ps, find the new minimum time period. [2 Marks]

c. If Clk_2 has positive skew of 200ps (additional to the skews given from buffers), what is the new time period. [2 Marks]

d. Check for any setup and hold violations with relevant equations, if the clock period is 3.5ns (without jitter), In case of violations state any 2 methods of removing the setup violation. [2 Marks]



Que 3. Solve the following: **[10 Marks+1 BONUS]**

a) Should we use XOR gates (designed using Transmission gates) in standard cell design? Explain briefly. [1 Mark]

b) What is time borrowing? What is the timing constraint in adjacent stages, so that latches can borrow time? [2 Marks]

BONUS QUE:
How can we enable time borrowing in FF based sequencing? [**BONUS** 1 Mark]

c) Compare among FF, Pulse latch and regular latch, which one is best among others and explain the reason (one point each) on below figure of merits: [4 Marks]

1) Performance
2) Power
3) Area
4) Robustness

[Hint: If Latch is the best among all three in some PPA, then explain why latch is better from the other two, do this for all 4 merits listed above]

d) Match each element of column A, with one of column B and C each. [3 Marks]

Design Style (A)	**Figure of Merit (B)**	**Applications (C)**
Dynamic	Robust	Column Decoder
Static	High Density	Medical Applications
PTL	High Performance	Processor

---------- BEST OF LUCK ----------