ECE 314/514 Digital VLSI Design
Mid Semester Exam
22-Oct-2022

Max Marks:30 **Duration:75 mins**

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Instructions:

1. **This is a closed book exam**
2. Use of calculators is allowed.
3. Question paper contains 8 questions. Please answer all the questions
4. For Question-1, B.Tech students may attempt any 3 of the 5 parts. The extra 2 parts will be considered for **'bonus'** marks.
5. If you are making any assumptions, please mention them clearly in your sheet.
6. Institute plagiarism policy applies in this submission.

Q1 Explain Briefly:
Note: Btech students can attempt any 3 of the following subparts, rest 2 will be considered as bonus marks for them.

(a) Explain what is the difference between the value of gate capacitance observed in the inversion region for MOS cap and MOSFET? [CO1] **[1 marks]**

(b) Explain why multiple contacts are placed on the diffusion layer to connect it to metal 1 layer? What is the disadvantage of putting just one contact? [CO1] **[1 marks]**

(c) Why is 1/2 DRC spacing maintained when designing standard cell layouts? [CO1] **[1 marks]**

(d) What is Dishing? How do we prevent it? [CO1] **[1 marks]**

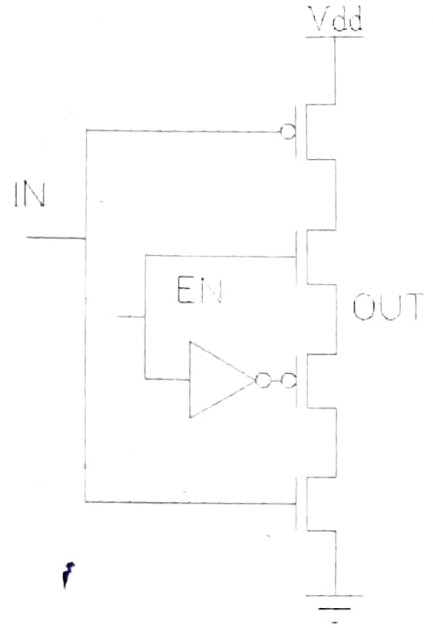
(e) Where do we use low-k dielectric and why? [CO1] **[1 marks]**

Q2 Explain:

(a) You observed that a particular lot was manufactured at SS corner and some chips are failing due to the same reason. You decide to use process compensation. Explain how can this recover the failing chips and what is the tradeoff involved (disadvantage of doing it)? [CO2] **[1 marks]**

(b) Why does subthreshold current increase with increase in temperature and ON current decrease with increase in temperature? [CO3] **[1 Marks]**

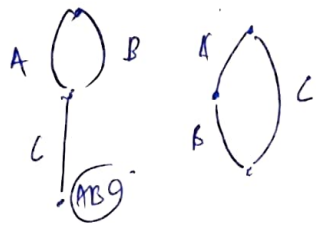
Q3. A designer proposed a tri-state inverter circuit as follows. The functionality desired is that when EN = VDD, then the circuit should behave as an inverter. [CO 1]



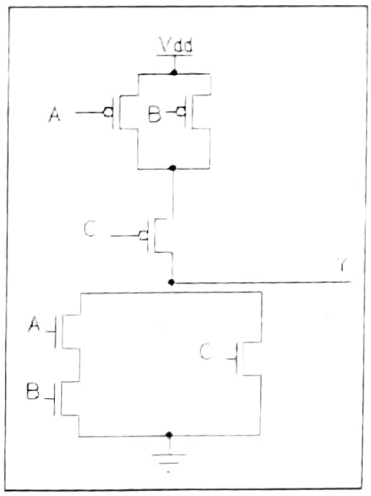
Desired functionality:-
When EN = VDD, IN = VDD, OUT = GND,
When EN = VDD, IN = GND, OUT = VDD
When EN = GND, OUT = floating

(a) What will be the output logic levels? Why? **[1 marks]**

(b) Propose the corrected design. **[1 marks]**



Q4. For the given schematic answer the following questions :

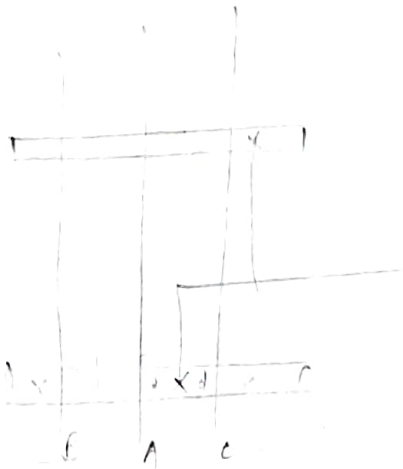


(a) Identify the CMOS logic represented above and size the transistors to match the resistance of a unit inverter. [CO 1] **[1 marks]**

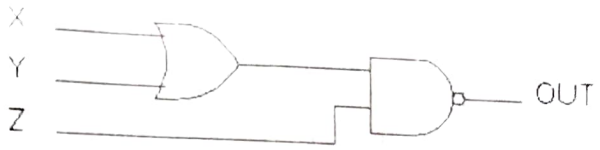
(b) Draw the stick diagram considering appropriate sharing of source and drain regions. [CO 1]**[2 marks]**

(c) Estimate the propagation delay for rise in terms of RC. [CO 1]**[1 marks]**

(d) Estimate the contamination delay for fall in terms of RC. [CO 1]**[1 marks]**



5 For the circuit here, answer the following questions:



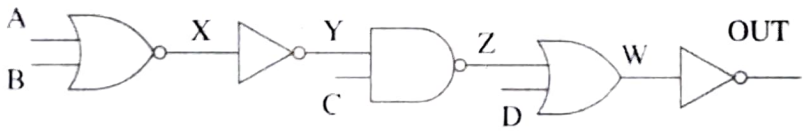
(a) Find the logical effort for the input X, considering driving a 50 unit load (H=50). Hint: You can consider OR logic by combination of NOR and NOT gate. You have to ensure that overall logic functionality should be well preserved. [CO 2]**[2 marks]**

(b) Consider the Probability of each input = 0.5 and every input is independent. What will be the activity factor of the circuit? [CO 3] **[1 marks]**

(c) Calculate the dynamic power of the circuit if the input frequency is 100MHz, output load of 50fF and supply voltage 1.08V? (ignore self-loading and short-circuit currents). [CO 3]**[1 marks]**

(d) How we improve dynamic power consumption by reducing the activity factor of the circuit. Explain any 2 ways. [CO 3]**[1 marks]**

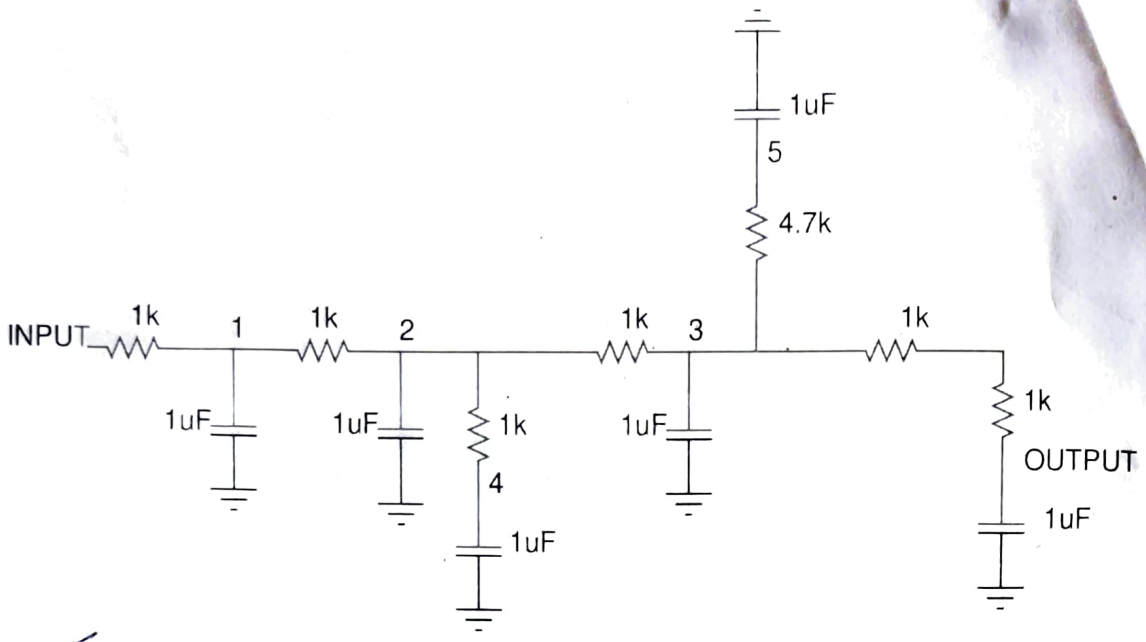
Q6. For the given circuit calculate the activity factor at OUT considering all inputs to be independent. [CO 3] **[2 Marks]**



Q7. Complete the below table and Explain the reason for your answer. (Worst PVT conditions of different FOMs for CMOS Inverter). [CO 2-CO 3] **[6 marks]**

Figure of Merits (FOM)	Process	Voltage	Temperature
Delay (propagation)			
Leakage Power			

1010 → 10
1110 → 14
0110 → 6



Q8. The above figure presents the lumped RC model of some circuit. We know beforehand that this circuit will work properly if the time taken for the output voltage to rise from 0V to Vdd/2 (for a stepped input) is less than 12 ms. Verify whether the above circuit meets this specification. (1,2,3,4 and 5 are node numbers for your easy reference).[CO 3] **[3 marks]**