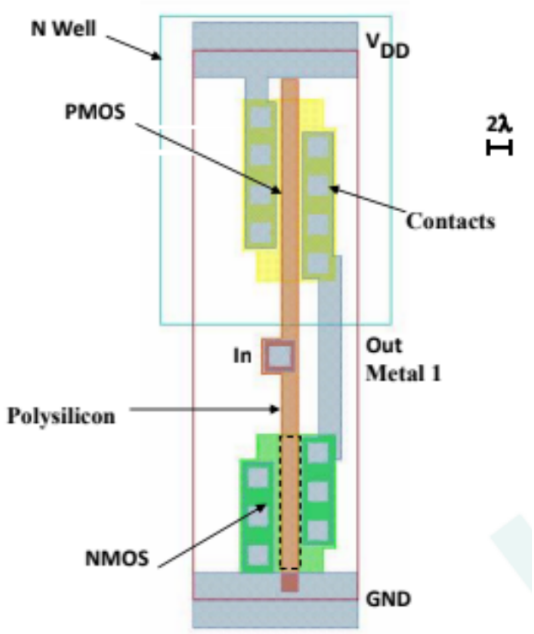
DVD MIDSEM RUBRIC:MONSOON 2022

Q1: Any 3 of the following for Btech

(a) Explain what is the difference between the value of gate capacitance observed in the inversion region for MOS cap and MOSFET? [1 Marks] (CO1)
Ans: There is no difference in capacitance as observed at low frequencies. However, at high frequencies, capacitance observed in the inversion region in MOSFET is higher than that of the MOSCAP. This is due to the fact that the charge that is required in response to the gate voltage change is supplied by the source/drain regions whereas they are provided by the bulk in the case of MOSCAP. Effectively, the gate capacitance in MOSCAP in the inversion region becomes a combination of two series combinations which decreases its value.

(b) Following is a layout of the inverter. (CO 1) [1 Marks]



Explain why multiple contacts are placed on the diffusion layer to connect it to metal 1 layer? What is the disadvantage of putting just one contact?
Ans: Multiple contacts are used to decrease the contact resistance [¼ mark] and offer redundancy [¼ mark] in case one of the contacts is mal-formed.
If we do not provide sufficient contact area by deploying a number of contacts, then it can result in higher contact resistance which will result in higher rise/fall times and degraded performance. Also, it increases IR drop causing power loss. [½ mark]
More contacts than necessary result in increased poly to contact capacitance and hence Gate-Drain, Gate-Source capacitances increase. These degrade circuit performance.

(c) Why do we leave 1⁄2 DRC spacing while designing layouts in standard cell topology?

[1 marks] (CO1)

Ans: In standard cell topology, one cell is abutted with another cell. Now if one leaves 1⁄2 the minimum DRC requirement across cell sharing, then after abutment, 1 full DRC is met. This will enable abutting cells at minimum possible spacings saving the area and time/effort to make DRC clean layouts.

(d) What is Dishing? How do we overcome it? [1 marks] (CO1)

Ans: Copper is a soft ductile metal which is surrounded by a barrier like Titanium Nitride. After chemical mechanical planarization (CMP), there may be some metal particles remaining on the surface of dielectric even after removing the extra metal layer. Hence, we do extra polishing that leads to erosion of copper in case of thick wires. This is called dishing. This increases the resistance of the wire.

In order to avoid dishing, slots are made in the wires of certain spacing. Slots are filled with SiO2, which now acts as pillars of higher mechanical strength and prevents the wires from dishing during CMP.

(e) Where do we use low-k dielectric and why ? [1 mark] CO1

Ans : Low K dielectrics are used in intermetal and intermetal dielectric. Reason to use Low-k dielectric : To keep the parasitic capacitance between interconnects low at lower technologies also. As, in lower technologies spacing between wires decreases, lower K is desired to decrease the inter and intra metal capacitance. This reduces the RC delay; crosstalk decreases and power consumption decreases.

Q2.

(a) You observed that a particular lot was manufactured at SS corner and some chips are failing due to the same reason. You decide to use process compensation. Explain how can this recover the failing chips and what is the tradeoff involved (disadvantage of doing it)? [1 marks] (CO 2)

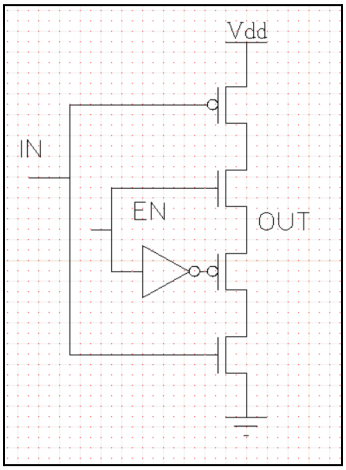
Ans: Process compensation can be performed by applying forward body bias [½ marks]to the chips. Similarly, leaky FF lots can be put in reverse body bias. This is called adaptive body biasing. Disadvantage of this approach is that leakage increases drastically by doing this. Another way to recover such dies would be to operate them at higher voltage. [½ marks] This is called Adaptive Voltage Scaling.

(b) Why does subthreshold current increase with increase in temperature and ON current decrease with increase in temperature?[1 Marks] (CO 3)

Ans: ON current is constituted by free carriers present in the conduction band. As we increase the temperature, the number of collisions between the charge carriers increases and hence the mobility of the carriers decreases which decreases the ON current. On the other hand, in subthreshold operation, there is a lack of free carriers. As the temperature increases in the

subthreshold region, carriers are generated due to thermal generation and due to availability of more charge carriers, the subthreshold current increases.

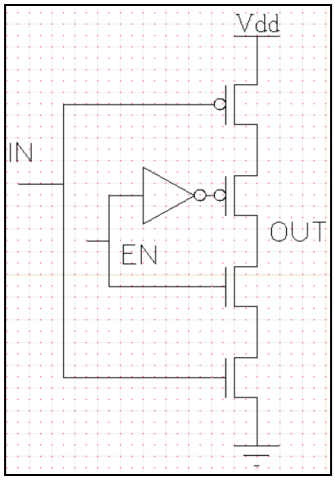
Q3. A designer proposed a tri-state inverter circuit as follows. The functionality desired is that when EN = VDD, then the circuit should behave as an inverter. (2 marks CO 1)
Desired functionality:-
When EN = VDD, IN = VDD, OUT = GND,
When EN = VDD, IN = GND, OUT = VDD
When EN = GND, OUT = floating



(i) What will be the output logic levels? Why ? [1 Marks]
(ii) Propose the corrected design. [1 Marks]
Ans:

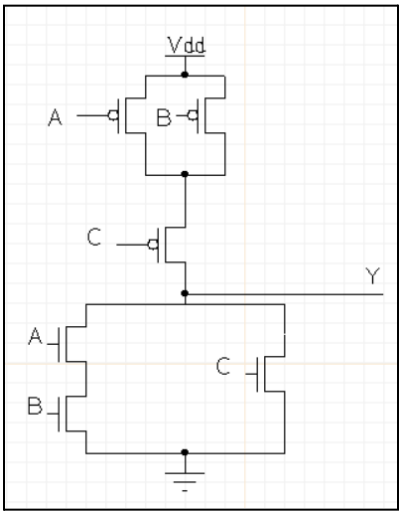
(i) Output in the proposed circuit can rise only till Vdd-V_{TN} and can fall only till Vdd+|V_{TP}| where V_{TN} and V_{TP} are threshold voltages of NMOS and PMOS transistors. This is because the NMOS is used in the pull up network and PMOS is used in the pull down network. This will cause threshold drop across and PMOS and NMOS used for enabling logic.

(ii) To fix this limited voltage swing, we can modify the circuit to ensure that Pull up network contains only PMOS and the pull down network contains NMOS. In the following circuit, this is achieved.



Q4. Answer the following questions:

The schematic of the CMOS logic is given below.



i. Identify the CMOS logic represented above and size the transistors to match the resistance of a unit inverter. [1 marks] (CO1)

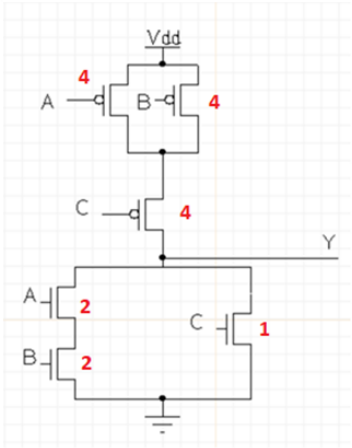
ii. Draw the stick diagram considering appropriate sharing of source and drain regions. [2 marks] (CO1)

iii. Estimate the propagation delay for rise in terms of RC. [1 marks] (CO1)

iv. Estimate the contamination delay for fall in terms of RC. [1 marks] (CO1)

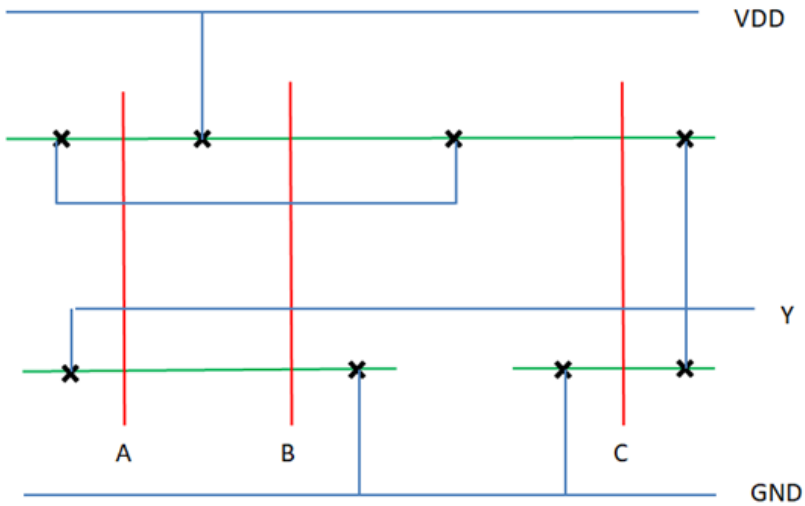
Sol.

i. CMOS Logic = $\overline{A.B + C}$ **[0.5 Marks]**



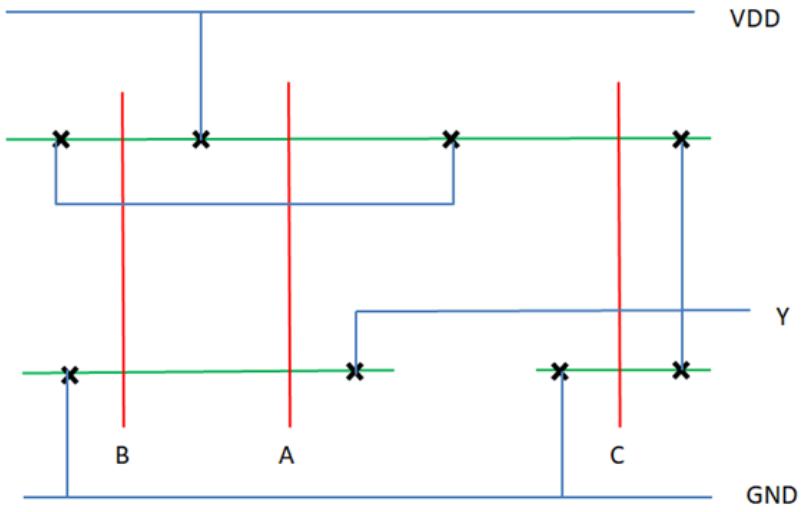
[0.5 Marks]

ii. Stick Diagram:



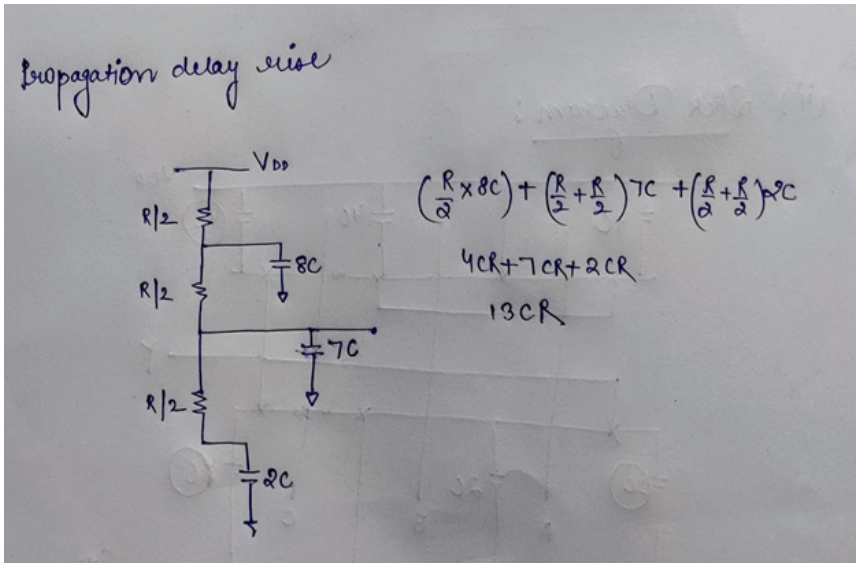
[1.5 Marks]

More Efficient by sharing interchanging the A and B, metal will be less



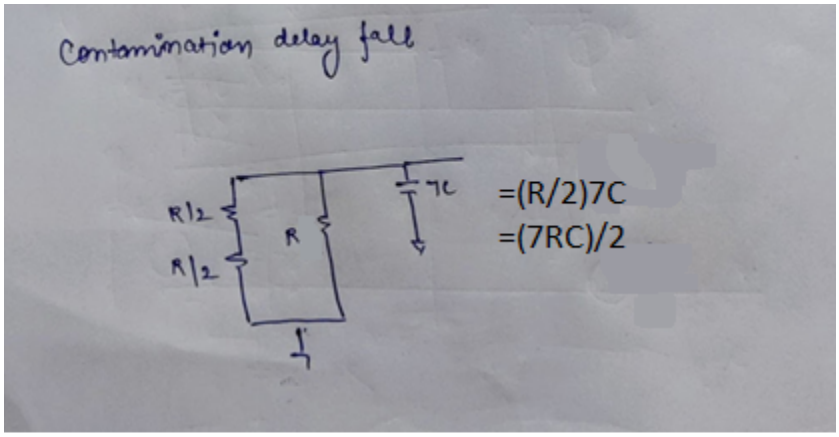
[2 Marks]

iii. Propagation Delay rise



[1 Marks]

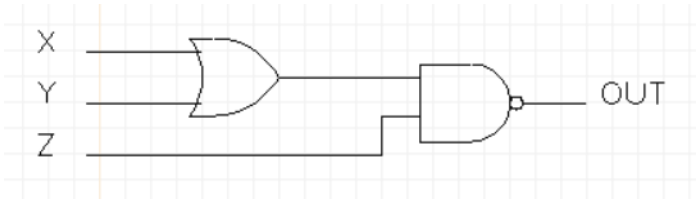
iv. Contamination Delay fall



[1 Marks]

Q5. Answer the following questions:

i. Find the logical effort for the input X, considering driving a 50 unit load (H=50). Hint: You can consider OR logic by combination of NOR and NOT gate. You have to ensure that overall logic functionality should be well preserved.



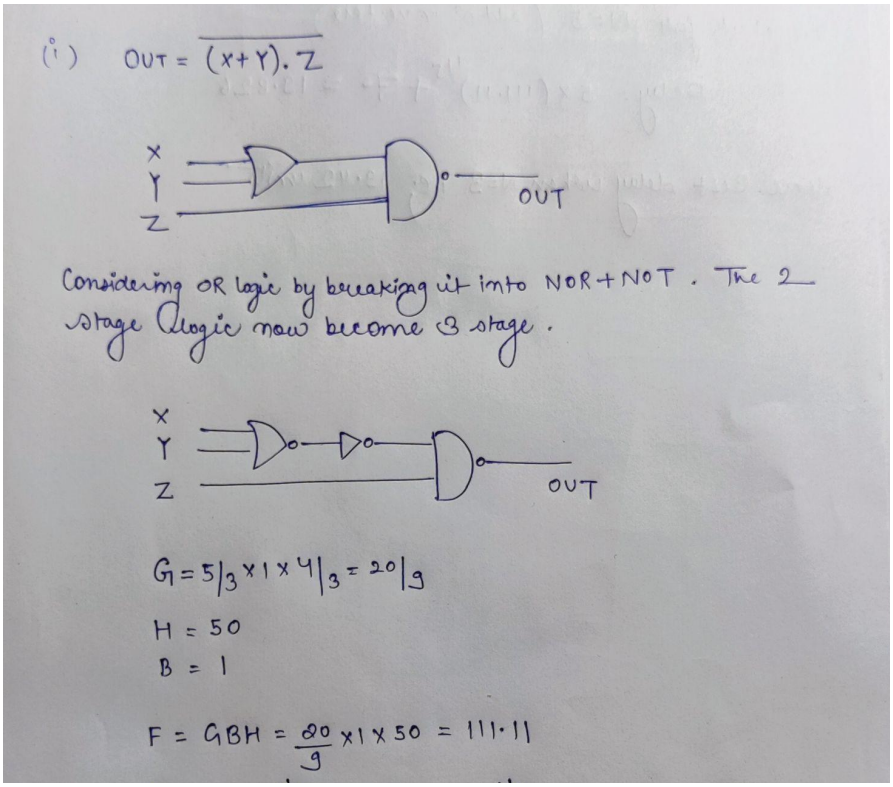
[2 marks] (CO2)

ii. Consider the Probability of each input = 0.5 and every input is independent. What will be the activity factor of the circuit? [1 marks] (CO3)

iii. Calculate the dynamic power of the circuit if the input frequency is 100MHz, output load of 50fF and supply voltage 1.08V? (ignore self-loading and short-circuit currents) [1 marks] (CO3)

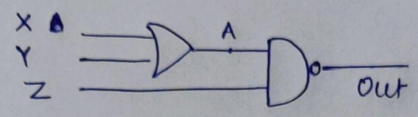
iv. How we improve dynamic power consumption by reducing the activity factor of the circuit. Explain any 2 ways. [1 marks] (CO3)

Solution 5.



[2 Marks]

(iii) $Out = \overline{(X+Y).Z}$



$P(X) = P(Y) = P(Z) = 1/2$

$P(A) = 1 - \overline{P(X)}\ \overline{P(Y)}$

$1 - 1/2 \cdot 1/2 = 3/4$

$P(out) = 1 - P(A)\,P(Z)$

$= 1 - 3/4 \cdot 1/2$

$= 5/8$

$\alpha_{out} = (1 - P(out))\,P(out)$

$= 3/8 \cdot 5/8$

$= 15/64$

(iv) Dynamic Power $= \alpha C V_{DD}^2 f$

$= \frac{15}{64} \times 50 \times 10^{-15} \times 1.08^2 \times 100 \times 10^6$

$= 1.37\ \mu W$

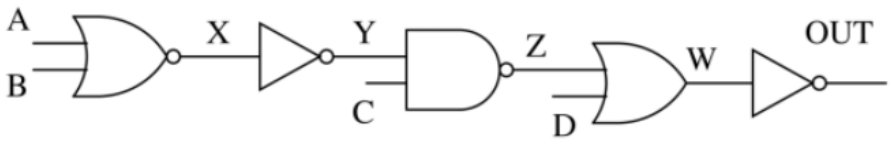
[1+1 Marks]

iv) 1. **Clock Gating**: It ANDs the clock signal with an enable to turn off the clock going into blocks which are idle in the system. Clock already has a high activity factor in an IC, so this method significantly reduces the overall dynamic power due to unwanted switching activity. Additionally, if a gate doesn't have a clock signal controlling it, we can save power by adding an enable signal, so that the gate consumes power only when in use.

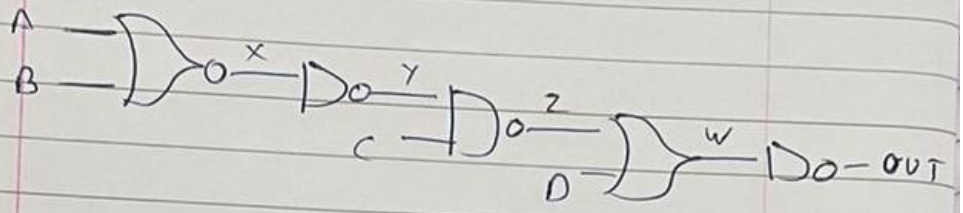
[0.5 Marks]

2. **Prevent Glitches**: Gates sometimes make spurious/erroneous transitions when inputs do not arrive simultaneously. These can lead to activity factors exceeding 1 and hence increase power dissipation. They can be avoided by proper timing of the signals during operation. Glitches may also be prevented by implementing complex gates and logic in a manner such that gating of circuit is done by late arriving signal. **[0.5 Marks]**

Q6. For the given circuit calculate the activity factor at OUT [2 Marks]. (CO 3)



Sol.



At x :- $P(1) = \frac{1}{2} \times \frac{1}{2} = \frac{1}{4}$

At y :- $P(1) = 1 - \frac{1}{4} = \frac{3}{4}$

At z :- $P(1) = 1 - P(y=1 \text{ \& } c=1)$

$= 1 - \frac{3}{4} \times \frac{1}{2}$

$= 1 - \frac{3}{8}$

$= \frac{5}{8}$

At w :- $P(1) = 1 - \left(\frac{1}{2} \times \frac{3}{8}\right)$

$= \frac{13}{16}$

At OUT :- $P(1) = 1 - \frac{13}{16} = \frac{3}{16}$

$\alpha = \frac{3}{16} \times \frac{13}{16} = \frac{39}{256}$

Q7. Complete the below table with an explanation . (Worst PVT conditions of different FOMs for CMOS Inverter). [6 marks] CO3 - CO2

Figure of Merit (FoM)	Process	Voltage	Temperature
Delay (propagation)			
Leakage Power			

Ans:

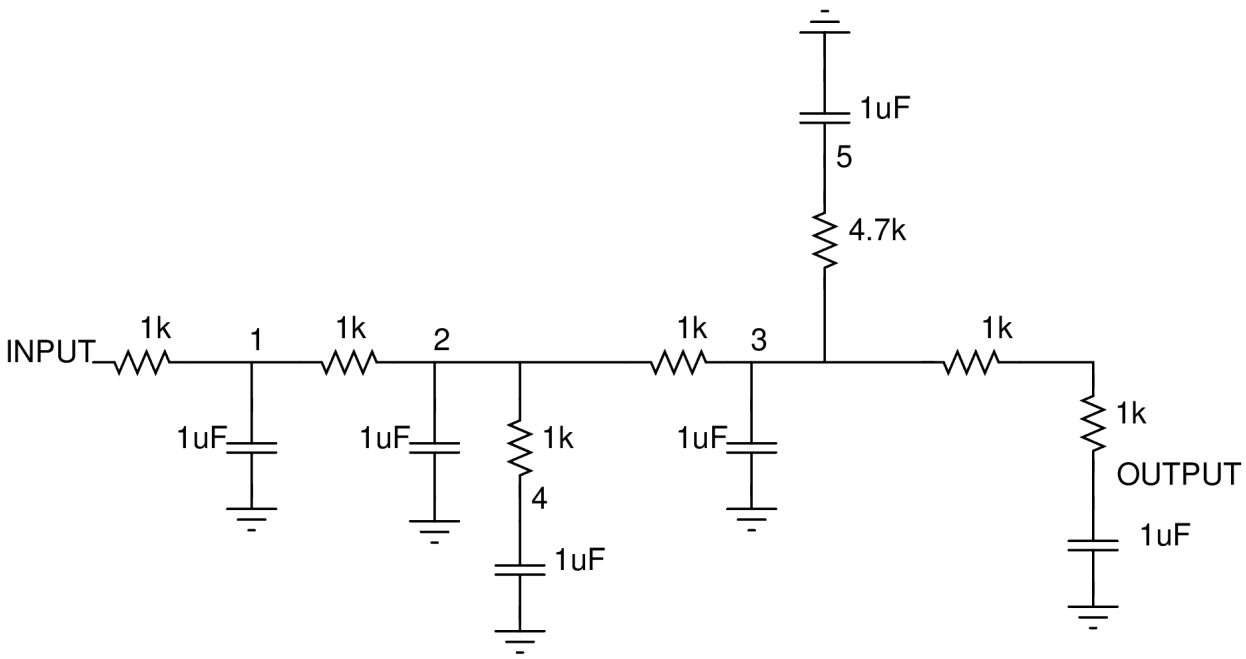
Figure of Merit (FoM)	Process *(2 marks, 1 mark for each)*	Voltage *(2 marks, 1 mark for each)*	Temperature *(2 marks, 1 mark for each)*
Delay (propagation)	SS	1.08V	125C
Leakage Power	FF	1.32V	125C

Delay (propagation) :

For worst case delay, we would want our design to function at worst cases, when both the NMOS and PMOS are slow slow. Hence, SS slot would be the process corner and delay is worst at low voltage (lesser current) hence, lowest voltage 1.08V should be chosen So, for delay design must qualify for SS 1.08V corner. At high temperature , the electrons gain very high kinetic energy , because of which they start to collide with the substrate atoms , as a result of which their speeds decrease . Hence , high temperature is the worst case temp for propagation delay.

Leakage Power :

For worse leakage, the design must function when we have the highest occurring leakage also. And leakage increases at higher VDD and hence 1.32V should be verified. Similarly, leakage power increases with reduction in Vt. Low Vt means Fast devices, hence Fast NMOS and Fast PMOS should be taken into verification. As for FF, lower Vt means more leakage. Leakage is maximum at high temperatures.



Q8. The above figure represents the lumped RC model of a particular circuit. We know beforehand that this circuit will work properly if the time taken for the output voltage to rise from 0V to Vdd/2 (for a stepped input) is less than 12 ms. Verify whether the above circuit meets this specification. (C 02) [3 marks]

Solution:

Only the resistances on the path b/w input and output are relevant.

Node 1

$Z_{D1} = 1K\Omega \times 1PF = 1ms$

Node 2

$Z_{D2} = (1K\Omega + 1K\Omega) \times 1PF = 2ms$

Node 4

$Z_{D4} = (1K\Omega + 1K\Omega) \times 1PF = 2ms$

Node 3

$Z_{D3} = (1K\Omega + 1K\Omega + 1K\Omega) \times 1PF = 3ms$

Node 5

$Z_{D5} = (1K\Omega + 1K\Omega + 1K\Omega) \times 1PF = 3ms$

Output node.

$Z_{out} = (1K\Omega + 1K\Omega + 1K\Omega + 1K\Omega + 1K\Omega) \times 1PF = 5ms$

Net elmore delay = 16 ms

On calculating,the time taken to rise to 50 percent of the peak voltage for a step response is 0.69*16ms = 11.04ms. So this module will work within the specified time constraints. [3 Marks]