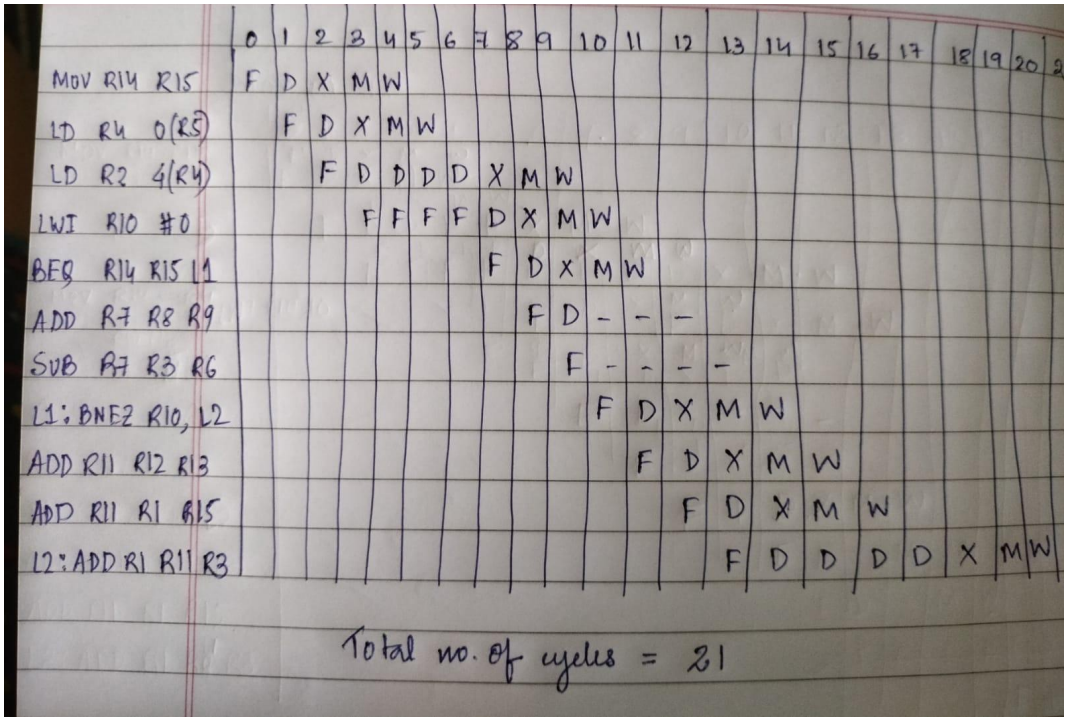
Midsem Solutions
CSE/ECE 511 Computer Architecture

Q1
Marks distribution:

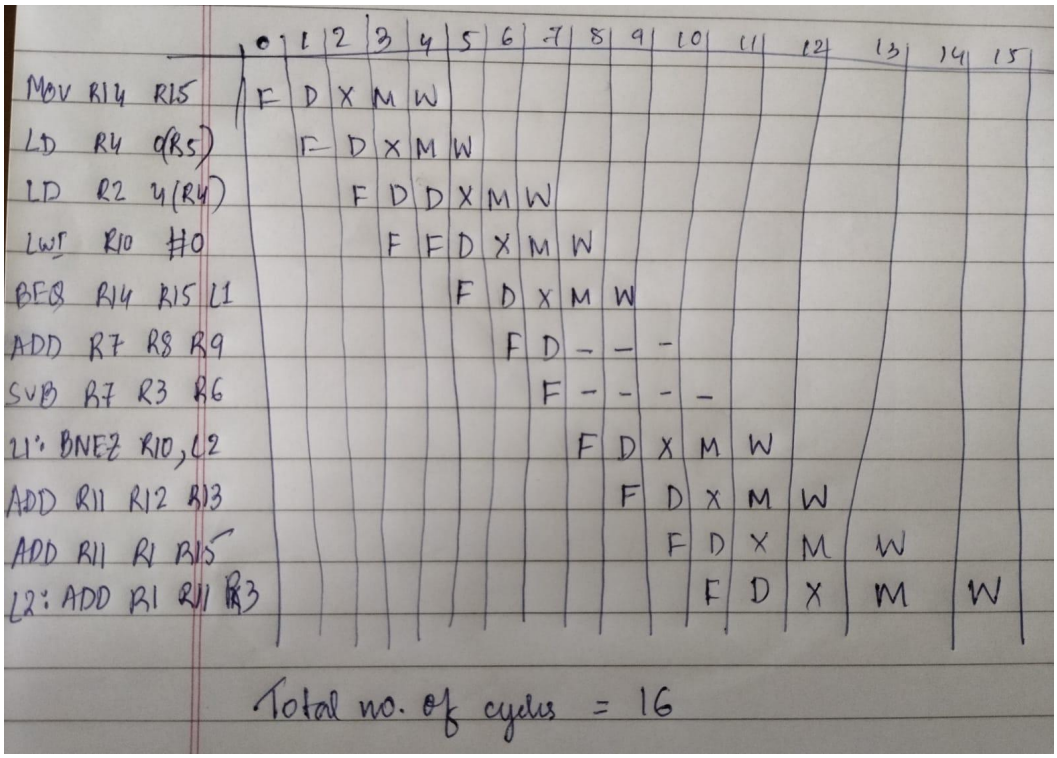
Instruction No.	Marks
1	No marks
2	0.5
3	0.5
4	0.5
5	0.5
6	1
7	1
8	1
9	1
10	1
11	No marks

0.5 Mark for cycle count

a.



b.



Q2

a. 10,000 * 32 /8 = 40,000 bytes - 2 Marks

b. 3:1 for L : S type instruction therefore 7500 instruction of L and remaining 2500 instruction of S. Therefore 7500 * 4bytes + 2500 * 2bytes = 30,000 + 5,000 = 35,000bytes. These 7500 instructions will be stored in ImemA and the rest 2500 instructions will be stored in ImemB. - 2 Marks

c. 10,000 instructions and 4 bytes for the address of each instruction therefore 40,000bytes for sending address.
40,000 * 1 (for sending address) + 40,000 * 1 (sending instruction data back) nJ = 80,000nJ. - 2 Marks

d. 40,000 nJ for sending address since for both instruction memory, address space is 32-bit. 7500*4*1 =30,000nJ for sending instruction data back for type L instructions from ImemA. 2500*2*3=15,000nJ for sending instruction data back for type S instructions from ImemB. Therefore total is :
40,000 (for sending address) + 45,000 (sending instruction data back) nJ = 85,000nJ.
- 2 Marks

e. Total bytes transferred = 80,000. Therefore, we need 80,000ms - 2 Marks

f. Total bytes transferred = 75,000. Therefore, we need 75,000ms - 2 Marks

g. In FL-ISA there are no 16-bit instructions hence no memory is required in Imem B.

ISA	Imem A	Imem B
FL-ISA	40,000 Bytes (0.5 Mark)	0 Bytes (0.5 Mark)
VL-ISA	7500 * 4 = 30,000 Bytes (0.5 Mark)	2500 * 2 = 5000 Bytes (0.5 Mark)

h. VL-ISA takes less time hence will be preferred for server-type processors whereas FL-ISA takes less energy and hence will be preferred for mobile-based processors. - 1 Mark

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Q3

Direct Mapped

Cycle time = 0.4 ns

miss rate = 6.8 %

miss penalty = 100 ns

hit time = 1 cycle

AMAT = hit time + MR x MP

= 1 x 0.4 + $\frac{6.8}{100}$ x 100 — 1.5

= 0.4 + 6.8 = **7.2 ns**

2-way set-associative

cycle time = 1.4 ns

MR = 4.9 %

AMAT = HT + MR x MP

= 1.4 + $\frac{4.9}{100}$ x 100 = 4.9 + 1.4

= **6.3 ns**

— 1.5

4-way

MR = 4.4 %

cycle time = 1.4 ns

AMAT = HT + MR x MP

= 1.4 + $\frac{4.4}{100}$ x 100 = 4.4 + 1.4

= **5.8 ns**

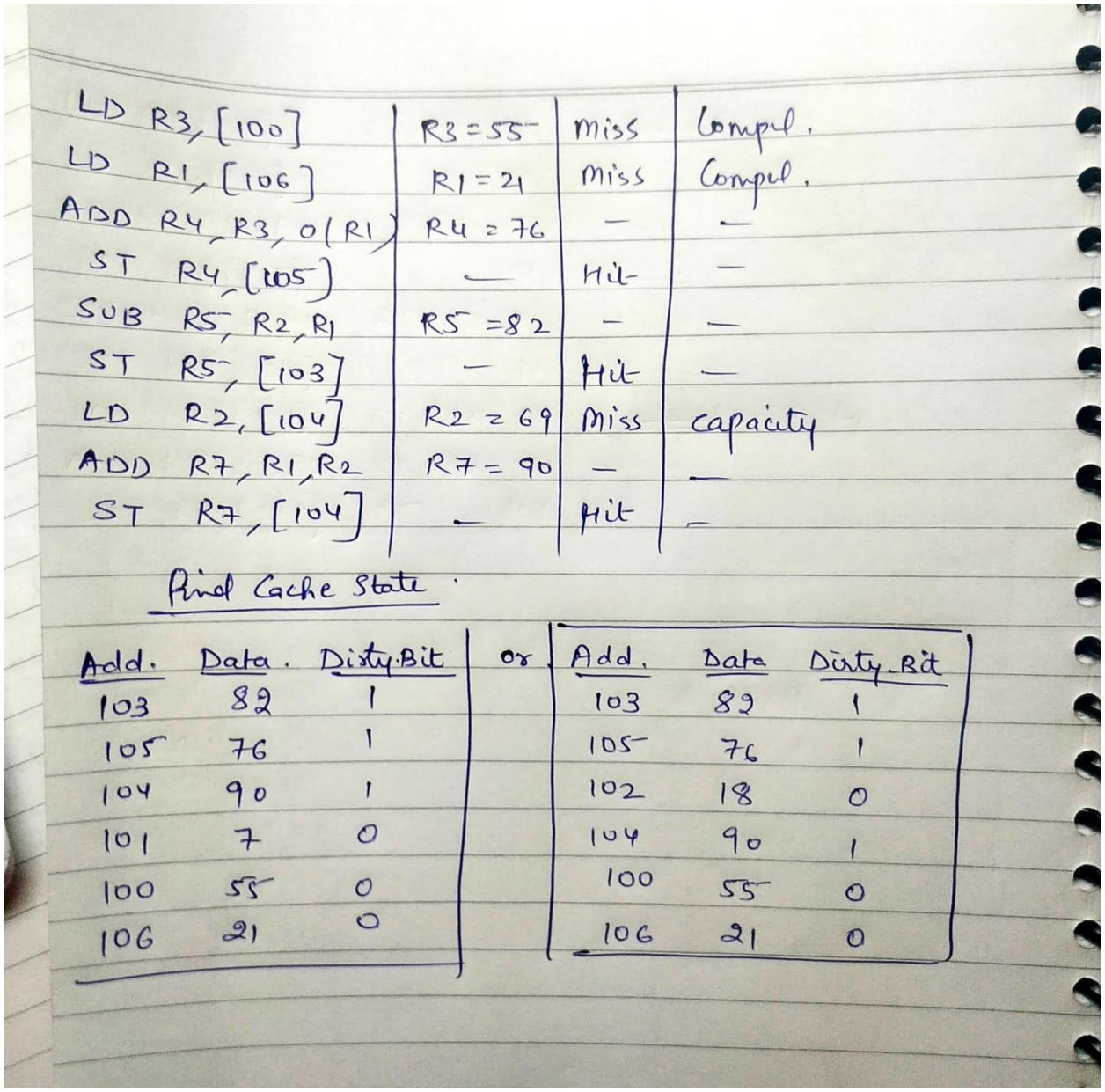
— 1.5

As associativity increases the AMAT decreases

— 0.5

Q4.

[Address 100 and add 106 data loaded in cache, 2.5marks]
[0.5 for each miss, hit, compul, or capacity => 4.5marks]
[1 mark for each dirty_bit=1 mark,=> 3 marks]
[LRU correctly used, 2 marks]
[0.5 marks for each correct register value=> 3 marks]



LD R3, [100]	R3 = 55	Miss	Compul.
LD R1, [106]	R1 = 21	Miss	Compul.
ADD R4, R3, 0(R1)	R4 = 76	—	—
ST R4, [105]	—	Hit	—
SUB R5, R2, R1	R5 = 82	—	—
ST R5, [103]	—	Hit	—
LD R2, [104]	R2 = 69	Miss	capacity
ADD R7, R1, R2	R7 = 90	—	—
ST R7, [104]	—	Hit	—

Final Cache State:

Add.	Data	Dirty Bit
103	82	1
105	76	1
104	90	1
101	7	0
100	55	0
106	21	0

or

Add.	Data	Dirty Bit
103	82	1
105	76	1
102	18	0
104	90	1
100	55	0
106	21	0