Question 1: A processor supports two different frequency settings for both core and uncore elements: 2.0GHz and 2.2GHz. According to you, which core and uncore frequencies settings might be optimal for running parallel Fibonacci and parallel sorting (one application at a time)? Optimal setting is the one that achieves maximum power savings without significant loss in performance). Brief justification. **[2 marks]**
Fibonacci: Core at 2.2 and uncore at 2.0. [+0.5 marks]
Fibonacci is a compute bound application, hence it will have optimal execution using high core frequency and low uncore frequency. [+0.5 marks]
Sorting: Core at 2.0 and uncore at 2.2. [+0.5 marks]
Sorting is a memory bound application, hence it will have optimal execution using low core frequency and high uncore frequency. [+0.5 marks]

Question 2: A dual core processor only has a private L1 cache (at each core) apart from the DRAM for storage (assume no disk access for this scenario). Assume the cost of the following actions as one cycle: a) moving a cache line from DRAM to L1 cache, b) BusRd, and c) BusRdX. There is zero cost for accessing a cache line from the L1 cache, and for all other operations whatsoever that are not specified here. What would be the cost (in cycles) for executing the statement "a++" at Core-0 for both the MSI and MESI cache coherence protocols. Assume cold caches at both the cores, and Core-1 remaining idle. Show the steps for your calculation. **[2 marks]**
MSI protocol: 3 cycles [0.25 marks]
BusRd to read in shared state (1) + load from RAM to L1 (1) + BusRdX for moving to Modify state (1) [0.75 marks]
MESI protocol: 2 cycles [0.25 marks]
BusRd to read in Exclusive state (1) + load from RAM to L1 (1) [0.75 marks]

Question-3: Name four approaches for achieving resilience in parallel programs. No justifications. **[2 marks]**
Checkpointing [0.5 marks], Forward recovery [0.5 marks], Replication [0.5 marks], and Failure prediction [0.5 marks]

Question-4: What does consistency and coherence imply while accessing two different memory locations A and B on a multicore processor? Answer briefly. No need to write the elaborate definitions or differences. **[2 marks]**
Consistency describe the set of rules about the **order** in which the **writes to two different memory locations** will be made **visible**. [+1 marks]
Coherence ensures **writes to a single memory location** will be seen in **order**. [+1 marks]

Question-5: Demonstrate boost context switching **using pseudocode**. APIs that require demonstration are **continuation**, **callcc** and **resume**. Exact syntax is not required. **[2 marks]**

```
continuation A(continuation c1) {        [0.5 marks]
  c1.resume();                           [0.5 marks]
}
main() {
continuation c2 = callcc(A);             [0.5 marks]
c2.resume();                             [0.5 marks]
}
```