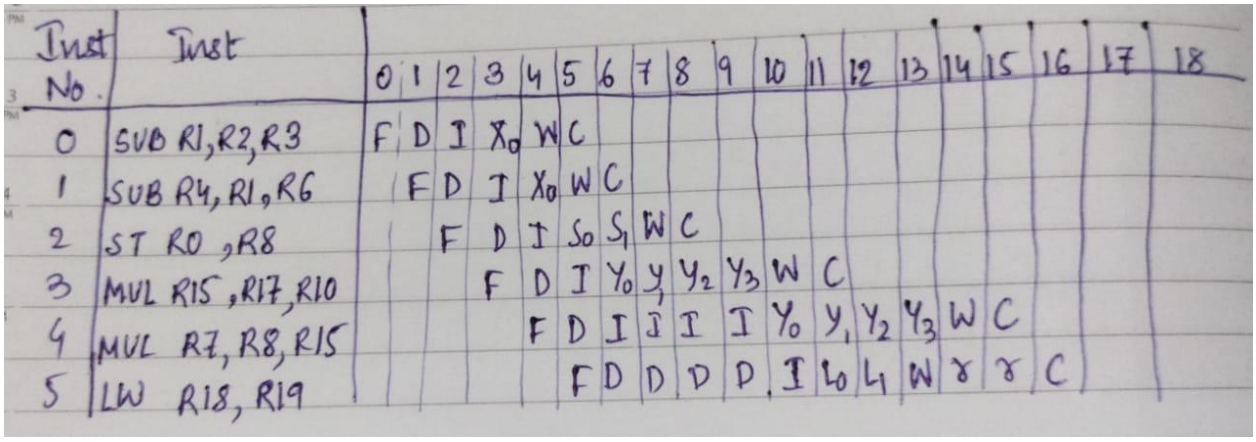
Quiz 3 solutions
CSE/ECE 511 Computer Architecture

Q1.
a)



Inst No.	Inst	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
0	SUB R1,R2,R3	F	D	I	X_0	W	C													
1	SUB R4,R1,R6		F	D	I	X_0	W	C												
2	ST R0 ,R8			F	D	I	S_0	S_1	W	C										
3	MUL R15 ,R17,R10				F	D	I	Y_0	Y_1	Y_2	Y_3	W	C							
4	MUL R7,R8,R15					F	D	I	I	I	I	Y_0	Y_1	Y_2	Y_3	W	C			
5	LW R18,R19						F	D	D	D	D	I	L_0	L_1	W	γ	γ	C		

b) State **of scoreboard when Instr. 3 is in Issue stage:**
R4 is pending in functional unit 'X' and is marked as having '0' more cycles until writeback.
The rest of the registers are not pending.

State of scoreboard when instr. 5 is in issue stage:
R15 is pending in functional unit 'Y' and is marked as having '0' more cycles until writeback.
R7 is pending in functional unit 'Y' and is marked as having '4' more cycles until writeback.
The rest of the registers are not pending.

Q2.

Note: There might be more than one correct answer other than the solution given below.

VLIW Instruction	MIPS Instruction	MIPS Instruction
1	01	02
2	03	05
3	04	06
4	07	08
5	09	10