ECE-314/514 - DVD End Semester Solution Rubric

Que 1. Given below are some design failures/challenges, given the design and the causes of failure, identify the cause of failure [1 Mark] and give suggestions to prevent/rectify them [1 Mark].
(Solve any 4). Solve all 5 for BONUS 2 Marks. [8 Marks+2 BONUS]

a. When a design was fabricated and tested, it was observed to fail at 900MHz, though the sign-off was done at 1GHz? This happened often for Slow lots, while Typical and Fast lots were functional at 1GHz also. What failure does it point to? [2 Marks]

Ans: Setup violation. It is deduced from the statement that yield is recovered at low frequencies. Also, it was failing for slow lots, while functioning with typical and fast was okay [1 Mark]. For slow lots delays have increased and design is not able to meet timings, leading to setup violation. [1 Mark]

b. A design was found to do incorrect computations when operated at high voltage. At lower voltages, such failures disappeared. Changing the frequency of operation did not help. What failure does this point to? [2 Marks]

Ans: Hold violation. At high voltages circuit operates faster and contamination delays reduce, therefore violation is coming [1 Mark]. Changing the frequency did not help because hold violations are independent of frequency of operation or time period [1 Mark].

c. A very high-speed processor was designed using Dynamic gates. It operates perfectly initially. However, after some time of operation, some computations start to be erroneous. This happens more in summers. Switching OFF and ON quickly doesn't help. But waiting for a few minutes lets it operate normally. Also, when the load on the processor is less, this problem doesn't appear. What could be the reason? [2 Marks]

Ans: Leakage, processor is high speed so more heating, resulting in higher leakage. Due to increased leakage, precharge is not able to work properly, resulting in erroneous results after the chip heats up [1 Mark]. Quickly OFF-ON did not help because we did not give time for the chip to cool down, whereas operating it after some time gives the processor sufficient time to cool down. Also, when the load is less the processor is operating at low frequency so less heating or no heating, consequently less leakage [1 Mark].

d. Sometimes, at power-ON, a processor consumes a lot of power. When RESET pin is asserted, power consumption reduces to normal. This design used a new architecture of sequential elements. What could be the problem? [2 Marks]

Ans: Meta-stability. Processor is consuming a lot of power which reduces to normal, when RESET is asserted, which is supported by the observation that a different architecture for sequential elements was used.[1 Mark]. To reduce meta-stability we need to reduce τ, so we need to size the circuit in such a way that setup + hold window is reduced [1 Mark]

e. Jaduguda is the oldest Uranium mine in the country. When you visit the villages nearby, you will notice that many people have physical abnormalities. Incidentally, your phone also behaves very quirky there. What could be the reason? [2 Marks]

Ans: Soft errors. Presence of abnormalities in villagers, indicates higher level of ambient radiations and high energy particles. [2 Mark]

Optional: Due to more radiations and energy of irradiating particles, fault behavior, soft errors can occur in the circuit. We can use radiation hardening and error correction codes to minimize soft errors.

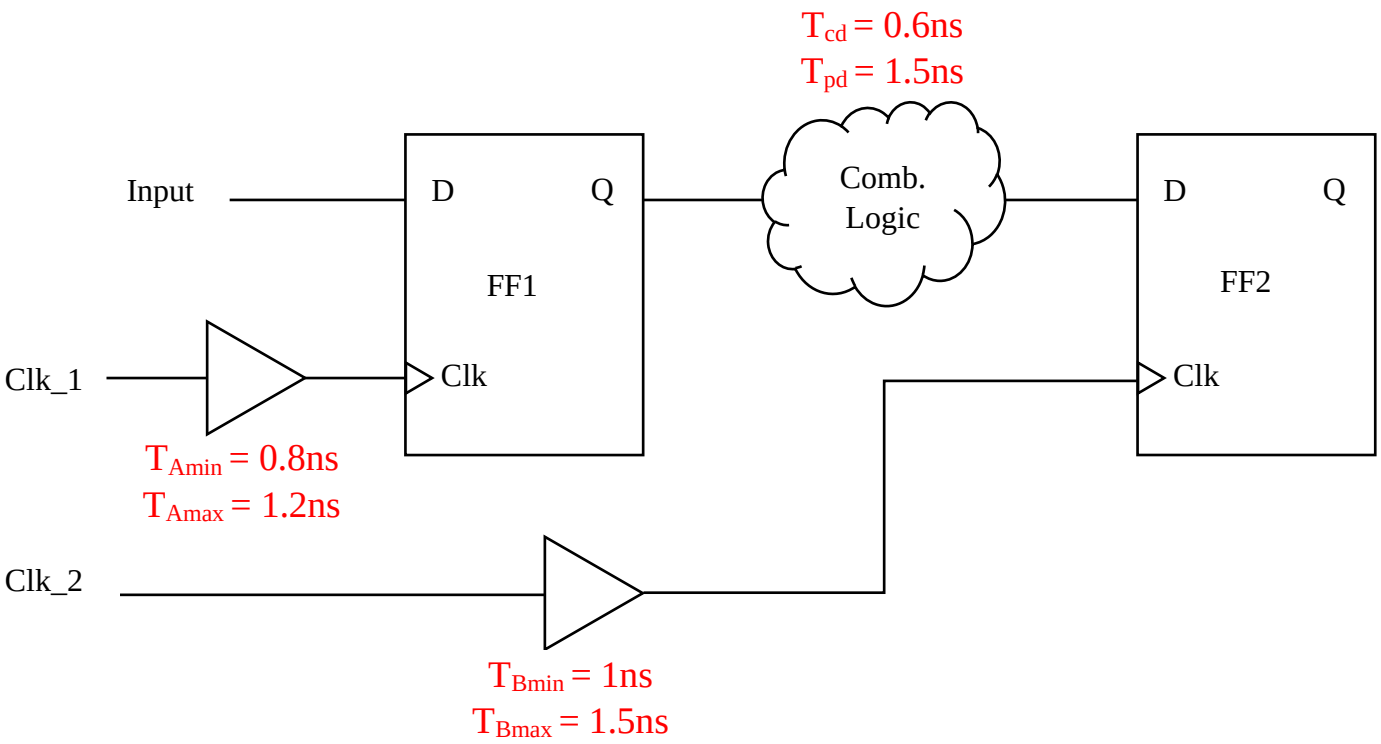
Que 2. For the given circuit, assume both the clocks have same time periods. Show all the steps, else no marks would be awarded. Given, for both the FFs, Tcq_{min} = 0.4ns, Tcq_{max} = 1ns, T_{setup} = 0.5ns, T_{hold} = 0.5ns. Calculate the following: [7 Marks]

a. Calculate minimum time period for operation. [1 Mark]

b. If the both the clocks have a jitter of 100ps, find the new minimum time period. [2 Marks]

c. If Clk_2 has positive skew of 200ps (additional to the skews given from buffers), what is the new time period. [2 Marks]

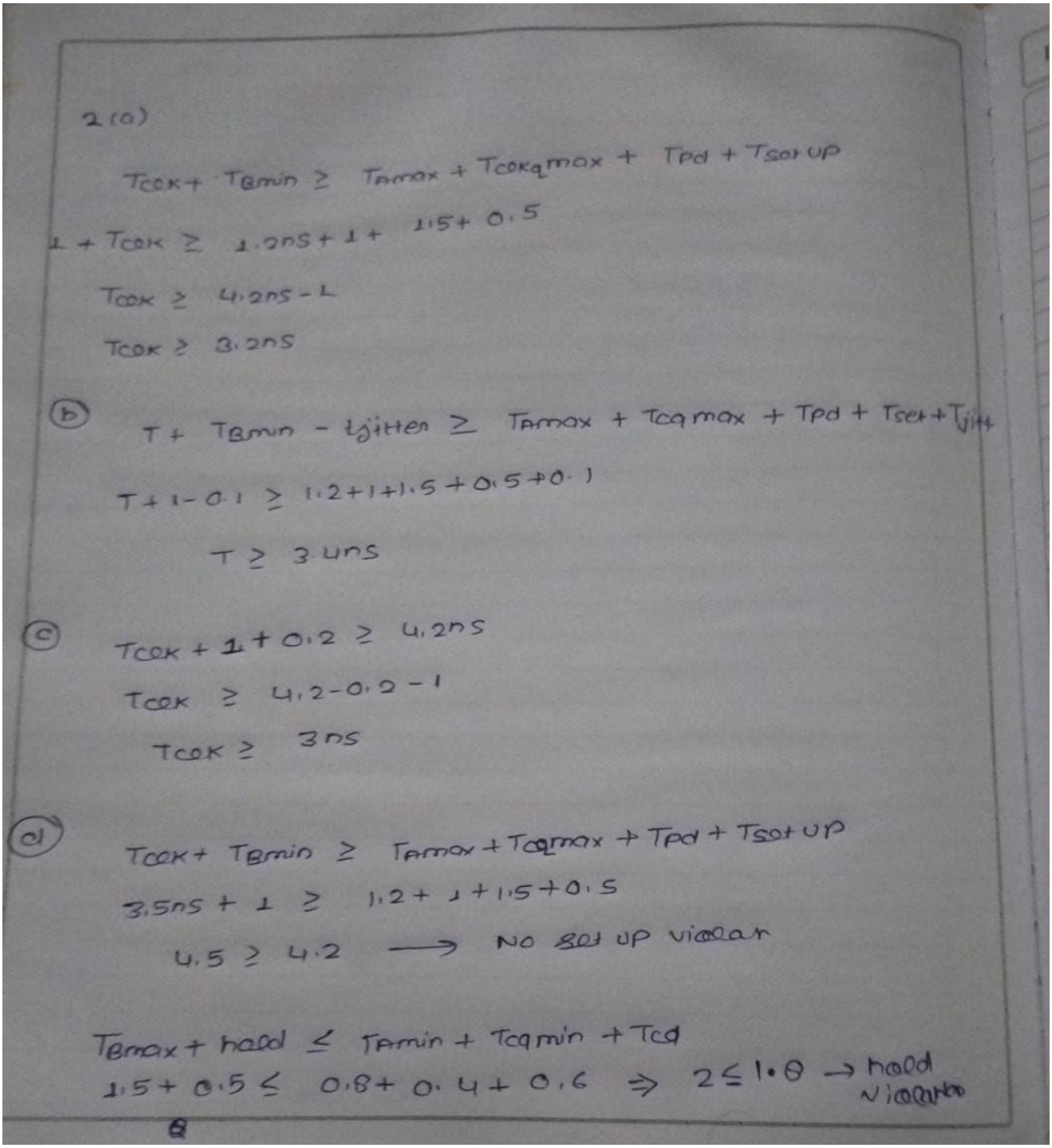
d. Check for any setup and hold violations with relevant equations, if the clock period is 3.5ns (without jitter), In case of violations state any 2 methods of removing the setup violation. [2 Marks]



Ans:

Rubric: In Q2(a) - 1 mark if formula and final answer both are correct .0.5marks if only formula is correct.

In Q2(b), Q2(c), Q2(d) - 2 marks if formula and final answer both are correct . 1 mark if only formula is correct.



Que 3. Solve the following: **[10 Marks+1 BONUS]**

a) Should we use XOR gates (designed using Transmission gates) in standard cell design? Explain briefly. [1 Mark]

Ans: No, because this implementation has diffusion input, because this can lead to different input capacitance, depending on the status of inputs and loading seen at the output of this gate. Therefore, it is difficult to size the drivers, and doing timing closure.
Tx gates-based implementation can, however be used in full custom designs.

Rubric: If only NO written 0.5 marks, If the reason is written, then total 1 mark.
If Yes written 0 marks

b) What is time borrowing? What is the timing constraint in adjacent stages, so that latches can borrow time? [2 Marks]

Ans: Time borrowing is a method of gaining some extra time from the next cycle. It is used in sequencing circuits and helps satisfying the timing constraints. [1 Marks] for definition

In (positive level) latches, we have "clock positive duration - setup" for sampling data. Therefore, previous stages, with long combinational paths have a larger window to satisfy the constraints of hold and setup.

Timing Constraint Explanation: The constraint in timing for time borrowing in latches is that the next logic will have lesser time as some of it's time has been borrowed by the previous stage. Hence, the next stage combinational logic block must have lesser delay. [0.5 marks]

2-Phase Latches	Pulsed Latches
$t_{borrow} \le \frac{T_c}{2} - \left(t_{setup} + t_{nonoverlap}\right)$	$t_{borrow} \le t_{pw} - t_{setup}$

Rubric:

0.5 marks for equation:

If only the formula from slides is written and is not explained correctly 0.5 marks deducted.

BONUS QUE:

How can we enable time borrowing in FF based sequencing? [**BONUS** 1 Mark]

Ans: We can enable time borrowing in FF based sequencing with the help of useful skew. Like if the capture FF (later FF in sequence) clock (termed as capture clock) is delayed, then we will get more time for the combinational logic in between launch and capture FF, hence time borrowing in FF.

c) Compare among FF, Pulse latch and regular latch, which one is best among others and explain the reason (one point each) on below figure of merits: [4 Marks]

1) Performance
2) Power
3) Area
4) Robustness

[Hint: If Latch is the best among all three in some PPA, then explain why latch is better from the other two, do this for all 4 merits listed above]

Ans:

	FF	Latch	Pulsed Latch
Performance	Good, less skew because same phase of clk considered	Better, easy time borrowing, managing two phases of clocks can lead to higher overheads.	Best, some level of inbuilt time borrowing. Single phase of clock to be managed. Also, least sequencing overhead.
Power	Poor, because of clock is tapped at many transistors, increasing cap at clock input	Better	Better
Area	Poor, larger cell size (as it is made of 2 latches).	Better, at system two-phase of clock tree, needs to be routed.	Best, single phase of clock is being used
Robustness	Best, Safe design. Only one edge of the clock is used. Noise is also lesser.	Average, because two phases of clock will have larger variations in insertion delay and skew.	Poor, designing the pulse duration is a challenge, specifically in presence of variations.

Rubric:
1 mark for each figure of merit explanation. In that 1 mark, 0.5 marks is for comparison and 0.5 marks for explanation of why does the comparison holds.'

d) Match each element of column A, with one of column B and C each. [3 Marks]

Ans:

Design Style (A)	Figure of Merit (B)	Applications (C)
Dynamic	High Perform	Processor
Static	Robust	Medical Applications
PTL	High Density	Column decoder

Rubric: 0.5 marks for each correct matching.