VLSI Design Flow

Mid Semester Exam (13th March 2022)

Time allowed: 1 hour *Maximum Marks: 30*

Note:

I. ***All questions are compulsory.***
II. ***Marks are indicated in bold at the end of each question.***
III. ***Be crisp and precise in your answer so that you can complete the answers in 1 hour.***
IV. ***Use the marks allotted to each question as an indicator of how elaborate you need to answer.***
V. ***Cheating or use of unfair means will be dealt with as per institute policy.***

1. For a given process, the yield is modeled by the following equation:

$$Yield = \left(1 + \frac{Ad}{\alpha}\right)^{-\alpha} \times 100\%$$

where A is the die area, d is the defect density, and α is the clustering parameter. The wafer size is 300 mm in diameter, and the die size is 25 mm^2. Assume that the cost of fabricating a wafer is $200, and there is no wastage of material in creating dies out of the wafer. Assume defect density is 0.5 defect/cm^2 and the clustering parameter is 0.5.

(a) Estimate the yield and the cost per die.

(b) Due to yield learning, defect density decreases to 0.1 defect/cm^2. Estimate the new yield and the cost per die. Explain why does the yield change from that computed in (a).

(c) Assume that defect density remains as 0.1 defect/cm2, but the die area is increased to 100 mm^2. Compute the new yield and the cost per die? Explain why does the yield change from that computed in (b). **[4+4+4 Marks]**

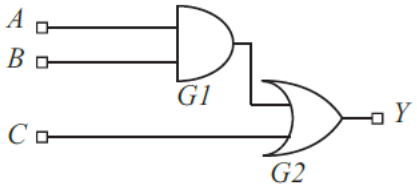
2.

a. You need to define a virtual clock with name *VCLK* and clock frequency 1 GHz. Then you need to define input delay of 100 ps at the input port named *IN* with respect to the virtual clock *VCLK*. Assume that you need to use nanosecond as the unit of time in the SDC file. Write a set of SDC commands to define these constraints.

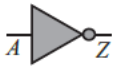
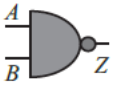
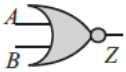
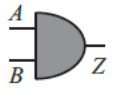
b. You are writing an SDC file for the functional mode. In the functional mode, the input port *TM* should be 0 and the input port *NORMAL* should be 1. Write a set of SDC commands to define these constraints.

c. Define multicycle path between flip-flop instances FF1 and FF2 (with clock pin name CP) that makes setup check on the 8th clock edge (instead of default 1st clock edge) and hold check on 2nd clock edge (instead of default 0th clock edge). Write a set of SDC commands to define these constraints. **[1+1+4 Marks]**

3. Consider the generic-gate circuit shown in Fig. (a). A technology mapper needs to map this generic circuit using library cells shown in Fig. (b). Show the schematic diagram of the mapped circuit (circuit that contains instances of library cells only) in each of the following cases and compute the circuit area, maximum combinational path delay, and power dissipation in each of the mapped circuit.



(a)

Cell Name	Symbol	Function	Area	Delay	Power
INV1		*Z=A'*	1	4	5
NAND8		*Z=(A.B)'*	8	4	40
NOR1		*Z=(A+B)'*	3	12	10
AND1		*Z=A.B*	4	16	50

(b)

(a) Mapper uses NAND gate(s) and inverter(s). And no other gate.

(b) Mapper uses only NAND gate(s), NOR gate(s) and inverter(s). And no other gate.

(c) Mapper uses only AND gate(s), NOR gate(s) and inverter(s). And no other gate.

(d) Which of the above cases has (i) minimum area (ii) minimum path delay for the worst case, and (iii) minimum power [Just mention a, b, or c for each part of this question].

[3+3+3+3 Marks]