DVD QUIZ 9 Rubric

Q1. Suppose you have designed a chip and after fabrication it fails to meet either setup time requirement or hold time requirement. Which failure is more crucial and why. Give reasons?

[0.5 +1.5]

Soln:

Hold time requirement is more crucial to meet.

After fabrication we cannot add and reduce delay in the data or clock paths to adjust setup or hold requirement. So if there is hold failure, there is no remedy and the chip has to be rejected as hold requirement is not dependent on clock frequency. However, we can reduce the clock frequency to meet the setup requirments and we will still be able to sell the chip rated at a lower frequency rating.

Q2. Why is Adaptive sequencing used in circuit design? Give a scenario to show how can adaptive sequencing reduce power consumption.

[1 +1.5]

Soln:

Designers include timing margins for various factors like voltage, temp, process and data dependency which makes the overall margin very pessimistic. This can leave a lot of margin and prevent the circuit from running at optimal power and performance for the given condition. So, an Adaptive sequencing circuit is used to recover the extra margins.

Let us say, at 1.2 volts the circuit is rated to operate at 800Mhz at worst condition. But in present condition at 1.2v the circuit can operate at 900Mhz. So we may lower the voltage to a lesser value say 1.1 which will still be able to operate the circuit at 800Mhz and we can save some power.

Q3. You are given a pipeline stage as shown in fig 1. The clock frequency is 20ns and the setup and hold time of all the flops are 3ns and 2ns respectively. The combinational circuit has propagation delay of 10ns and contamination delay of 6ns.

(i) Does the circuit if fig 1 meet the setup and hold requirements?

[1]

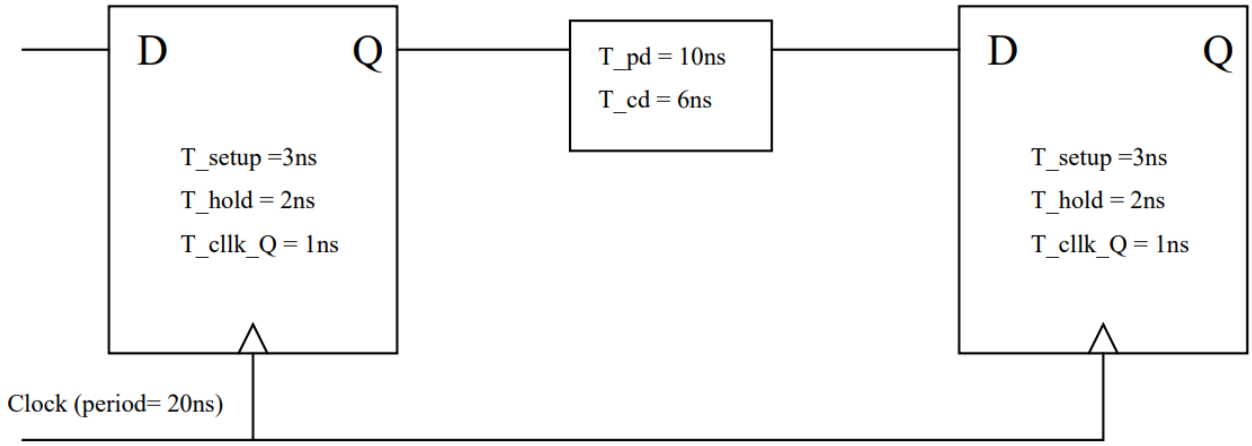


Fig 1

(ii) Now you want to break the pipeline stage into two stages so that you can double the clock frequency(clock period =10ns) , but at best you can break the combinational block into two blocks of propagation delays 7ns and 3ns and contamination delays of 3ns and 2 ns respectively as shown in the fig 2. Does this circuit meet the timing constraints? Show the violations (if any).

[1.5]

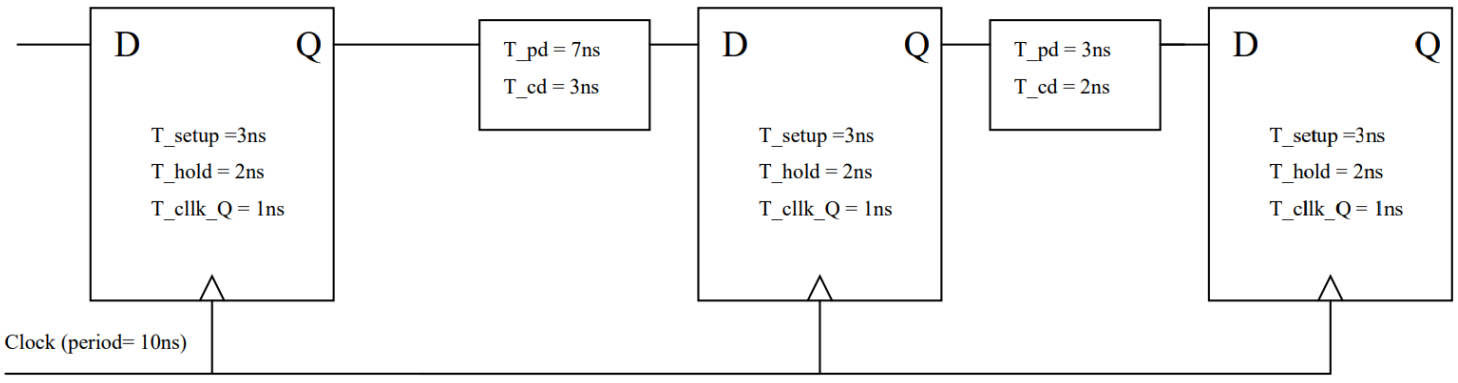


Fig 2

Fig 2

(iii) How can you remove the violations keeping the clock period 10ns only. (Hint : Use time borrowing)

[3]

Soln :

(i)

For setup

Arrival time @ D pin of 2nd flop = 1 +10 =11 ns

Required time = 20 - 3 = 17ns

As, Arrival time < Required time, setup is met

For hold

Arrival time @ D pin of 2nd flop = 1 + 6 =7 ns

Required time = 2

As, Arrival time > Required time , hold is met

(ii)

For path 1

For setup

Arrival time @ D pin of 2nd flop = 1 +7 =8 ns

Required time = 10 - 3 = 7ns

As, Arrival time > Required time setup is **not met**

For hold

Arrival time @ D pin of 2nd flop = 1 +3 =4 ns

Required time = 2

As, Arrival time > Required time , hold is met

For path 2

For setup

Arrival time @ D pin of 3rd flop = 1 +3 =4 ns

Required time = 10 - 3 = 7ns

As, Arrival time < Required time setup is met

For hold

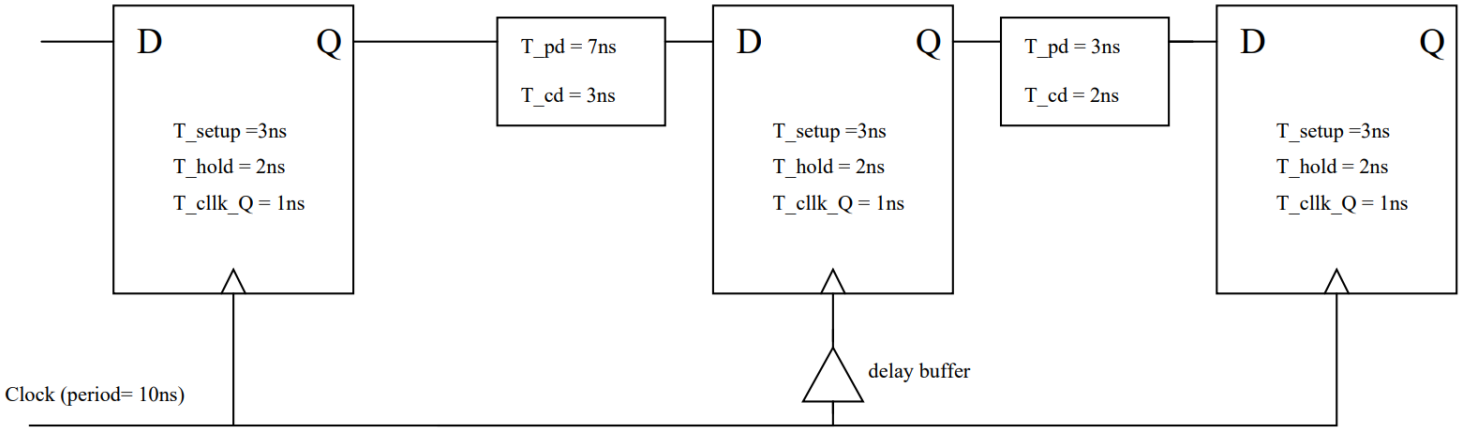
Arrival time @ D pin of 3rd flop = 1 +2 =3 ns

Required time = 2

As, Arrival time > Required time , hold is met

(iii)

We will have to add delay buffer in the clock path of 2nd flop , so that the available time period for the path 1 is increased and setup requirements are met. However in doing so we are essentially reducing the available time for path 2. We need to make sure that the delay introduced should be in a range which meets the setup requirement for path 2 as well as met hold requirement for both the parts.



For path 1

Let delay of buffer is T_buff

For setup

Arrival time @ D pin of 2nd flop = 1 +7 =8 ns

Required time = 10 + T_buff - 3

To meet setup, Arrival time < Required time

8 < 10+ T_Buff - 3

T_Buff > 1ns……(a)

For hold

Arrival time @ D pin of 2nd flop = 1 +3 =4 ns

Required time = 2 +Tbuff

To meet hold , Arrival time > Required time

4 > 2+ T_buff

T_Buff < 2ns ……(b)

For path 2

For setup

Arrival time @ D pin of 3rd flop = Tbuff +1 +3

Required time = 10 - 3 =7ns

To meet setup, Arrival time < Required time

Tbuff +1+3 < 7

T_Buff < 3 ns……..(c)

For hold

Arrival time @ D pin of 3rd flop = Tbuff +1 +2

Required time = 2 ns

To meet hold , Arrival time > Required time

Tbuff +1 +2 > 2

T_Buff > -1 ns……..(d)

From inequalities a,b,c and d we get the range of T_buff to be **1ns to 2ns** for meeting the constraints.