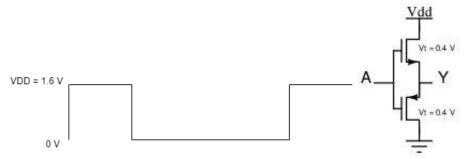
Instructions

- 1. This is a take-home quiz, with no compulsion to join the meeting, but please ask your doubts in the meeting itself.
- 2. The quiz duration is 20 mins and 10 mins extra given to upload your scanned PDFs (high quality) on the google classroom. Upload answer PDF on classroom
- 3. The quiz starts at **8:00 PM** sharp and ends at 8:20 PM. 10 minutes are reserved for scanning and uploading the quiz to Google Classroom, any submission after **8:30 PM** will attract a penalty
- 4. Meeting link for doubts: https://meet.google.com/gyd-cecr-tez

Q1. Draw the output waveform for the given input waveform for the given circuit and support your answer conceptually.



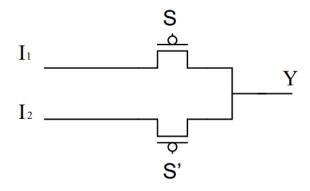
[2 Marks]

Q2. Calculate the logical effort of input F (average) for the following skewed gates. For simplicity, assume that any change in width will be done by a factor of 3, for making low or high skewed gates. Consider F as the inner input for making circuits of the below function.

High Skewed :
$$Y = \overline{(A + B) \cdot (C + D) \cdot F}$$
 [3 Marks]

Q3. In a 3 input NAND Gate the leakage power consumption drastically reduces on some input combinations (A=0, B=0, C=0). Explain the phenomenon with the help of a schematic diagram. [2 Marks]

Q4. What function/ functionality does the circuit represent? What is the problem in the implementation below? How would you correct it? Draw the modified circuit diagram [0.5 + 0.5 + 1 marks]



Q5. What is the challenge with transmission gate networks? How can we resolve it? [0.5 + 0.5 marks]