CSE/ECE 511 EndSem Solution

Q1

```
RAM AL = 200
With L1 AL = 10 (hit)
With L1 AL = 210 (Miss)
Let miss rate be m
AMAT = hitrate*hitlatency + missrate*misslatency
= (1-m)*10 + m*(210)

AMAT <= 200 (for cache to be useful)
m <= 19/20
```

Q2

The number of sets in the cache = $(16 * 2^10) / (2^32) = 256$ Since a word size is 4 bytes, int is word-sized and the size of a cache block is 32 bytes, the number of ints that would fit in a cache block is 8.

In the first loop:

Every miss followed by 3 successive hits and then this will go till i =1022.

```
i = 0 ⇒access a[0] - compulsory miss

I = 2 ⇒ access a[2] - hit

i = 4 ⇒ access a[4] - hit

i = 6 ⇒ access a[6] - hit

i = 8 ⇒ access a[8] - Compulsory miss
......
```

Therefore total miss in the first loop = 128And hits = 384

In Second Loop:

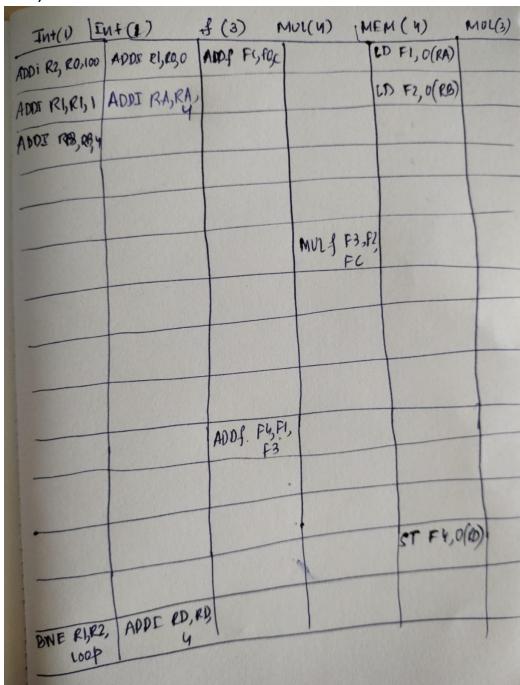
Access to a[0] will result in a hit because it is still in cache.

Access to a[1024] will result in a compulsory miss and will map to one of the cache lines of set 128 access to a[1024*2] will result in a compulsory miss and will map to one of the cache lines of set 0 and this will carry on.

Therefore the total number of misses in the second loop will be 1024 - 1 and hit = 1

Q3.

2 11	Provincent	Prediction	Achiel	Cont(c)	New State	
		N	N	6	00	for 5 loop iteration
BEGZ	00	N	T	7	01	BEQZ acurary
BNEZ	00	N	1	1	00	= 5/5 = 100%
BEQZ	01	N	N	C		BNES accuracy
BNEZ	00	N	T	I	01	
BEBZ	01	N	N	6	00	= 1/5 = 20%
		N	T	I	01	The last the last
BNEZ	00		N	C	00	
BEQ7	01	N	T	I	01	
BNEE	00	N				
BERZ	01	N	N	C	00	
BNE2	00	N	N	C	00	



0.6 for MULf; ADDf F4,F1,F3; ST; ADDI RD,RD,4; BNE R1, R2,loop 0.25 marks for rest instruction

Int (1)	Tut(D)	Add + (B)	Mul-f (4)	Memf(4)	Mil 3
ADDI 82, RD, 100		ADDIS PL, PO, C		1D F1, 0 (RA)	
	ADDE RI, RI, 2			LD F2, O(RB)	
			MVL. f F3, F2, FC		
				LD F2, 4(RB)	
	ADDI RB, RB, 8				
		Appg Fu, F1, F3			
			MULF F3, F2, FC	ED F1,4 (RA)	
	ADDI RA, RA, 8			ST F4,0(RD)	
ADDI RD, RD, Y					
		ADD F FY, FI, F3			
20 00 0	0.15			ST F4, 4(R)	
ADDT RD, RD, 8	BNF R1, K2, 100				
				J 4.	

Incremented by 8=0.25

0.25 for each

		0 1	3 3	+	5	6													1 28 2
1	ADDRI, RO,Ro	F D	I %	ω	C		7	8 "	1			6.3							Lanue
2	MUL 8 R 2 R4	F	DΙ	4,	4,	٧,	43	W (ا ا			6.3					Je	المعرا	bit deter
3	ADDI F3, R3, -3		۴D	Ĺ		-	I Y	(,	ωĊ			1							3000
4	ADD LT, R8, R9		F	D	I	X 6	ω -	((I		1							
5	B4E R3, R4, A			F	D	i	=	۲ >	6 W	7	C	(رمم	och	boonc	h labo	ه ا	vly.	yter
6	MUL RA, RIO, RII				F	Δ	i	4	<u> </u> 40	41	/		_				χσ	ريلي	0
7	ADD R5, R14, R6					F	D	i			/	0.5	_>	no 3	be	سی	e v	101'h'	A Jog
8	MUL R3, R1, R2						F	D (Z	1/0	/	0.5						. 14	
9	BEOZ R, A						1	FC	ì	I	1	0.2							
10	ADDI RS, RS, I							4	F D	i		0.5	5						
Ц	MUL RS, RII,R	6							F	D	/	0.							
[2 F	7: MUL, R8, R3, R	_4								F	D	13 14 15 1 6 41		NC	1				
13											F	DIX	w ~						

By register renaming, we were able to remove WAW hazard between instr. 2 and instr.4, and execute instr. 4 early. Similarly, we were able to remove WAR hazard between instr.6 and instr. 7.

	0	17	- 2	3 4	15	-	6	7.	8 .	9	10.	11	12	3	4	15	6 1	7 1	8.1	9 5	0	21	22	,23	
ADDRY, RZR3	F	D	I	R	X	W			-				1				1	1							
LD. f F1, O(R1)							X2	X3	W																
MULIF F2. F3, F4		1.	F	D	I	I	I	I	I	R	X	XZ	X3	Xy	W										
LD. f F1, 0(R2)				F	D	I	R	Xı	X2	X3	W			-											
SUBJ FY, FZ, FI					F	D	I	I	J	I	I	R	XI	X2	X	3 W							1		
ST. f F4, 0(R2)						F	D	I	I	I	Ī	I	I	I	Ī	I	R	X	X	Xz	h	1			
DD1 R2, R2, 3	1									R							-		1	1	1	1	1	1	
1B1 R4, R1, Y	1		-					F	D	I	R	X	n	1	1					1					

Or

6	Security of the second
ADD RY, RZ, R3	FDIRW
LID.B F1, 0(R1)	
MULG FO F3 F1	RAW.
10.6 F1, 0(R2) -	
SUB. 6 14: 12, A -	
ST. 6 F4: 0(R2) -	TO A STATE OF THE PARTY OF THE
ADDI R?, R2,3 -	
SU131 R4, R1, 4	

