CSE 112:
Computer Organization
Duration : 60 Minutes
Date: April 16, 2023

Mid Semester Exam

IIIT-Delhi, Winter 2023
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Guidelines

If you found any ambiguity in any of the questions or there appears to be a lack of information, then write an assumption on the answer sheet to explain your side interpretation of the problem and solve accordingly.

Problem I: Number Representation **2 + 4 + 4 = 10 Points**

Answer the following problems.

a) What is the condition for overflow in 2's complement addition.
b) Describe the single precision IEEE 754 Floating Point normal number format.
c) Find the range of both positive and negative single precision denormal numbers.

Problem II : Design and Timing Analysis of Carry Select Adder Circuits **5 + 5 = 10 Points**

a) You need to design two different carry select adder circuits for the addition of two 16-bit unsigned binary numbers.
One carry select adder circuit should be designed using 4-bit binary adder module only and the other carry select adder circuit should be designed using 8-bit binary adder module only.

Note: The Hardware components available to us in the form of blocks are 4x1 Multiplexer, 8x1 Multiplexer, 2x1 Multiplexer, 4-bit binary adder, 8-bit binary adder.

b) Calculate the longest path delay in both the circuits and write the equation in the form of the below-mentioned variables..

Timing Notations: Time taken by 4x1 Multiplexer = "$\mathbf{t_{4m}}$".
Time taken by 8x1 Multiplexer = "$\mathbf{t_{8m}}$".
Time taken by 2x1 Multiplexer = "$\mathbf{t_{2m}}$".
Time taken by 4-bit binary adder = "$\mathbf{t_{4a}}$".
Time taken by 8-bit binary adder = "$\mathbf{t_{8a}}$".

Problem III: Instruction Encoding **1+ 7 + 2 = 10 Points**

List of available instructions to programmers.

Instruction	Semantics	Syntax
Addition	reg1=reg1 + reg2	Add reg1, reg2
Subtraction	reg1=reg1 - reg2	Sub reg1, reg2
Multiplication	reg1=reg1 * reg2	Mul reg1, reg2
load	Load data from addr to reg1	Ld reg1 addr
move	Move content of reg2 to reg1	Mov reg1, reg2
Branch if equal to zero	Branch to addr if reg1 is equal to zero	Bz reg1 addr
Branch if not equal to zero	Branch to addr if reg3 is not equal to zero	Bnz reg3 addr

Syntax for Memory type instruction : <Opcode> <Filler Bits> <Register address> <Memory address>
Syntax for Register type instruction : <Opcode> <Filler Bits> <Destination Register Address> <Source Register Address>

In addition to the given instructions, you have 16 registers. Given that the opcode and register should be encoded in minimum binary representation and ISA can access 8-bit memory addresses.

Answer the following

1. What is the minimum number of bits required to represent the opcode of the given instructions.
2. Represent the above-mentioned instructions in terms of machine code using given syntax and within 16-bits only.

Note: The address to be chosen is $(0xAB)_{16}$.

3. Report the number of unused bits in all cases.

Problem IV: Assembly to Machine Code Translation **5 Points**

Assume a processor with 16 registers. Each of the registers is called by the processor by its corresponding value. Ex: R0 is called 0, R1 as 1, R2 as 2 and so on.

Mnemonic	add	mul	beq	sub
Binary	0001	0010	0100	1000

The instructions are represented as <opcode><destination register><source register 1><source register 2>.

For the following program, convert the given assembly code to machine code.

Program	add R7, R8, R10
	sub R15, R13, R2
	mul R5, R11, R14
	add R1, R3, R7
	mul R7, R8, R9