DVD Quiz 10

Rubrics

Q1. Why is Flash memories denser than SRAMs? Why are SRAMs better than Flash in terms of endurance? **(1+1 Marks)**

Ans. Flash store single bit of data on one transistor only, whereas in 6T SRAM's, we need 6 transistors to save one bit of data. Hence, the area of a flash cell is smaller than the SRAMs. But the SRAMs being static CMOS circuit with a bi-stable latch can handle more read-write operations compared to the flash as flash work on high input voltages which could lead to gate breakdown and other reliability issues.

Q2. What technique to save area is allowed to be used only in memory cell layouts & not in digital circuits? Why is it allowed? **(1+1 Marks)**

Ans. Long contacts are allowed to be made in memory cell layouts to save area. They are allowed to be used because memories are designed in a predefined pattern and the optics can be adjusted through resolution enhancement techniques (RET). Hence, we can have predefined masks for memories allowing long contacts which will not cause DRCs.

Q3. If devices in a 6T SRAM cell are sized as below in 65nm technology, which 2 figures of merit get degraded for each of them? Explain. **(2+2 Marks)**

a) PG: 280/65; PU: 120/80; PD: 260/80
b) PG: 180/65; PU: 220/65; PD: 260/65

Ans.

a) PG size is very large. This results in high BL leakage. Area also increases a little in comparison to case-2 **[1 Mark]**

Since Cell ratio is degraded significantly, SNM of the cell is bad **[1 Mark]**

b) Minimum length devices are used in the memory cell. So, cell leakage will be high. **[1 Mark]**

Since PU-ratio is degraded (>1), write operation is difficult and write margin of the cell will be bad. **[1 Mark]**

Q4. For a full adder draw the logic circuit for generation of Sum & Carry-out? **(1+1 Marks)**

Ans.

$Sum = A \oplus B \oplus C_{in}$

$Carry\_out = AB + B\,C_{in} + A\,C_{in}$