Q1. The truth table of the logic function is shown in Fig. 1.

A	B	C	F	
0	0	0	1	$\overline{B}$
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	0	$B+C$
1	0	1	1	
1	1	0	1	
1	1	1	1	

Fig. 1

We obtain F (A, B, C) = $\overline{B}$ for A = 0

F (A, B, C) = B + C for A = 1

(Give 10 marks if above expression is given correctly, otherwise for any other minimised expression give 5 marks)

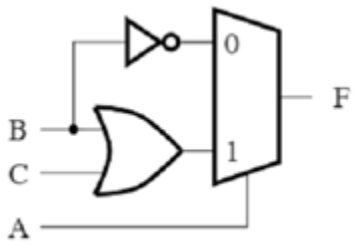
Using Shannon's Theorem, we can write

F (A, B, C) = A' F (0, B, C) + A F (1, B, C)

We have F (0, B, C) = B

F (1, B, C) = B + C

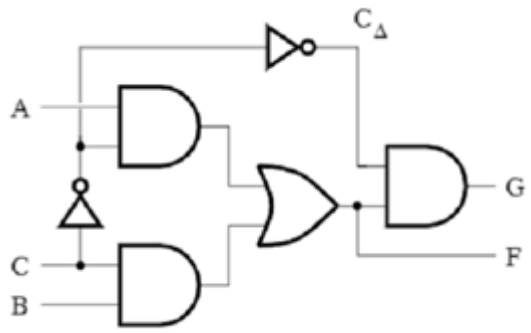
The logic function can be implemented as following:



This requires one 2:1 MULTIPLEXER, one OR gate and one NOT gate

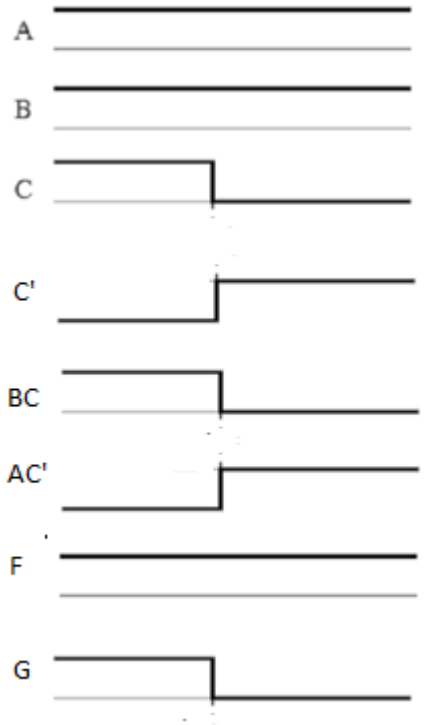
(4 marks for above logical expression and 6 marks for above logic realisation by using 1 OR, 1 NOT and 1 2:1 MUX. Otherwise 4 marks if more gates or MUX are used.)

Q.2

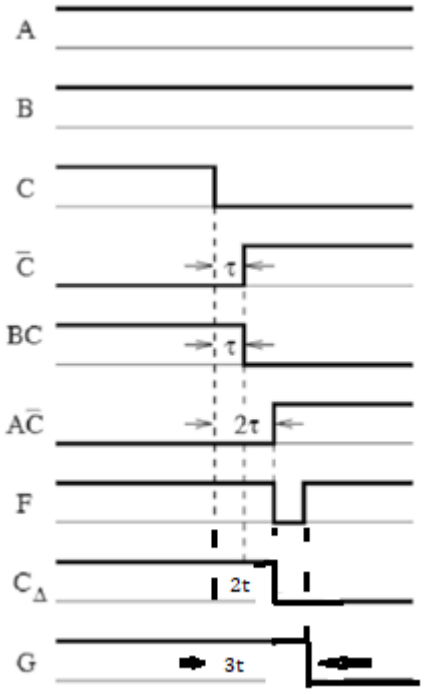


F = A C’ + B C

G = F . C

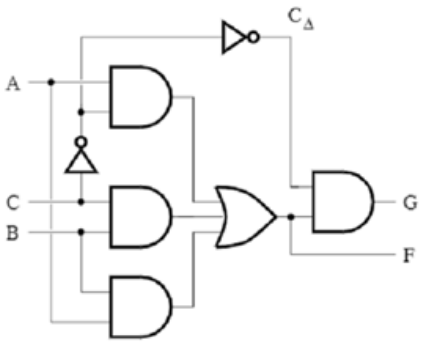


Output with $\tau = 0$



Output with $\tau = T$

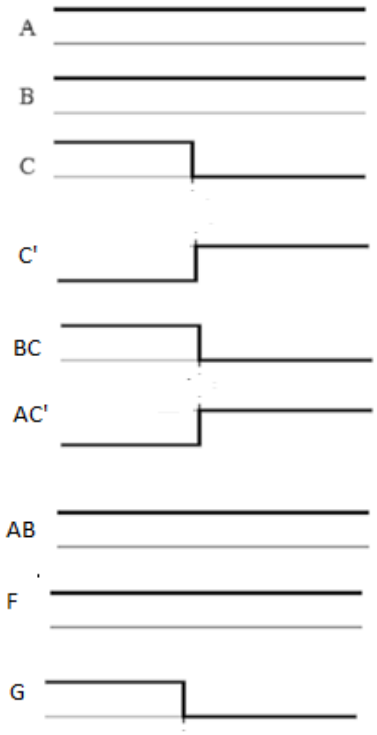
Figure 1a



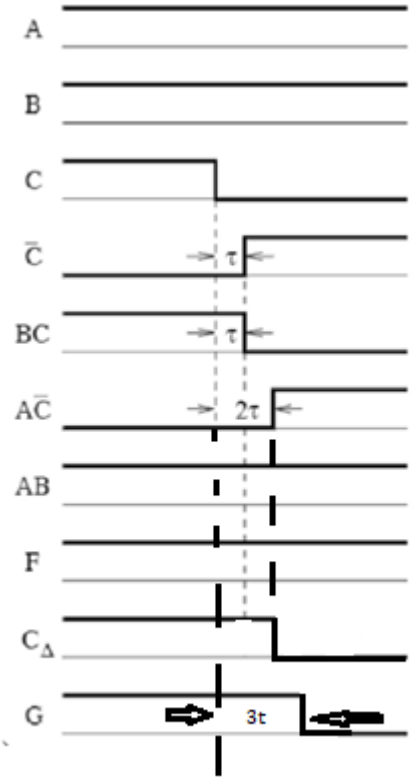
F = A C' + B C

G = F . C

(For correct Logic expression for F and G 2 Marks, one marks each for Fig. 1a and Fig. 1b).



Output with $\tau = 0$



Output with $\tau = T$

Figure 1b

(Give 3 marks each for drawing the correct waveforms with $\tau = 0$ i.e. 2 X 3 = 6, otherwise 1 marks for partial correct answer with more than half waveform correct. For $\tau = T$, give 5 marks for correct answers i.e. 2 X 5 = 10. Other wise 2 marks for partial correct answer with more than half waveform correct,)

The circuit Fig. 1a exhibit Dynamic hazard due to two concurrent paths with asymmetrical propagation delays. By adding a redundant term A.B in Fig. 1b to eliminate the static hazard as shown. This leads to eliminating the dynamic hazard in the logic circuit. **(2 Marks for correct answer.)**

Q.3 The truth table for 2 bit multiplier is shown in Fig, 2.

$X \cdot Y = Z$	X		Y		Z			
	X_1	X_0	Y_1	Y_0	Z_3	Z_2	Z_1	Z_0
$0 \cdot 0 = 0$	0	0	0	0	0	0	0	0
$0 \cdot 1 = 0$	0	0	0	1	0	0	0	0
$0 \cdot 2 = 0$	0	0	1	0	0	0	0	0
$0 \cdot 3 = 0$	0	0	1	1	0	0	0	0
$1 \cdot 0 = 0$	0	1	0	0	0	0	0	0
$1 \cdot 1 = 1$	0	1	0	1	0	0	0	1
$1 \cdot 2 = 2$	0	1	1	0	0	0	1	0
$1 \cdot 3 = 3$	0	1	1	1	0	0	1	1
$2 \cdot 0 = 0$	1	0	0	0	0	0	0	0
$2 \cdot 1 = 2$	1	0	0	1	0	0	1	0
$2 \cdot 2 = 4$	1	0	1	0	0	1	0	0
$2 \cdot 3 = 6$	1	0	1	1	0	1	1	0
$3 \cdot 0 = 0$	1	1	0	0	0	0	0	0
$3 \cdot 1 = 3$	1	1	0	1	0	0	1	1
$3 \cdot 2 = 6$	1	1	1	0	0	1	1	0
$3 \cdot 3 = 9$	1	1	1	1	1	0	0	1

Fig. 2

(6 Marks for correct truth table. Deduct marks proportionately for incorrect result)

From above truth table we obtain,

$$Z_0 = \overline{X_1} \cdot X_0 \cdot \overline{Y_1} \cdot Y_0 + \overline{X_1} \cdot X_0 \cdot Y_1 \cdot Y_0 + X_1 \cdot X_0 \cdot \overline{Y_1} \cdot Y_0 + X_1 \cdot X_0 \cdot Y_1 \cdot Y_0$$

$$= X_0 \cdot Y_0$$

$$Z_1 = \overline{X_1} \cdot X_0 \cdot Y_1 \cdot \overline{Y_0} + \overline{X_1} \cdot X_0 \cdot Y_1 \cdot Y_0 + X_1 \cdot \overline{X_0} \cdot \overline{Y_1} \cdot Y_0 + X_1 \cdot \overline{X_0} \cdot Y_1 \cdot Y_0 + X_1 \cdot X_0 \cdot \overline{Y_1} \cdot Y_0 + X_1 \cdot X_0 \cdot Y_1 \cdot \overline{Y_0}$$

$$= \overline{X_1} \cdot X_0 \cdot Y_1 + X_0 \cdot Y_1 \cdot \overline{Y_0} + X_1 \cdot \overline{X_0} \cdot Y_0 + X_1 \cdot \overline{Y_1} \cdot Y_0$$

$$Z_2 = X_1 \cdot \overline{X_0} \cdot Y_1 \cdot \overline{Y_0} + X_1 \cdot \overline{X_0} \cdot Y_1 \cdot Y_0 + X_1 \cdot X_0 \cdot Y_1 \cdot \overline{Y_0}$$

$$= X_1 \cdot \overline{X_0} \cdot Y_1 + X_1 \cdot Y_1 \cdot \overline{Y_0}$$

$$Z_3 = X_1 \cdot X_0 \cdot Y_1 \cdot Y_0$$

(Minimisation can be done using Karnaugh maps as well)

(2 marks for each correct expression i.e. 4 X 2 – 8)

Logic Circuit of Multiplier is shown in Fig. 2.

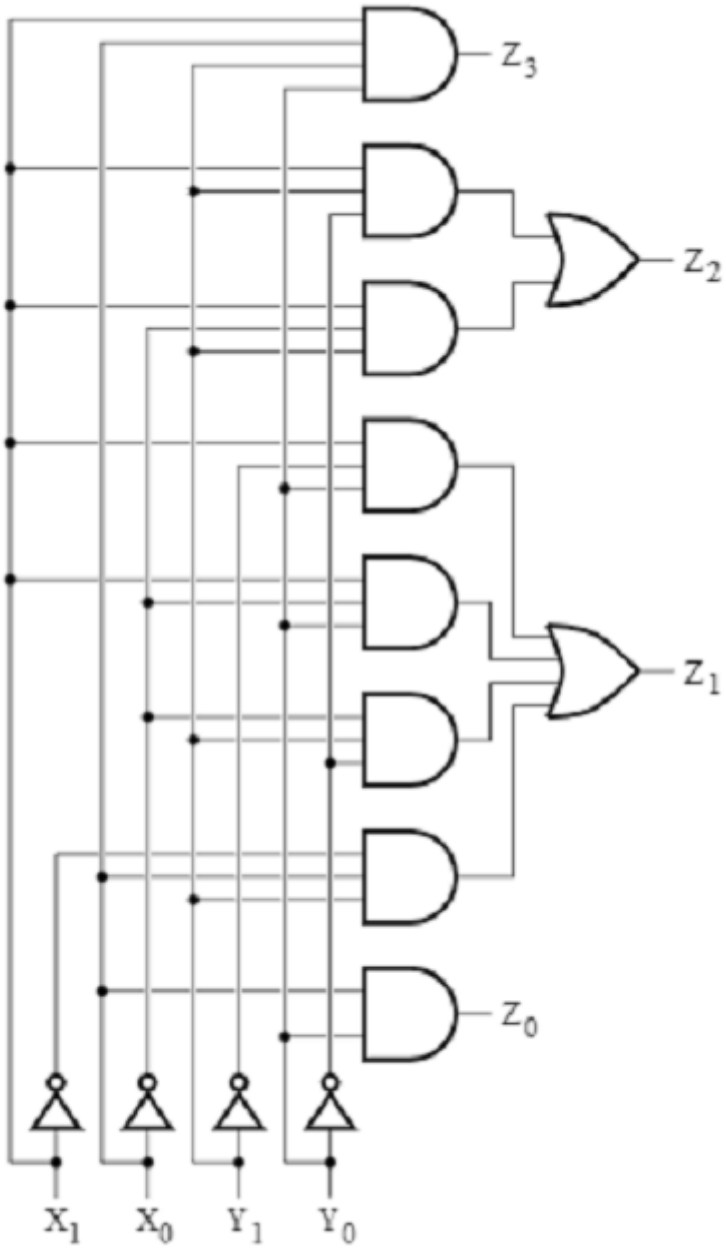


Fig. 2

(6 marks for correct realisation. For partial correct answers, deduct marks proportionately.)