CSE/ECE 511: Quiz 2: Set A

Note: Institute Plagiarism policy applies.

Q1. For the program given below. answer the following questions. **[10 Marks]**

```
ADD R1, R2, R3
SUB R2, R4, R5
MUL R5, R2, R3
DIV  R1, R4, R5
```

a. Determine all dependencies (RAW, WAR & WAW) and their type for the above program. **[5 Marks]**
b. There are 16 physical registers (p1-p16). Initially architectural registers R1 to R8 are mapped to physical registers p1 to p8 respectively. Rewrite the above program such that only true data dependencies remain. **[5 Marks]**

Q2. Consider the following high-level language program, which is compiled into the following assembly language program. **[20 Marks]**

High-level language

```
while (i < N)
{
        A[i] = B[i] + i;
        i++;
}
```

Assembly language:

R1 stores the base address of array B, and R2 stores the base address of array A

```
loop:   lw F1, 0(R1)
        addiu R1, R1, 4
        add.s F2, R3, F1
        sw F2, 0(R2)
        addiu R2, R2, 4
        addiu R3, R3,1
        bne R3, R4,loop
```

Consider a VLIW EQ compiler with the processor having one integer unit, one floating point unit and one load/store unit. *addiu* takes one clock cycle, *add.s* (floating point addition) takes two clock cycles, and *lw* and *sw* take four clock cycles. Assume branch instruction is executed in integer units. Assume the compiler does not reorder the instructions.

a. Pack the instructions for the above program. Determine the Floating Point Operation per second (FLOPS). **[4+1 Marks]**
b. Assuming 16 integer registers and 16 floating point registers, unroll the loop to perform three iterations at once. **[7.5 Marks]**
c. Pack the instructions for the unrolled program. Determine the FLOPS. **[6+1 Marks]**
d. Determine the gain in FLOPS post-loop unrolling and explain the reason for the gain. **[0.5 Marks]**

CSE/ECE 511: Quiz 2: Set B

Note: Institute Plagiarism policy applies.

Q1. For the program given below. answer the following questions.

```
SUB R7, R2, R3
SUB R5, R4, R1
MUL R1, R5, R3
ADD R7, R4, R6
```

a. Determine all dependencies (RAW, WAR & WAW) and their type for the above program. **[5 Marks]**
b. There are 16 physical registers (x1-x16). Initially architectural registers R1 to R8 are mapped to physical registers x1 to x8 respectively. Rewrite the above program such that only true data dependencies remain. **[5 Marks]**

Q2. Consider the following high-level language program, which is compiled into the following assembly language program.

High-level language

```
while (i < N)
{
        A[i] = B[i] + i;
        i = i + 2 ;
}
```

Assembly language:
R1 stores the base address of array B, and R2 stores the base address of array A

```
loop:   lw F1, 0(R1)
        addiu R1, R1, 4
        add.s F2, R3, F1
        sw F2, 0(R2)
        addiu R2, R2, 4
        addiu R3, R3, 2
        bne R3, R4, loop
```

Consider a VLIW EQ compiler with the processor having one integer unit, one floating point unit and one load/store unit. addiu takes one clock cycle, *add.s* (floating point addition) takes two clock cycles, and lw and sw take five clock cycles. Assume branch instruction is executed in integer units. Assume the compiler does not reorder the instruction.

a. Pack the instructions for the above program. Determine the Floating Point Operation per second (FLOPS). **[4 +1 Marks]**
b. Assuming 16 integer registers and 16 floating point registers, unroll the loop to perform three iterations at once. **[7.5 Marks]**
c. Pack the instructions for the unrolled program. Determine the FLOPS. **[6+1 Marks]**
d. Determine the gain in FLOPS post-loop unrolling and explain the reason for the gain. **[0.5 Marks]**

CSE/ECE 511: Quiz 2: Set C

Note: Institute Plagiarism policy applies.

Q1. For the program given below. answer the following questions.

```
ADD R7, R2, R3
SUB R4, R4, R1
DIV  R1, R4, R3
ADD R7, R4, R6
```

a. Determine all dependencies (RAW, WAR & WAW) and their type for the above program. **[5 Marks]**
b. There are 16 physical registers (e1-e16). Initially architectural registers R1 to R8 are mapped to physical registers e1 to e8 respectively. Rewrite the above program such that only true data dependencies remain. **[5 Marks]**

Q2. Consider the following high-level language program, which is compiled into the following assembly language program.

High-level language

```
while (i < N)
{
        A[i] = B[i] + i;
        I = i+3;
}
```

Assembly language:
R1 stores the base address of array B, and R2 stores the base address of array A

```
loop:   lw F1, 0(R1)
        addiu R1, R1, 4
        add.s F2, R3, F1
        sw F2, 0(R2)
        addiu R2, R2, 4
        addiu R3, R3, 3
        bne R3, R4, loop
```

Consider a VLIW EQ compiler with the processor having one integer unit, one floating point unit and one load/store unit. addiu take one clock cycle, *add.s* (floating point addition) takes two clock cycles, and lw and sw take five clock cycles. Assume branch instruction is executed in integer units. Assume the compiler does not reorder the instruction.

a. Pack the instructions for the above program. Determine the Floating Point Operation per second (FLOPS). **[4 +1 Marks]**
b. Assuming 16 integer registers and 16 floating point registers, unroll the loop to perform three iterations at once. **[7.5 Marks]**
c. Pack the instructions for the unrolled program. Determine the FLOPS. **[6+1 Marks]**
d. Determine the gain in FLOPS post-loop unrolling and explain the reason for the gain. **[0.5 Marks]**