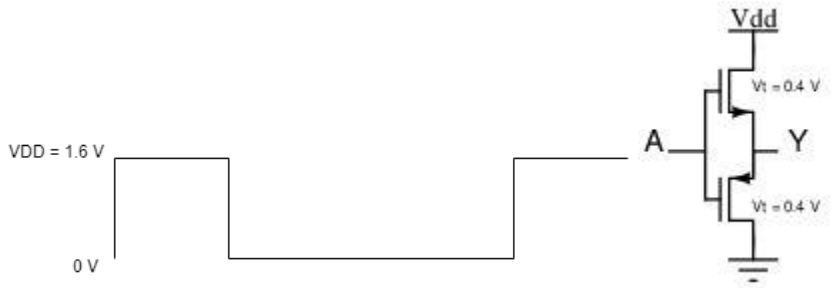
DVD Quiz 6 Rubric

Q1. Draw the output waveform for the given input waveform for the given circuit and support your answer conceptually.

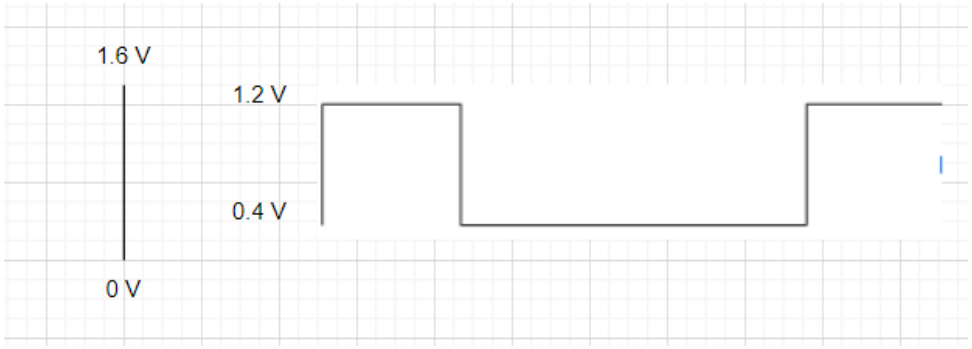


[2 Marks]

Answer:

Since NMOS cannot pass a strong 1 & PMOS cannot pass a strong 0 so we will have Vt drops across them and the swing will reduce accordingly.

[1 Mark]



[1 Mark]

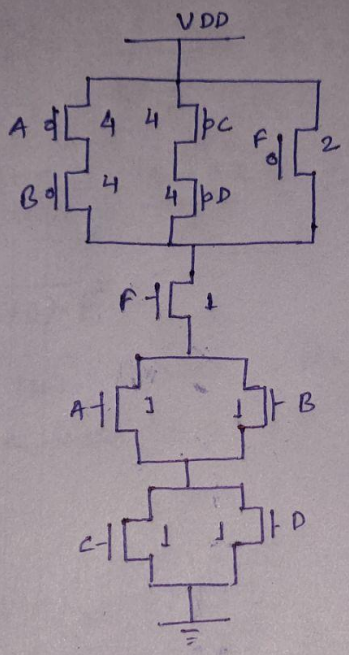
Q.2 Calculate the logical effort of input F (average) for the following skewed gates.
For simplicity, assume that any change in width will be done by a factor of 3, for making low or high skewed gates. Consider F as the inner input for making circuit of the below function.

High Skewed : $Y = \overline{(A+B) \cdot (C+D) \cdot F}$ [3 Marks]

Answer

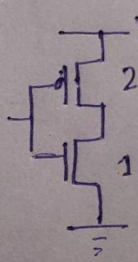
q2) $Y = \overline{(A+B)\cdot(C+D)\cdot F}$

i) For high skewed case we have to downsize the NMOS. So instead of 3 we keep it 1 (∵ width is decreased by a factor of 3). Also, F is critical input



for asymmetric gates, the reference inverter is taken accordingly to equal rise resistance & equal fall resistan

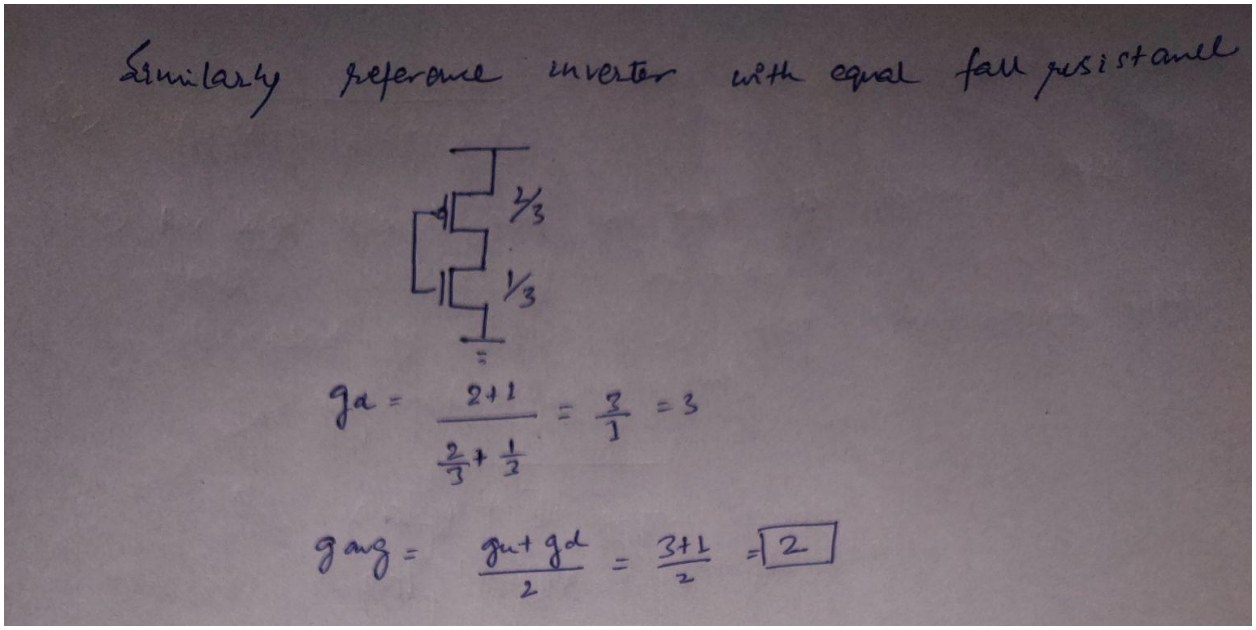
For given design, the inverter with equal rise resistance is



Therefore $g_u = \frac{2+1}{2+1} = 1$

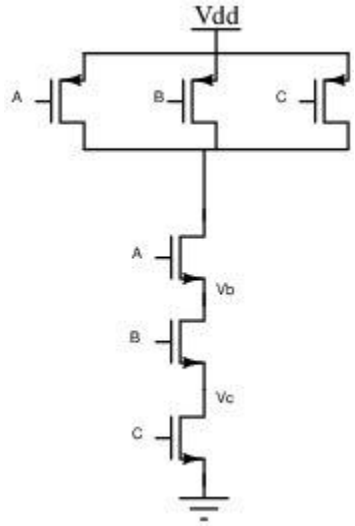
← Gate cap for the given circuit of F i/p

← gate cap of the reference inverter



Q3. In a 3 input NAND Gate the leakage power consumption drastically reduces on some input combinations (A=0, B=0, C=0). Explain the phenomenon with the help of a schematic diagram.. [2 Marks]

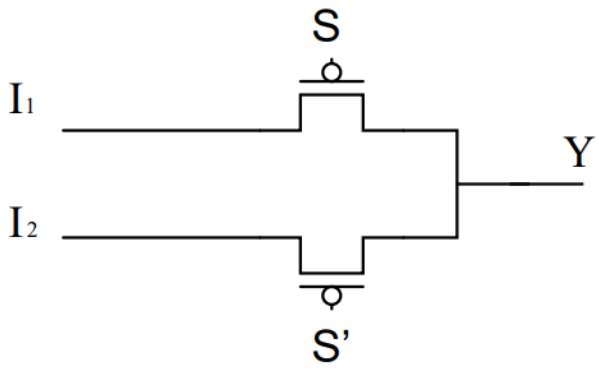
Answer:



This happens due to the stacking effect [0.5 Marks]. When A, B & C inputs are 0 then the Vb and Vc nodes are not pulled to the ground; they have certain potential depending on the resistance of the NMOS. Due to this Vsb increases and this leads to an increase of Vt of the device [0.5 Marks]. Leakage is inversely proportional to Vt so Leakage reduces [0.5 Marks] Also, Vgs is negative for A & B NMOS and zero for C, this leads to a reduction in gate leakage. [0.5 Marks]

Q4. What function/ functionality does the circuit represent? What is the problem in the implementation below? How would you correct it? Draw the modified circuit diagram

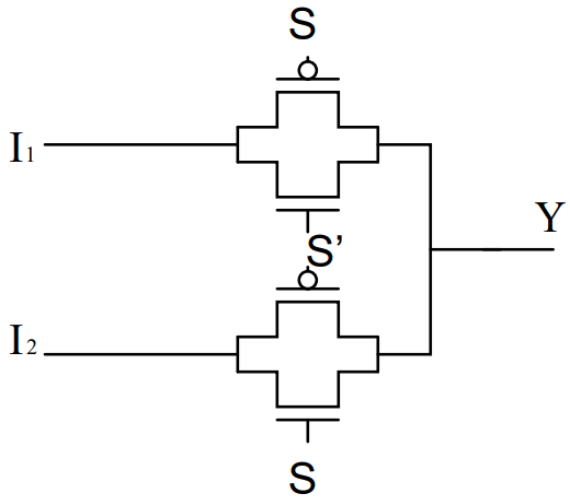
[0.5 +0.5+1 marks]



Answer:

The figure represents the MUX circuit. PMOS pass weak 0, so if the selected input is 0 then the output will be Vth of PMOS rather than 0.

We can improve the circuit by making a transmission gate implementation of the MUX circuit.



Q5. What is the challenge with transmission gate networks? How can we resolve it?

[0.5 +0.5 marks]

Answer:

The long-chain transmission gate network has very high RC delays.

This can be resolved by adding buffers after a few stages.