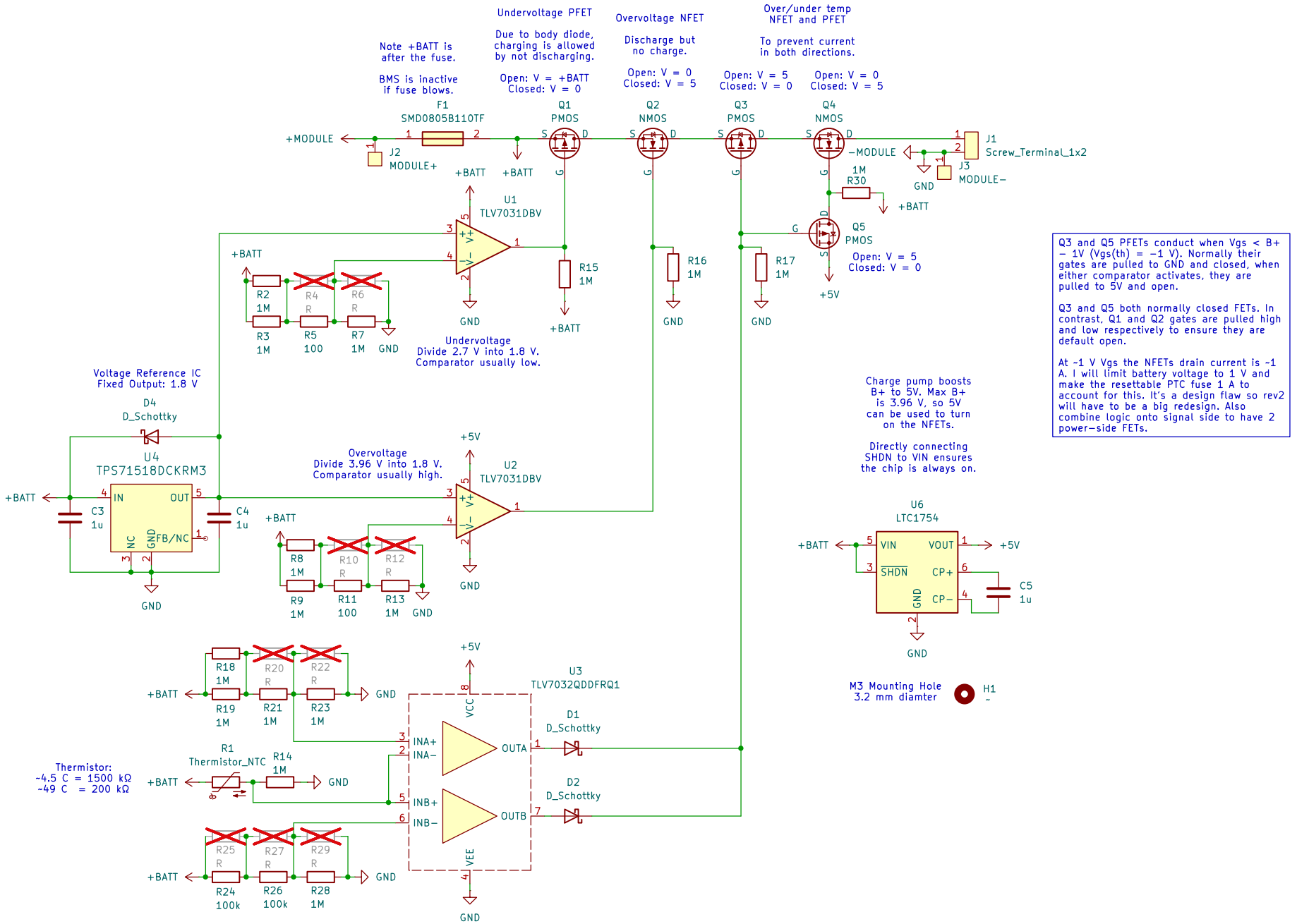
Undervoltage PFET
Due to body diode, charging is allowed by not discharging.
Open: V = +BATT
Closed: V = 0
Overvoltage NFET
Discharge but no charge.
Open: V = 0
Closed: V = 5
Over/under temp NFET and PFET
To prevent current in both directions.
Open: V = 5
Closed: V = 0
Open: V = 0
Closed: V = 5
Note +BATT is after the fuse.
BMS is inactive if fuse blows.
F1
SMD0805B110TF
Q1
PMOS
Q2
NMOS
Q3
PMOS
Q4
NMOS
+MODULE
J2
MODULE+
+BATT
U1
TLV7031DBV
R15
1M
R16
1M
R17
1M
R30
1M
Q5
PMOS
Open: V = 5
Closed: V = 0
−MODULE
J1
Screw_Terminal_1x2
J3
MODULE−
GND
+5V
R2
1M
R4
R
R6
R
R3
1M
R5
100
R7
1M
Undervoltage
Divide 2.7 V into 1.8 V.
Comparator usually low.
Q3 and Q5 PFETs conduct when Vgs < B+ − 1V (Vgs(th) = −1 V). Normally their gates are pulled to GND and closed, when either comparator activates, they are pulled to 5V and open.
Q3 and Q5 both normally closed FETs. In contrast, Q1 and Q2 gates are pulled high and low respectively to ensure they are default open.
At ~1 V Vgs the NFETs drain current is ~1 A. I will limit battery voltage to 1 V and make the resettable PTC fuse 1 A to account for this. It's a design flaw so rev2 will have to be a big redesign. Also combine logic onto signal side to have 2 power−side FETs.
Voltage Reference IC
Fixed Output: 1.8 V
D4
D_Schottky
U4
TPS71518DCKRM3
IN
OUT
NC
GND
FB/NC
C3
1u
C4
1u
Overvoltage
Divide 3.96 V into 1.8 V.
Comparator usually high.
U2
TLV7031DBV
R8
1M
R10
R
R12
R
R9
1M
R11
100
R13
1M
Charge pump boosts B+ to 5V. Max B+ is 3.96 V, so 5V can be used to turn on the NFETs.
Directly connecting SHDN to VIN ensures the chip is always on.
U6
LTC1754
VIN
VOUT
SHDN
CP+
CP−
C5
1u
M3 Mounting Hole
3.2 mm diamter
H1
~
R18
1M
R20
R
R22
R
R19
1M
R21
1M
R23
1M
U3
TLV7032QDDFRQ1
VCC
VEE
INA+
INA−
INB+
INB−
OUTA
OUTB
D1
D_Schottky
D2
D_Schottky
R1
Thermistor_NTC
R14
1M
Thermistor:
~4.5 C = 1500 kΩ
~49 C = 200 kΩ
R25
R
R27
R
R29
R
R24
100k
R26
100k
R28
1M