Design Review

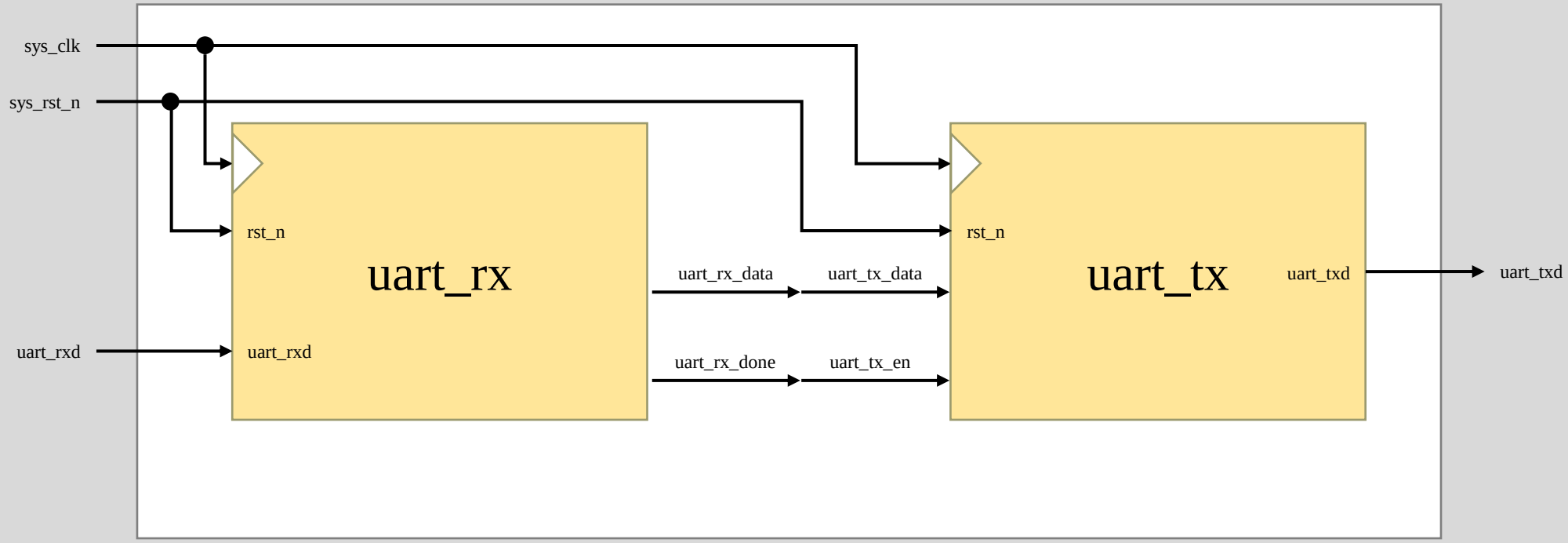
UART

Presenter: Chi Lee

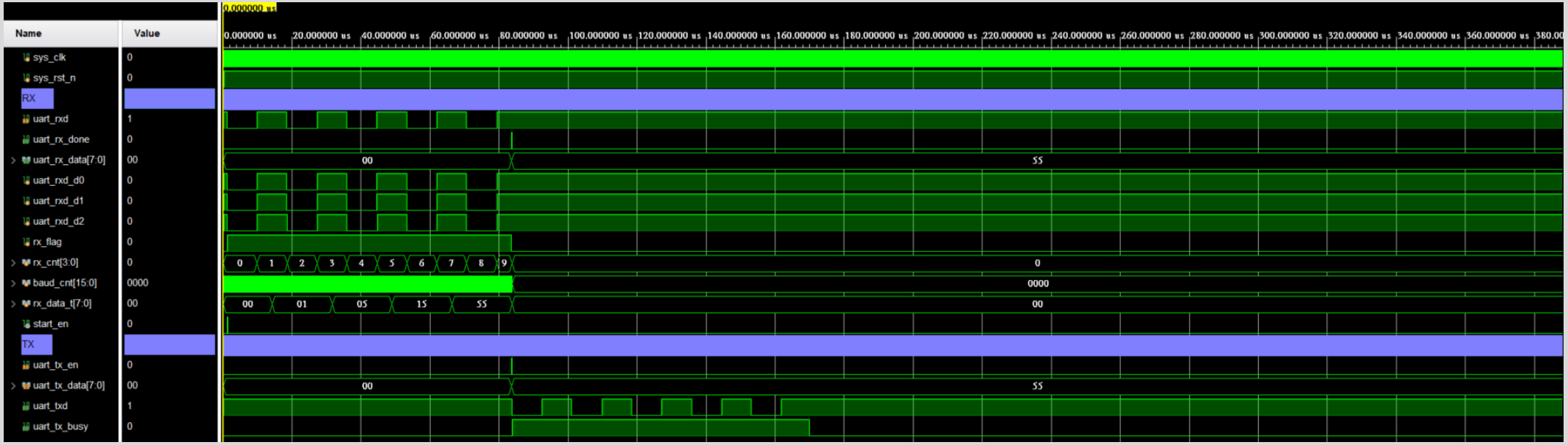
Overview

- FPGA Clock : 100 MHz
- FPGA Part : Xilinx xc7a35tcpg236-1
- HDL Editor : VScode
- EDA Tool : Vivado v2019.2
- UART Baud Rate : 115200 bps

System Block



Pre-layout Simulation



Thank you