CLJD

Progress Report

<2019-10-17>

Draft Description

The Arithmetic Logic Unit, or ALU, for our purposes will be used with a set of inputs both data and instruction to perform different arithmetic operations. Once the arithmetic operations are calculated, the ALU will generate an output. As stated, the ALU will “calculate” the different inputs given, similarly to a calculator. The major functions on the ALU will be to add, subtract, multiply, and divide.

In order to perform these math functions, the ALU will need to handle the following basic logic functions: ANDing, ORing, XORing, NOTing, NANDing, NORing, and XNORing. Since the ALU is still in the process of being coded, it’s possible that not *every* one of the logic functions will be used; however, it is likely that they will. Lastly, the ALU should be able to handle overflow and carry-over errors if presented with such.

This group’s ALU will have numbers of 16 bit integers. The ALU will be coded using Verilog as a central language. The environments and workspaces will differ throughout the team members, as long as the ALU is coded in Verilog and it follows the described instructions above.

The overall purpose of the ALU is simply to perform simple calculations via a combinational digital logic circuit, and to follow the requirements specifications listed in Dr. Becker’s project description.

Draft Member Tasks

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Charles | Liora | Jacob | Dylan |
| Updated Report | | | | |
| Title Page | \* |  |  | \* |
| Updated Report |  |  |  | \* |
| Updated Description |  |  |  | \* |
| Updated Member Task List | \* | \* | \* | \* |
| Updated Software Discovery |  | \* |  |  |
| Updated Participation  Census |  | \* |  |  |
| System Design | | | | |
| Title Page | \* |  |  |  |
| Parts List |  |  |  | \* |
| Input List |  |  |  | \* |
| Output List |  |  |  | \* |
| Interface List |  |  |  | \* |
| Module List | \* |  |  |  |
| Mode List |  | \* |  |  |
| Circuit Diagram |  |  | \* |  |
| State Machine Diagram |  |  | \* |  |
| Code and Output | | | | |
| Add | \* |  |  |  |
| Subtract |  | \* |  |  |
| Multiply |  |  |  | \* |
| Divide |  |  | \* |  |
| Bit Shift | \* |  |  |  |

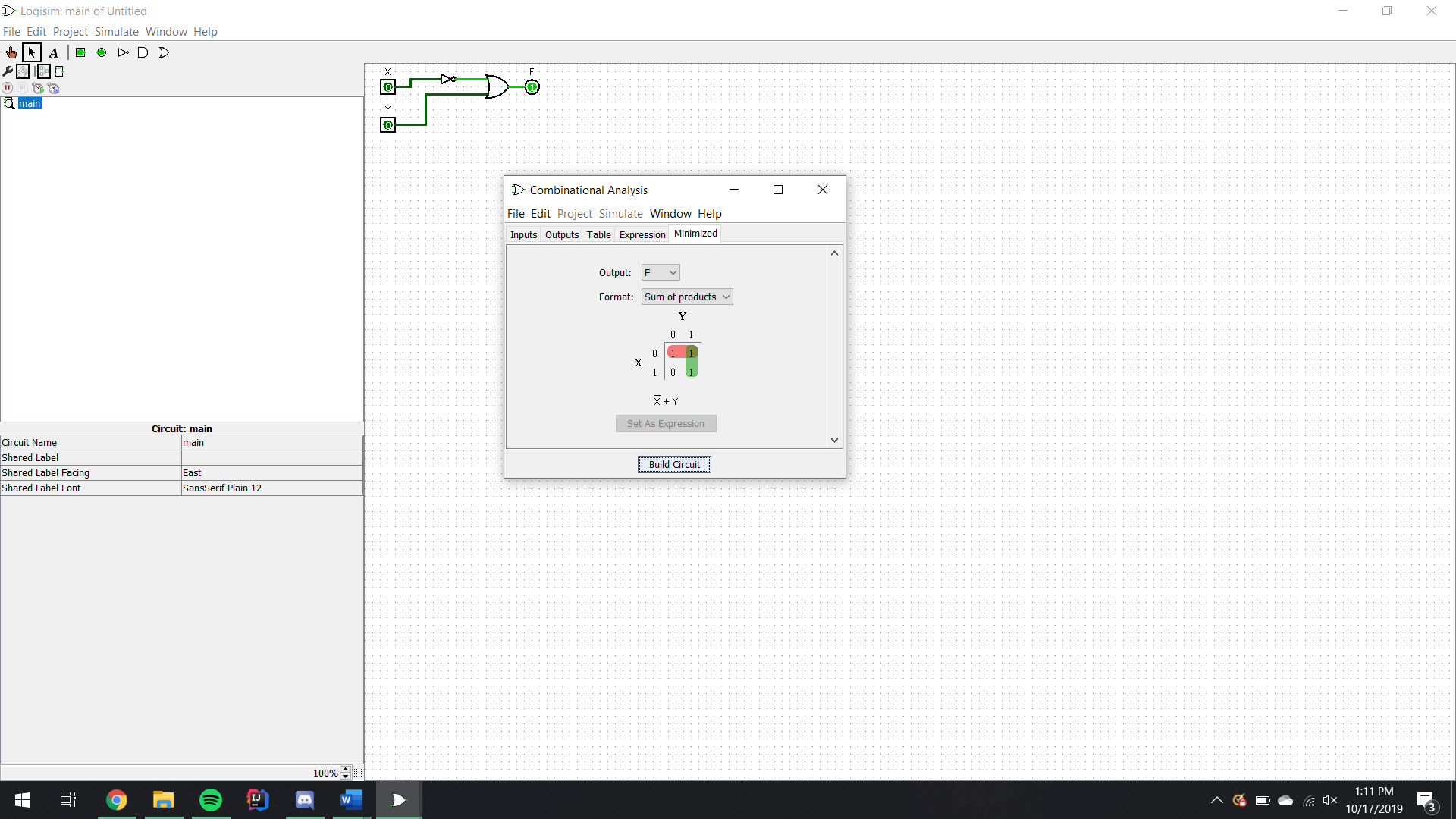
Draft Software Discovery

The circuit development software we are using for our ALU project is Logisim. Logisim is an open source software (GPL) graphical tool designed for creating and testing digital logic circuits. It has an easily accessible toolbar interface which enables quick learning and implementation of circuit diagrams for all skill levels. Logisim is used widely around the world in most colleges and universities, which gives proof to its quality.

One key feature of Logisim is it being free and able to run on any machine supporting Java 5 or later. Since Java 8 was released in 2014, it is safe to say all machines today support Java 5 or later. Apart from running on any machine, another key feature of Logisim is its ability to automatically generate circuits and k-maps based on Boolean logic and truth tables set by the user. To further that, the user has the option to create the circuit only using NAND gates, which is significant because any function can be implemented this way and results in cheaper circuits. This can all be done in the “combinational analysis” module in the software. Circuits can also be used as sub-circuits of other circuits, which practices the concept of hierarchical circuit design. While creating circuits, the wiring tool draws vertical and horizontal wires that automatically connects to components and other wires, all of which are color-coded in order to aid in design and debugging of the system. Furthermore, Logisim has a large component library which is organized by the tabs on the left of the interface under “wiring”, “gates”, “plexers”, “arithmetic”, “memory”, “input/output”, and “base” that the user can choose from while creating a circuit. Once users are satisfied, completed circuits can be saved into a file or exported to a GIF file.

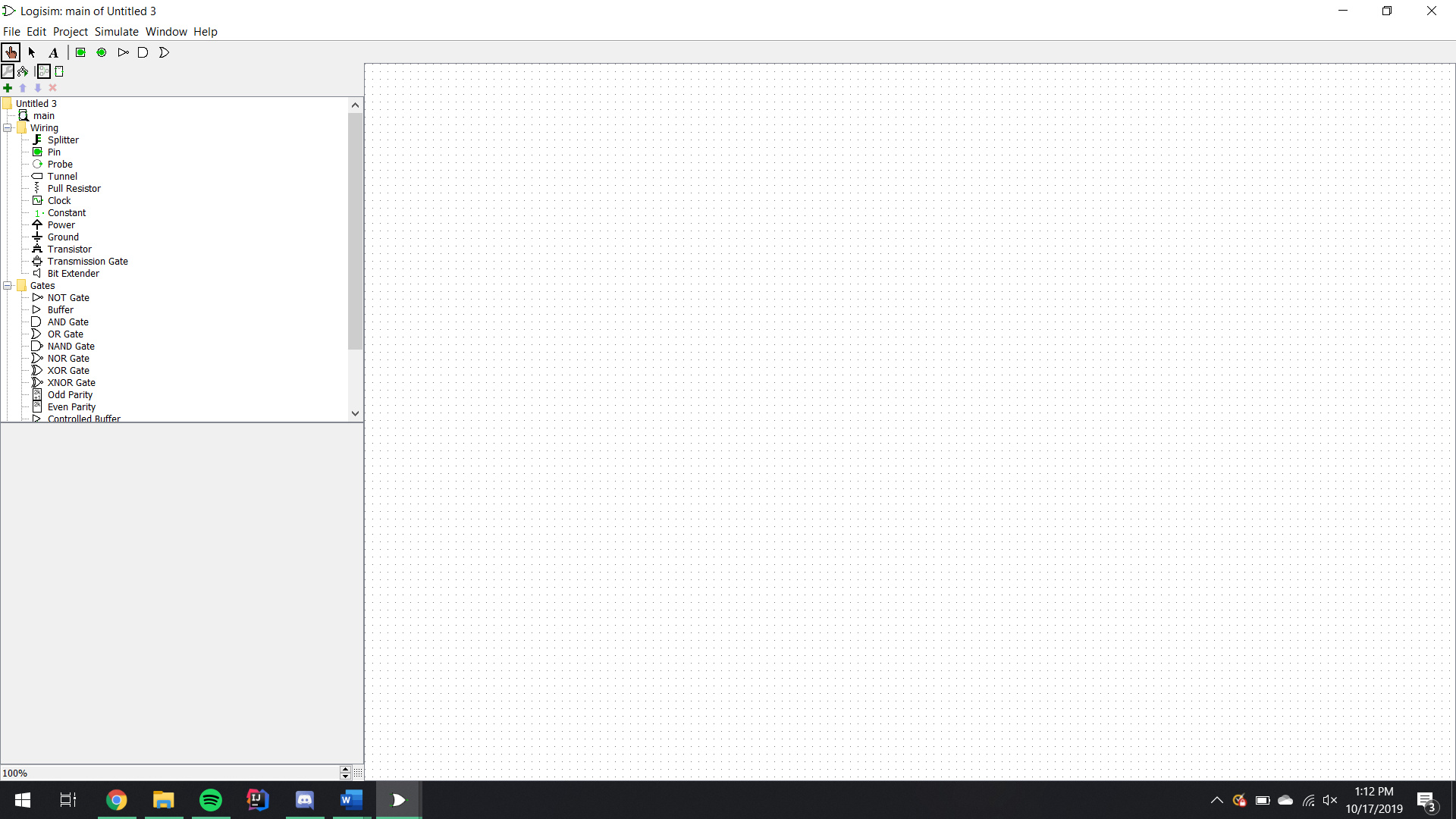
One thing to note about Logisim is its lack of updates. The developer of Logisim suspended the development of the software indefinitely starting October 11, 2014. Even though no updates have been made since then, Logisim is still a great software to download for creating circuits. There has been 9,633 downloads this week for Windows, and a total of 84 reviews resulting in 4.5 stars. You can download the software from its respective sourceforge.net page, resulting in a very quick and easy download process.

The type and version of Verilog we are using is iVerilog version 10.2.

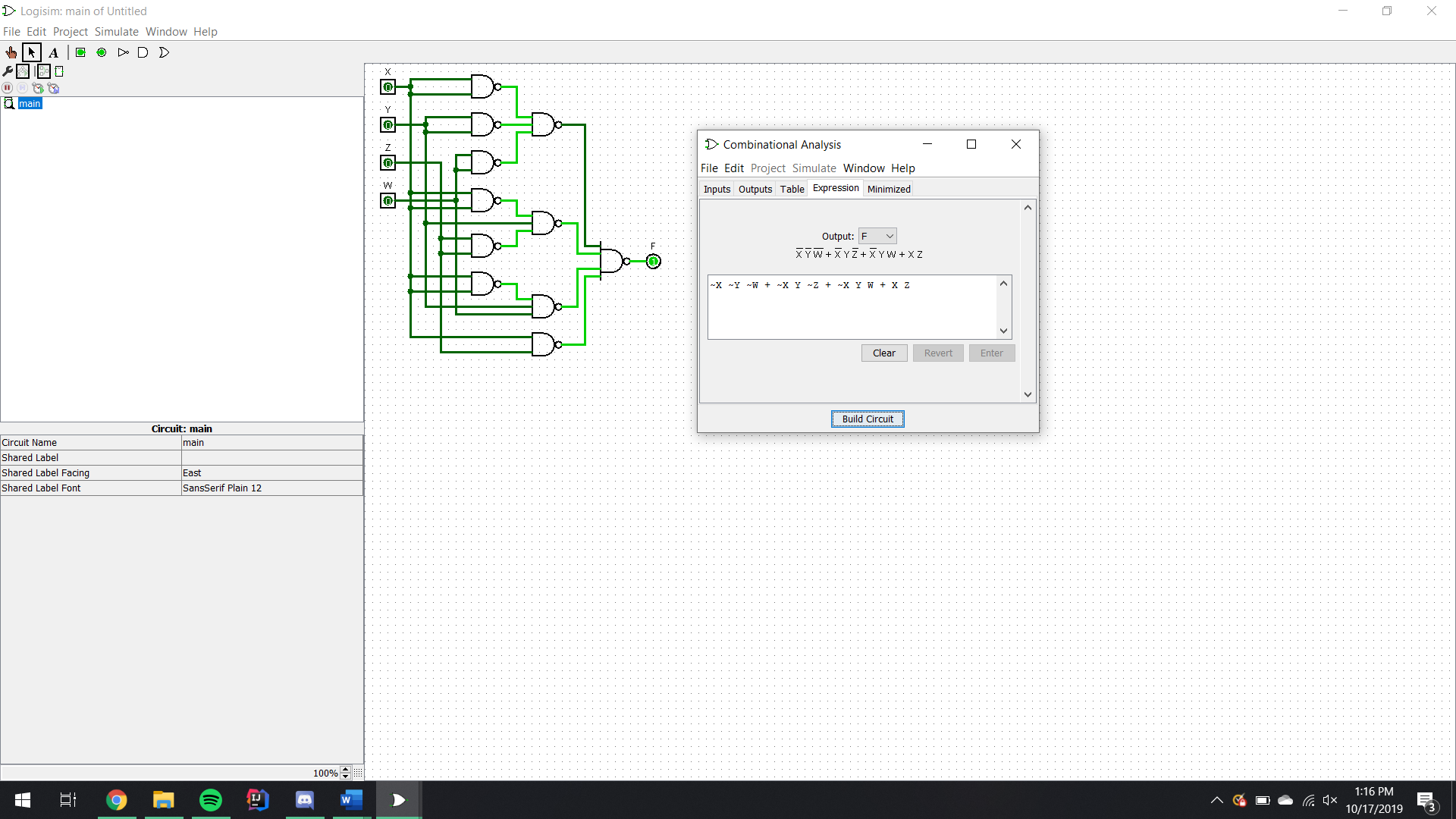


k-map automatically generated, Logisim

Component Library under tabs on left



Boolean logic expression shown, and circuit automatically drawn using NAND gates



Participation Census