CLJD

Progress Report

<2019-10-17>

Draft Description

The Arithmetic Logic Unit, or ALU, for our purposes will be used with a set of inputs both data and instruction to perform different arithmetic operations. Once the arithmetic operations are calculated, the ALU will generate an output. As stated, the ALU will “calculate” the different inputs given, similarly to a calculator. The major functions on the ALU will be to add, subtract, multiply, and divide.

In order to perform these math functions, the ALU will need to handle the following basic logic functions: ANDing, ORing, XORing, NOTing, NANDing, NORing, and XNORing. Since the ALU is still in the process of being coded, it’s possible that not *every* one of the logic functions will be used; however, it is likely that they will. Lastly, the ALU should be able to handle overflow and carry-over errors if presented with such.

This group’s ALU will have numbers of 16 bit integers. The ALU will be coded using Verilog as a central language. The environments and workspaces will differ throughout the team members, as long as the ALU is coded in Verilog and it follows the described instructions above.

The overall purpose of the ALU is simply to perform simple calculations via a combinational digital logic circuit, and to follow the requirements specifications listed in Dr. Becker’s project description.

Draft Member Tasks

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Charles | Liora | Jacob | Dylan |
| Updated Report | | | | |
| Title Page | \* |  |  | \* |
| Updated Report |  |  |  | \* |
| Updated Description |  |  |  | \* |
| Updated Member Task List | \* | \* | \* | \* |
| Updated Software Discovery |  | \* |  |  |
| Updated Participation  Census |  | \* |  |  |
| System Design | | | | |
| Title Page | \* |  |  |  |
| Parts List |  |  |  | \* |
| Input List |  |  |  | \* |
| Output List |  |  |  | \* |
| Interface List |  |  |  | \* |
| Module List | \* |  |  |  |
| Mode List |  | \* |  |  |
| Circuit Diagram |  |  | \* |  |
| State Machine Diagram |  |  | \* |  |
| Code and Output | | | | |
| Add | \* |  |  |  |
| Subtract |  | \* |  |  |
| Multiply |  |  |  | \* |
| Divide |  |  | \* |  |
| Bit Shift | \* |  |  |  |

Draft Software Discovery

Participation Census