CLJD

Updated Report

<2019-11-21>

Updated Description

The Arithmetic Logic Unit, or ALU as descripted in the draft description, still fulfils the requirements of taking a set of data and instruction inputs to perform different arithmetic operations. The ALU calculates these inputs, as if it were a calculator. The ALU functions fulfilled are add, subtract, multiply, and divide. The size of the numbers being calculated are 16 bit integers, thus we have carry-over and overflow errors that the ALU handles. The ALU reflected from this report can perform the following basic logic functions: ANDing, ORing, XORing, NOTing, NANDing, NORing, and XNORing.

**The obvious but unforeseen carry-over error that was added is handling carry-over in the multiply module.** Another unforeseen error handle which was not explicitly stated in the first progress report is **handling a divide-by-zero error**. The divide module currently reflects this error handle. **We have also defined a decoder, multiplexer, and a state machine** which was not originally defined in the draft description.

Our development workspaces differ but we are still using Verilog version 10.1 as the central language.

The overall purpose of the ALU is to perform simple calculations via a combinational digital logic circuit, and to follow the requirements specifications listed in Dr. Becker’s project description.

Updated Report

Updated Member Task List

Updated Software Discovery

Updated Participation Census