UNO R3			UNO R4	
Interface	**#**	**Description**	**#**	**Description**
			8	PWM Timers (2 * 32bits / 6 * 16bits)
Timer 16 bits	3	Timers (2 * 8bits / 1 * 16bits)	2	
RealTime counter	1		1	
PWM channel	6		8	
ADC channels	6	ADC 10 bit. PDIP package	1	ADC 14 Bits
Serial USART	1		4	
SPI Interface	1		2	
WD Timer	1		1	
Analog comparator	1	On chip	2	Analog Comparator 8 bits
Interrupt and Wake Up on pin change	1		1	
I2C	1		2	
			1	DAC 12 bits

JANALOG

UNO R3								UNO R4					
Pin	**Function**	**Type**	**Direction**	**Pull-Up**	**Description for GRBL**	**CPU Channel**	**Bit**	**Pin**	**Function**	**Type**	**Direction**	**Pull-Up**	**Description for GRBL**
1	NC	NC						1	BOOT	NC			MD
2	IOREF	IOREF						2	IOREF	IOREF			Reference for digital logic V - connected to 5 V
3	Reset	Reset				C	6	3	Reset	Reset			Reset
4	+3V3	Power						4	+3V3	Power			+3V3 Power Rail
5	+5V	Power						5	+5V	Power			+5V Power Rail
6	GND	Power						6	GND	Power			Ground
7	GND	Power						7	GND	Power			Ground
8	VIN	Power						8	VIN	Power			Voltage Input
9	A0	GPIO	In	yes	Reset / Abort	C	0	9	A0	GPIO ?	In	yes	Reset / Abort
10	A1	GPIO	In	yes	Feed Hold	C	1	10	A1	GPIO ?	In	yes	Feed Hold
11	A2	GPIO	In	yes	Cycle Start / Resume	C	2	11	A2	GPIO ?	In	yes	Cycle Start / Resume
12	A3	GPIO	Out		Coolant Enable	C	3	12	A3	GPIO ?	Out		Coolant Enable
13	A4 / SDA	Analog			not used (reserved)	C	4	13	A4	Analog			not used (reserved)
14	A5 / SCL	Analog			not used (reserved)	C	5	14	A5	Analog			not used (reserved)

CPU Pin (Pxx)
201
14
0
1
2
101
100

JDIGITAL

UNO R3									UNO R4				
Pin	**Function**	**Type**	**Direction**	**Pull-Up**	**Description for GRBL**	**CPU Channel**	**Bit**	**Interrupt on Bit change**	**Pin**	**Function**	**Type**	**Direction**	**Pull-Up**
1	D0	Digital / GPIO				D	0		1	D0 / TX0	Digital		
2	D1	Digital / GPIO				D	1		2	D1 / TX0	Digital		
3	D2	Digital / GPIO	Out		Step Pulse X-Axis	D	2		3	D2	Digital	Out	
4	D3	Digital / GPIO	Out		Step Pulse Y-Axis	D	3		4	D3	Digital	Out	
5	D4	Digital / GPIO	Out		Step Pulse Z-Axis	D	4		5	D4	Digital	Out	
6	D5	Digital / GPIO	Out		Direction Pulse X-Axis	D	5		6	D5	Digital	Out	
7	D6	Digital / GPIO	Out		Direction Pulse Y-Axis	D	6		7	D6	Digital	Out	
8	D7	Digital / GPIO	Out		Direction Pulse Z-Axis	D	7		8	D7	Digital	Out	
9	D8	Digital / GPIO	Out		Stepper enable/Disable	B	0		9	D8	Digital	Out	
10	D9	Digital / GPIO	In	yes	Limit Pulse X-Axis	B	1	yes	10	D9	Digital	In	yes
11	SS	Digital	In	yes	Limit Pulse Y-Axis	B	2	yes	11	D10 / CS / CANTX0	Digital	In	yes
12	MOSI	Digital	See below : Spindle Control						12	D11 / COPI	Digital	In	yes
13	MISO	Digital							13	D12 / CIPO	Digital	Out	
14	SCK	Digital							14	D13 / SCK / CANRX0	Digital	Out	
15	GND	Power							15	GND	Power		
16	AREF	Digital							16	AREF	Digital		
17	A4 / SD4	Digital				C	4		17	SDA	Digital		
18	A5 / SD5	Digital				C	5		18	SCL	Digital		

Variable Spindle					
			B	3	
In	yes	Limit Pulse Z-Axis	B	4	
Out		Spindle Direction	B	5	

Normal Spindle (in config.h #define VARIABLE_SPINDLE is commented out)						
To be checked	In	yes	Limit Pulse Z-Axis	B	3	yes
	Out		Spindle Enable	B	4	
	Out		Spindle Enable	B	5	

Description for GRBL	CPU Pin (Pxx)	Interrupt on Bit change
	301	
	302	
Step Pulse X-Axis	104	
Step Pulse Y-Axis	105	
Step Pulse Z-Axis	106	
Direction Pulse X-Axis	107	
Direction Pulse Y-Axis	111	
Direction Pulse Z-Axis	112	
Stepper enable/Disable	304	
Limit Pulse X-Axis	303	
Limit Pulse Y-Axis	103	
Limit Pulse Z-Axis	411	
Spindle Enable	410	
Spindle Direction	102	
	10	
	101	
	100	

LEDs

UNO R3			UNO R4	
Function	**CPU Channel**	**Bit**	**Function**	**CPU Pin (Pxx)**
Built In	B	5	Built In	102
TX	ATMEGA16U2-MU(R) D	5	TX	109
RX	ATMEGA16U2-MU(R) D	4	RX	GPIO 43 (ESP32-S3)