

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|------------------------------|---------------------|-------------------------|-------------------------|------------------------------|---------------|------------------|------------------|
| PeriCfg0 | FBDiv_skip | clkTreeDisable | CLKSel | disVCO | disSER | disEOM | disDES | disCLK |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg1 | PLL_I | | | | PLL_BiasGen | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg2 | PLL_R | | | PLL_P | | PLL_P | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg3 | VRefGen | - | ENABLEPLL | PLL_vcoRailMode | PLL_vcoDAC | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg4 | TS_PD | PS_ForceDown | PS_Enable | PS_CapRst | PS_CPCurrent | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg5 | PS_PhaseAdj | | | | PS_PhaseAdj | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg6 | RefStrSel | | | | RefStrSel | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg7 | GRO_TOARST_N | GRO_Start | CLK40_SetCM | CLK40_InvData | CLK40_Equ | CLK40_EnTer | CLK40_EnRx | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| PeriCfg8 | GRO_TOA_Latch | GRO_TOA_CK | CLK1280_SetCM | CLK1280_InvData | CLK1280_Equ | CLK1280_EnTer | CLK1280_EnRx | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| PeriCfg9 | GRO_TOT_CK_Latch | GRO_TOTRST_N | FC_SetCM | FC_InvData | FC_Equ | FC_EnTer | FC_EnRx | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| PeriCfg10 | BCIDOffset[7:0] | | | | BCIDOffset[7:0] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg11 | emptySlotBCID[3:0] | | | | BCIDOffset[11:8] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg12 | emptySlotBCID[11:4] | | | | emptySlotBCID[11:4] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg13 | asyPLLReset | asyLinkReset | asyAlignFastcommand | readoutClockDelayPixel | | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg14 | asyResetGlobalRead-out | asyResetFastcommand | asyResetChargeInj | readoutClockWidthPixel | | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg15 | - | asyStartCalibration | asyResetLockDetect | readoutClockDelayGlobal | | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg16 | LTx_AmplSel | | readoutClockWidthGlobal | | readoutClockWidthGlobal | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg17 | RTx_AmplSel | | | chargeInjectionDelay | | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg18 | disLTx | onChipL1AConf | fcDataDelayEn | fcClkDelayEn | fcSelfAlignEn | softBoot | disPowerSequence | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| PeriCfg19 | disRTx | singlePort | serRateRight | serRateLeft | linkResetTestPattern | disScrambler | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg20 | eFuse_TCKHP | | | | triggerGranularity | | | mergeTriggerData |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg21 | - | - | eFuse_Bypass | eFuse_Start | eFuse_Rstn | eFuse_Mode | eFuse_EnClk | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg22 | eFuse_Prog[7:0] | | | | eFuse_Prog[7:0] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg23 | eFuse_Prog[15:8] | | | | eFuse_Prog[15:8] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg24 | eFuse_Prog[23:16] | | | | eFuse_Prog[23:16] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg25 | eFuse_Prog[31:24] | | | | eFuse_Prog[31:24] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg26 | linkResetFixedPattern[7:0] | | | | linkResetFixedPattern[7:0] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg27 | linkResetFixedPattern[15:8] | | | | linkResetFixedPattern[15:8] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg28 | linkResetFixedPattern[23:16] | | | | linkResetFixedPattern[23:16] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg29 | linkResetFixedPattern[31:24] | | | | linkResetFixedPattern[31:24] | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg30 | IfReLockThrCounter | | | | IfLockThrCounter | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PeriCfg31 | - | - | TDCStrobeTest | TDCClockTest | IfUnLockThrCounter | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |