Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PixCfg0	–	RfSel			IBSel		CLSel	
	0	0	0	0	0	0	0	0
PixCfg1	–	–	QInjEn			QSel		
	0	0	0	0	0	0	0	0
PixCfg2	–	–	–	DACDiscri		HysSel		
	0	0	0	0	0	0	0	0
PixCfg3	–	–	–	ScanStart	CLKEn	Bypass	BufEn	RSTn
	0	0	0	0	0	0	0	0
PixCfg4	DAC[7:0]							
	0	0	0	0	0	0	0	**1**
PixCfg5	TH_offset						DAC[9:8]	
	0	0	0	0	0	0	0	0
PixCfg6	enable_TDC	resetn_TDC	autoReset_TDC	testMode_TDC		level_TDC		–
	0	0	0	0	0	0	0	0
PixCfg7	–	–	–	workMode		disTrigPath	disDataReadout	addrOffset
	0	0	0	0	0	0	0	0
PixCfg8	L1ADelay[0]	selfTestOccupancy						
	0	0	0	0	0	0	0	0
PixCfg9	L1ADelay[8:1]							
	0	0	0	0	0	0	0	0
PixCfg10	lowerCal[7:0]							
	0	0	0	0	0	0	0	0
PixCfg11	upperCal[5:0]						lowerCal[9:8]	
	0	0	0	0	0	0	0	0
PixCfg12	lowerTOA[3:0]				upperCal[9:6]			
	0	0	0	0	0	0	0	0
PixCfg13	upperTOA[1:0]		lowerTOA[9:4]					
	0	0	0	0	0	0	0	0
PixCfg14	upperTOA[9:2]							
	0	0	0	0	0	0	0	0
PixCfg15	lowerTOT[7:0]							
	0	0	0	0	0	0	**1**	0
PixCfg16	upperTOT[6:0]							lowerTOT[8]
	0	0	0	0	0	0	0	0
PixCfg17	lowerCalTrig[5:0]						upperTOT[8:7]	
	0	0	0	0	0	0	0	0
PixCfg18	upperCalTrig[3:0]				lowerCalTrig[9:6]			
	0	0	0	0	0	0	0	0
PixCfg19	lowerTOATrig[1:0]		upperCalTrig[9:4]					
	0	0	0	0	0	0	0	**1**
PixCfg20	lowerTOATrig[9:2]							
	0	0	0	0	0	0	0	0
PixCfg21	upperTOATrig[7:0]							
	0	0	0	0	0	0	0	0
PixCfg22	lowerTOTTrig[5:0]						upperTOATrig[9:8]	
	0	0	0	0	0	0	0	0
PixCfg23	upperTOTTrig[4:0]					lowerTOTTrig[8:6]		
	0	0	0	0	0	0	0	0
PixCfg24	–	–	–	–	upperTOTTrig[8:5]			
	0	0	0	0	0	0	0	0
PixCfg25	0	0	0	0	0	0	0	0
PixCfg26	0	0	0	0	0	0	0	0
PixCfg27	0	0	0	0	0	0	0	0
PixCfg28	0	0	0	0	0	0	0	0
PixCfg29	0	0	0	0	0	0	0	0
PixCfg30	0	0	0	0	0	0	0	0
PixCfg31	0	0	0	0	0	0	0	0