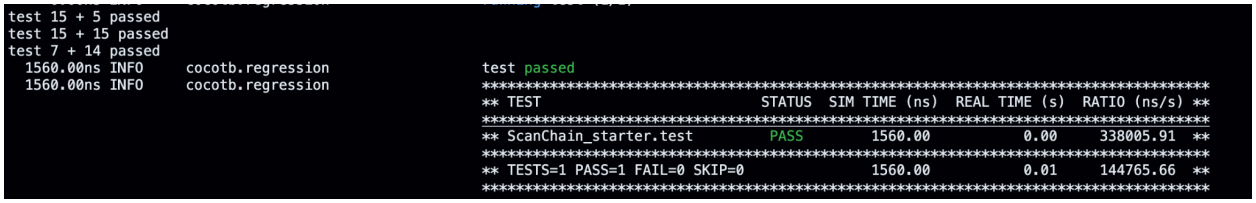
Task #2

Output of testing:



I liked that the use of helper functions made testing a lot easier, as I only had to think of the bit values to input in the order of the inputs/outputs of the adder.log file. I could easily check whether or not my sum was expected.

Task #6

I’m working on the System Verilog for my project, working through some of the modules and making sure the logic is working. I’m also thinking of ways to have access to more memory for my project or some kind of work around because I may need buffers to store my computations in. I’m hoping to finish most of my SV and start creating some very basic test benches.