HSE clock initialization

Code snippet :

```
rcc_set_main_pll(                    // Setup 40 MHz clock
  RCC_PLLCFGR_PLLSRC_HSE,            // PLL clock source
  16,                                // PLL VCO division factor
  80,                                // PLL VCO multiplication factor
  0,                                 // PLL P clk output division factor
  0,                                 // PLL Q clk output division factor
  RCC_PLLCFGR_PLLR_DIV4              // PLL sysclk output division factor
 ); // 16MHz/4 = 4MHz; 4MHz*40 = 160MHz VCO; 160MHz/2 = 80MHz PLL
```

Output result = 40MHz

Code snippet :

```
rcc_set_main_pll(                    // Setup 20 MHz clock
  RCC_PLLCFGR_PLLSRC_HSE,            // PLL clock source
  16,                                // PLL VCO division factor
  40,                                // PLL VCO multiplication factor
  0,                                 // PLL P clk output division factor
  0,                                 // PLL Q clk output division factor
  RCC_PLLCFGR_PLLR_DIV4              // PLL sysclk output division factor
 ); // 16MHz/4 = 4MHz; 4MHz*40 = 160MHz VCO; 160MHz/2 = 80MHz PLL
```

Output result = 20MHz