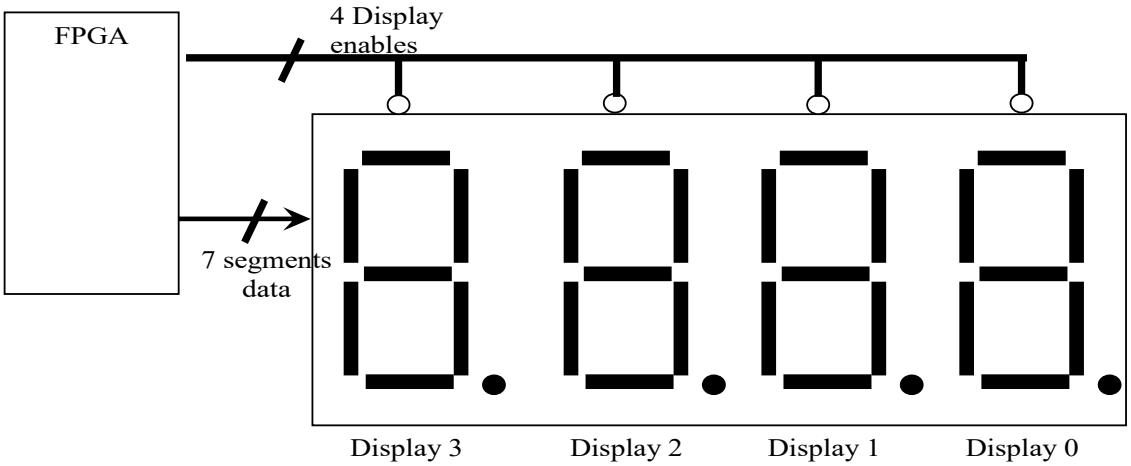
CALIFORNIA STATE POLYTECHNIC UNIVERSITY, POMONA
COLLEGE OF ENGINEERING

ECE 2300L Fall 2019 **Felix Pinai**

Lab11: Digital Clock

Objective:

Design, build, and test a digital clock module, DigitalClock, using FPGA



Background:

The human eye has a property known as Persistence of Vision **(POV),** which causes it to hold an image briefly. The brighter the image, the longer it holds in our eyes. The feature of POV can be used to time-multiplex a display by rapidly cycling through each of the four 7-segment displays on your board. A 400Hz clock is suggested to be used in this experiment. Your circuit will need to display the minute (two digits) and second (two digits). For example, "0955" means 9 minutes and 55 seconds.

Block Diagram

Refer to figure 11.1.

You will need to build the following blocks:

1) 400 Hz clock generator that divides down the 100 MHz clock input down to 400 Hz.

2) 1Hz clock generator that further divides down the 400 Hz clock input down to 1Hz.

3) A '0-to-9 Counter' block that will count from 0 to 9. The clock input is the 1Hz clock. The counter will only count up when the signal 'CLK_EN' is 1 and when the 1Hz clock is active. This block will be used twice.

4) A '0-to-5 Counter' block that will count from 0 to 5. It has the same 1Hz input as clock as well as the 'CLK_EN' control pin. This block will be used twice.

5) A Clock Enable Generator (CLKEN_GEN) block will be used to enable the clock input to either the '0-to-9 Counter' block or the '0-to-5 Counter' block. It has three inputs: 'EN1','EN2' and 'LD'. It has only 1 output called 'CLK_EN'. When both 'EN1' and 'EN2' pins are '1', then 'CLK_EN' is set to '1'. Also, when the 'LD' pin is '1', 'CLK_EN' is also set to '1'. This block will decide when the 1Hz clock is allowed to clock the counter.

6) A '59-SECOND DETECTOR' block will check when the second display portion is equal to 59. When this is true, then this block will provide a signal to enable the clock to be generated to the minute display portion

7) A '4-to-1 MUX' block that multiplexes the 4-digit outputs from each second and minute blocks.

8) A '2-bit Counter' block that will provide the input selections to the '4-to-1 MUX' above.

9) A '2-to-4 Decoder' that will provide the enabling of each of the 4 digits of the 7-segment display unit. **Each enable pin is active low.**

PRELAB:

Before you can start working on the design shown on Figure 11.1, it is best to build and test a couple of small circuits involved in the design.

Part 1) Design of the '0-9 Counter'

Use the last part of the previous lab where the 4-bit counter was designed (assuming a behavior design was used):

a. Use the following basic 4-bit counter (using D flip-flops):

```
module counter_4bit (clk, Q);
input clk;
output reg [3:0] Q;

always @(posedge clk)
Q = Q + 1;

endmodule
```

b. Modify that design so that the counter only goes up to 9 instead of F. Add an 'if' statement before the line 'Q=Q+1' to check for the count Q. If that count is 9, then force that count to 0. Else, it should keep counting up.

c. In addition, modify that design such that the counter now has an additional input called 'CLK_EN' and an extra output called 'CARRY_OUT'. See Figure 11.2.

When ‘CLK_EN’ is 1, then every time the input clock ‘CLK’ transitions from 0 to 1 (positive edge), the count is incremented by 1. If this pin is 0, then the count remains unchanged no matter the clock.

The ‘CARRY_OUT’ output is set to 1 on the positive transition of the clock ‘CLK’ and when the count is equal to 9. This ‘CARRY_OUT’ signal must be a combinational decode of the count being equal to 9 meaning if the count equals 9, then the ‘CARRY_OUT’ is 1. Use the ‘assign’ statement to generate this output.

Replace the 4-bit counter on the previous lab (that counts from 0 to F) so that the count only goes from 0 to 9. Use a switch for ‘CLK_EN’. When the switch is off, the counter should not count and vice versa. Use a LED for the ‘CARRY_OUT’.

Part 2) Design of the ‘0-5’ Counter

Change the design on part 1) such that the counter is now a 0-to-5 counter still with the ‘CLK_EN’ input but it no longer requires the ‘CARRY_OUT’ output. See Figure 11.3.

Part 3) Design of the ‘4-to-1 MUX’

a. You need to build a 4-to-1 multiplexer circuit whereas there are two selector bits called SEL0 and SEL1 used to choose one input out of 4 possible choices. See Figure 11.4A. The inputs are called IN0, IN1, IN2, and IN3. The logic state of the select input is then output to the pin called MUX_OUT. Connect the IN0, IN1, IN2, and IN3 each to a slide switch. The same applies to the SEL0 and SEL1 pins. The signal MUX_OUT should be a LED. Set the IN input switches to a desired set of positions and then use the SEL switches to select which IN input to appear on the LED.

b. When you are done verifying the design, change it so that each input (IN0, IN1, IN2, IN3) is now a matrix of 4 elements, e.g. [3:0] IN0, [3:0] IN1, etc. Do the same for MUX_OUT which should be then [3:0] MUX_OUT. The multiplexer will switch between four sets of four inputs. See Figure 11.4B. You don’t need to verify this modification because it would take a lot of switches to test the implementation. Simply just change the definition of the module.

LAB:

Final Implementation

You need to build now the circuit shown on Figure 11.1. There are three switches used on this design. Each switch, when pressed, will increment the corresponding second or minute display in order to set the value of the digital clock. Here are some helps on the different blocks:

- Modify the ‘SlowClkGen’ module from last week’s lab to divide the input 100 MHz clock in order to generate a 400 Hz clock. Just change the divisor value in order to get the clock to be 400 Hz instead of the original value of 1 Hz. Calculate the ratio to change from 100 Mhz to 400 Hz and take half of that ratio. Replace the original number with the

new calculated number. This should create the '400Hz CLOCK MODULE' block (1) (the block number is marked inside a small square block of each block).

- Do the same to generate the '1HZ CLOCK MODULE' block (2) by taking the CLK_400HZ clock and divide it down to 1Hz. The output clock CLK_1Hz must be also routed to an LED to show the clock pulse.

- The '0-to-9 counter' in Part 1) above can be used now as each (3) block on the general block diagram.

- The 0-to-5 counter in Part 2) is the (4) block on the design.

- The 'CLKEN_GEN' block (5) is a simple combination of the three inputs 'EN', 'EN1 and 'LD' based on the description provided above. Simply use an 'assign' statement to generate the combinational logic output for this signal.

- The '59-SECOND DETECTOR' block (6) is also a combination block that sets the output signal 'EQ59' when the inputs DATA1 [3:0] and DATA0 [3:0] are respectively a '5' and a '9'. Just do a logic comparison and the output should be 1 when the values match to what they should be. Use of the 'assign' statement is highly recommended.

- The '4-to-1 multiplexer' on the Prelab part 3) is now block (7) on the general block diagram.

- Block (8) shows a 2-bit counter that can be easily implemented by changing the 4-bit counter used on the previous lab down to a 2-bit counter.

- The '2-to-4 decoder' block (9) can be derived from the decoder designed on the first lab. The outputs are the 'AN[3:0]' used to enable each individual 7-segment. Make sure that the output pins are active low and not active high. If the Nexys-4 board is used, add four more outputs for AN4, AN5, AN6, and AN7 and force them to be all '1' so that the corresponding 7-segment is not turned on.

The main design should **be only a list of instance calls of the various modules mentioned above**. There is a total of 15 blocks on the diagram. There should be 15 instance calls with some of them being repeated calls of a same module. Make sure to place the commented directive above the instance calls to help you through the design.

The design should work as a digital clock starting with 0 minute and 0 second. The clock counts up and, if left alone, the display will show the count to be up to 59:59 and then it will wrap around to 00:00. Each switch, when pressed, will advance the associated digit (ten-second, minute, and ten-minute). The switches are used to setup the initial time for the clock. For convenience, choose the location of each switch such that it is right under the corresponding 7-segment display in order to indicate which display the switch is intended to modify.