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Road vehicles — Controller area network (CAN) —

Part 2: High-speed medium access unit

Véhicules routiers — Gestionnaire de réseau de communication (CAN) —

Partie 2: Unité d'accès au support à haute vitesse

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Foreword

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ISO 11898-2 was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

ISO 11898 consists of the following parts, under the general title *Road vehicles — Controller area network (CAN)*:

— *Part 1: Data link layer and physical signalling*

— *Part 2: High-speed medium access unit*

— *Part 3: Low-speed fault tolerant physical medium attachment*

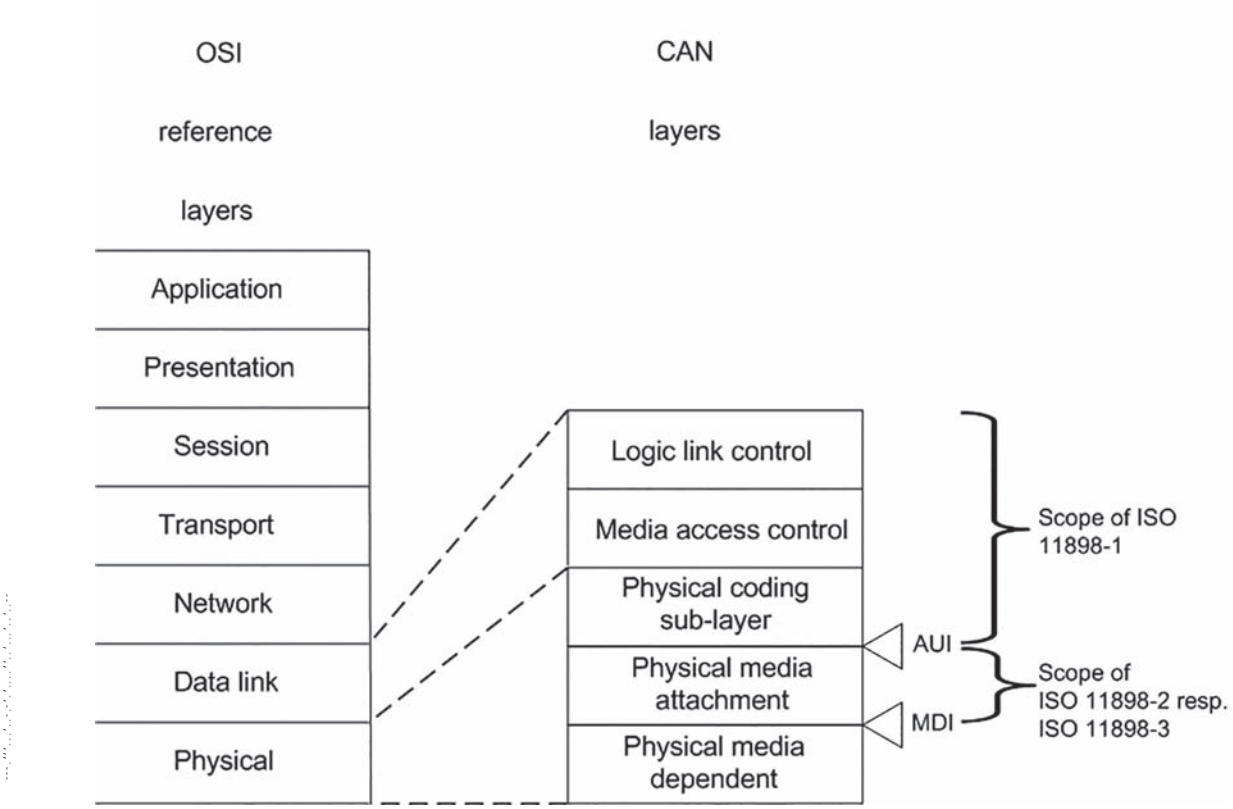
— *Part 4: Time-triggered communication*

Introduction

ISO 11898 was first published as one document in 1993. It covered the CAN data link layer as well as the high-speed physical layer. In the reviewed and restructured ISO 11898- series parts 1 and 4 defined the CAN protocol and time-triggered CAN (TTCAN) while the parts 2, 5 and 6 defined the high-speed physical layer, and part 3 defined the low-speed fault tolerant physical layer.

ISO 11898-2:2003, ISO 11898-5:2007 and ISO 11898-6:2013 have been withdrawn and replaced by this version of ISO 11898-2.

Figure 1 shows the relation of the OSI (Open System Interconnection) layers and its sub-layers to the ISO 11898 part 1 and part 2 as well as part 3.



Key

AUI	attachment unit interface
MDI	media dependant interface
OSI	open system interconnection

Figure 1 — Overview of ISO 11898 specification series

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Road vehicles — Controller area network (CAN) —

Part 2:
High-speed medium access unit

1 Scope

This part of ISO 11898 specifies the high-speed physical media attachment (HS-PMA) of the controller area network (CAN) a serial communication protocol that supports distributed real-time control and multiplexing for use within road vehicles. This includes HS-PMAs without and with low-power capability as well as with selective wake-up functionality. The physical media dependant sub-layer is not in the scope of this part.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this part and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7498-1:1994, *Information technology — Open Systems Interconnection — Basic Reference Model: The Basic Model — Part 1*

ISO 11898-1:2015, *Road vehicles — Controller area network (CAN) — Part 1: Data link layer and physical signalling*

ISO 16845-2:2014, *Road vehicles — Controller area network (CAN) conformance test plan — Part 2: High-speed medium access unit with selective wake-up functionality*

3 Terms and definitions

For the purpose of this document, the terms and definitions given in ISO 11898-1 and the following apply. See figure A.1 in Annex A for a visualization of the definitions.

3.1
attachment unit interface (AUI)
The attachment unit interface is the interface between the PCS that is specified in part 1 of ISO 11898 and the PMA that is specified in this of ISO 11898.

3.2
ground (GND)
electrical signal ground

3.3
medium attachment unit (MAU)
unit that comprises the physical media attachment and the media dependent interface

3.4
media dependent interface (MDI)
interface that ensures proper signal transfer between the media and the physical media attachment

3.5
physical coding sublayer (PCS)
sub-layer that performing bit encoding/decoding and synchronization

3.6
physical media attachment (PMA)
sub-layer that converts physical signals into logical signals and vice versa

3.7
transceiver
implementation that comprises one or more physical media attachments

4 Symbols and abbreviated terms

For the purpose of this part, the symbols and abbreviated terms given in ISO 11898-1 and the following apply. Some of these abbreviations are also defined in ISO 11898-1. If the definition of the term here is different from the definition in ISO 11898-1, this definition applies.

AUI	attachment unit interface
EMC	electro-magnetic compatibility
ESD	electro static discharge
GND	ground
HS-PMA	high-speed PMA
MAU	medium attachment unit
MDI	media dependent interface
PCS	Physical coding sub-layer
PMA	physical media attachment
PMD	physical media dependent
WUF	wake-up frame
WUP	wake-up pattern

5 Functional description of the HS-PMA

5.1 General

The HS-PMA comprises one transmitter and one receiving entity. It shall be able to bias the connected physical media – an electric two-wire cable – relative to a common ground. The transmitter entity shall drive a differential voltage between the CAN_H and CAN_L signals to signal a logical 0 (dominant) respectively a logical 1 (recessive) to be received by other nodes connected to the very same media. These two-signals are the interface to the physical media dependent sub-layer.

The HS-PMA shall provide an AUI to the physical coding sub-layer as specified in ISO 11898-1. It comprises the TXD and RXD signals as well as the GND signal. The TXD signal receives from the physical coding sub-layer the bit-stream to be transmitted on the MDI. The RXD signal transmits to the physical coding sub-layer the bit-stream received from the MDI.

Implementations that comprise one or more HS-PMAs shall at least support the “normal” mode of operation. Optionally, a “low-power mode” may be implemented.

Some of the items specified in the following depend on the operation mode of the (part of the) implementation, in which the HS-PMA is included.

Table 1 shows the possible combinations of HS-PMA operational modes and expected behaviour.

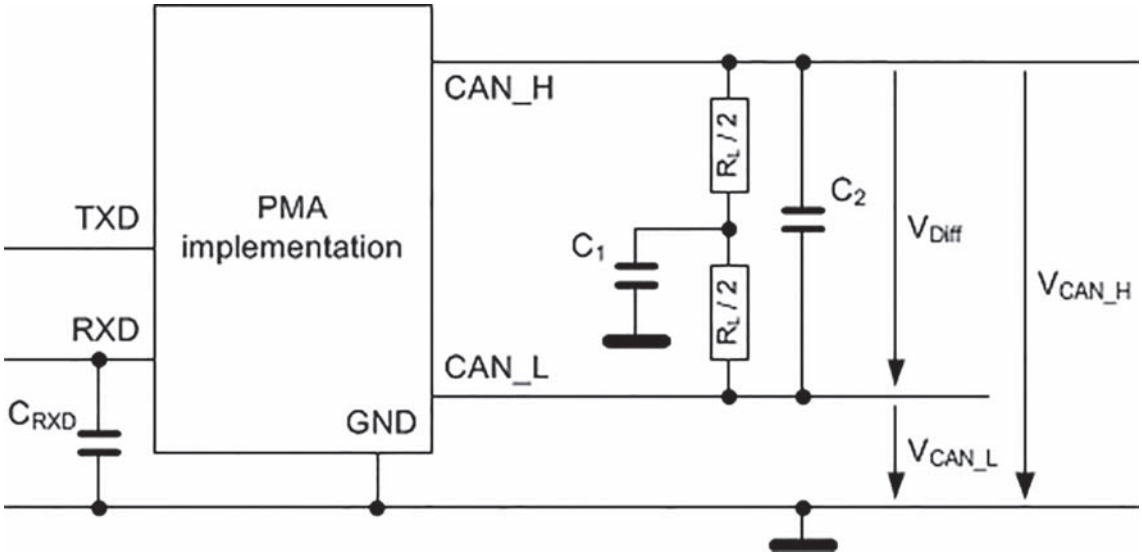
Table 1 — HS-PMA operating modes and expected behaviour

Operating mode	Bus biasing behaviour	Transmitter behaviour
Normal	Bus biasing active	Dominant or recessive[a]
Low-power	Bus biasing active or inactive [a]	Recessive
[a] Depends on input conditions as described in this document		

All parameters given in this clause of this part shall be fulfilled throughout the operating temperature range and supply voltage range (if not explicitly specified for unpowered) as specified individually for every HS-PMA implementation.

5.2 HS-PMA test circuit

The outputs of the HS-PMA implementation to the CAN signals are called CAN_H and CAN_L, TXD is the transmit data input and RXD the receive data output. Figure 2 shows the external circuit that defines the measurement conditions for all required voltage and current parameters. R_L represents the effective resistive load (bus load) for a HS-PMA implementation, when used in a network and C_1 represents an optional split-termination capacitor. The values of R_L and C_1 vary for different parameters that the PMA implementation needs to meet and are given as condition in the following tables.



Key

V_{Diff}: Differential voltage between CAN_H and CAN_L wires

V_{CAN_H}: Single ended voltage on CAN_H wire

V_{CAN_L}: Single ended voltage on CAN_L wire

C_{RXD}: Capacitive load on RXD

Figure 2 — HS-PMA test circuit

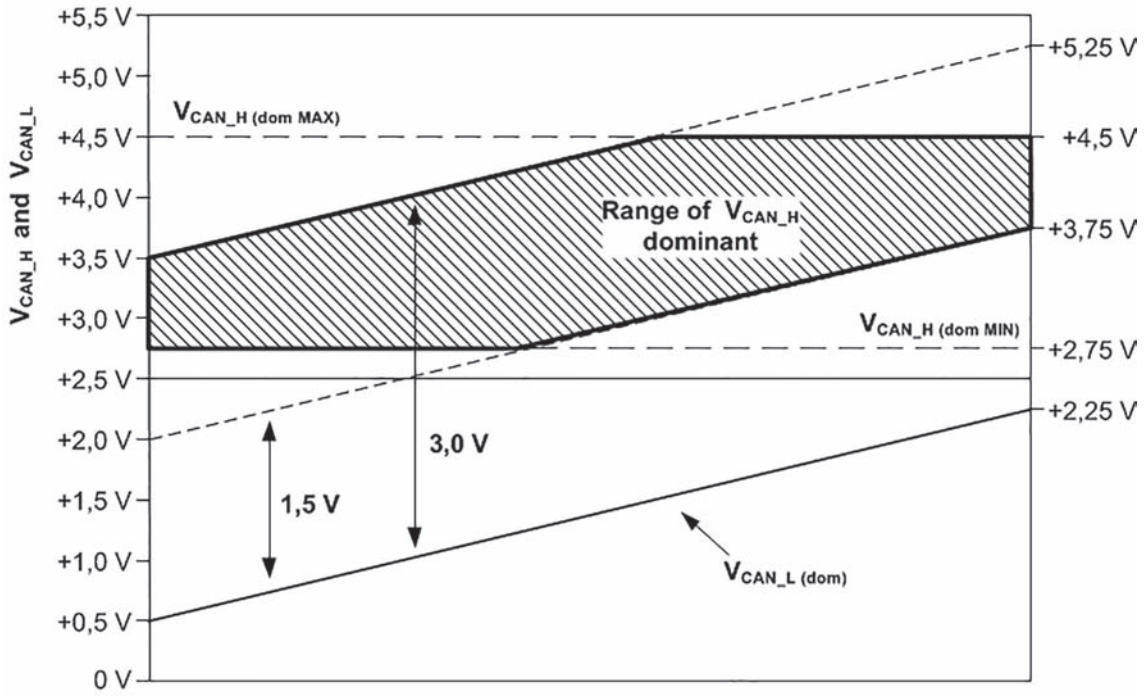
5.3 Transmitter characteristics

This section specifies the transmitter characteristics of a single HS-PMA implementation under the conditions as depicted in Figure 2; so no other HS-PMA implementations connected to the media. The behaviour of a HS-PMA implementation connected to other HS-PMAs is out of scope in this sub-section. Refer to section A.2 for consideration when multiple HS-PMAs are connected to the same media. The voltages and currents that are required on the CAN_L and CAN_H signals are specified in Table 2 to Table 6. Table 2 specifies the output characteristics during dominant state.

Figure 3 illustrates the voltage range for the dominant state.

Table 2 — HS-PMA dominant output characteristics

Parameter	Notation	Value			Condition
		Min	Nom	Max	
		V	V	V	
Single ended voltage on CAN_H	V_{CAN_H}	+2,75	+3,5	+4,5	R_L = 50 … 65
Single ended voltage on CAN_L	V_{CAN_L}	+0,5	+1,5	+2,25	R_L = 50 … 65
Differential voltage on normal bus load	V_{Diff}	+1,5	+2,0	+3,0	R_L = 50 … 65
Differential voltage on effective resistance during arbitration	V_{Diff}	+1,5	Not defined	+5,0	R_L = 2240
Optional: Differential voltage on extended bus load range	V_{Diff}	+1,4	+2,0	+3,3	R_L = 45 … 70
All requirements in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential voltage (see Figure 3). Measurement setup according to Figure 2 (only one HS-PMA present) R_L: see "Condition" - column above C_1 = 0 pF (not present) C_2 = 0 pF (not present) C_{RXD} = 0 pF (not present)					



Key

V_{Diff}: differential voltage between CAN_H and CAN_L wires

V_{CAN_H}: single ended voltage on CAN_H wire

V_{CAN_L}: single ended voltage on CAN_L wire

Figure 3 — Voltage range of V_{CAN_H} during dominant state of CAN node, when V_{CAN_L} varies from minimum to maximum voltage level (50 Ω...65 Ω bus load condition)

In order to achieve a level of RF emission that is acceptably low, the transmitter shall meet the driver signal symmetry as required by Table 3.

Table 3 — HS-PMA driver symmetry

Parameter	Notation	Value		
		Min	Nom	Max
Driver symmetry[a]	v_{SYM}	+0,9	+1,0	+1,1
a $V_{SYM} = (V_{CAN\_H} + V_{CAN\_L}) / V_{CC}$, with V_{CC} being the supply voltage of the transmitter. V_{SYM} shall be observed during dominant and recessive state and also during the transition from dominant to recessive and vice versa, while TXD is stimulated by a square wave signal with a frequency that corresponds to the highest bit rate for which the HS-PMA implementation is intended, however, at most 1 MHz (2 Mbit/s) (HS-PMA in normal mode). Measurement setup according to Figure 2 R_L = 60 (tolerance ≤ ±1 %) C_1 = 4,7 nF (tolerance ≤ ±5 %) C_2 = 0 pF (not present) C_{RXD} = 0 pF (not present)				

The maximum output current of the transmitter shall be limited according to Table 4.

Table 4 — Maximum HS-PMA driver output current

Parameter	Notation	Value		Condition
		Min mA	Max mA	
Absolute current on CAN_H	I_{CAN_H}	not defined	115	-3 V ≤ V_{CAN_H} ≤ +18 V
Absolute current on CAN_L	I_{CAN_L}	not defined	115	-3 V ≤ V_{CAN_L} ≤ +18 V
Measurement setup according to Figure 2 with either V_{CAN_H} or V_{CAN_L} enforced to voltage levels as mentioned in the conditions by connection to an external voltage source, while the HS-PMA is driving the output dominant. The absolute maximum value does not care about the direction in that the current flows. $R_L > 10^{10}$ (not present) C_1 = 0 pF (not present) C_2 = 0 pF (not present) C_{RXD} = 0 pF (not present) NOTE It is expected that the implementation does not stop driving its output dominant when the voltages on CAN_H and CAN_L are outside the limits mentioned in Table 8.				

Table 5 specifies the recessive output characteristics, when bus biasing is active.

Table 5 — HS-PMA recessive output characteristics, bus biasing active

Parameter	Notation	Value		
		Min V	Nom V	Max V
Single ended output voltage on CAN_H	V_{CAN_H}	+2,0	+2,5	+3,0
Single ended output voltage on CAN_L	V_{CAN_L}	+2,0	+2,5	+3,0
Differential output voltage	V_{Diff}	-0,5	0	+0,05

Table 5 *(continued)*

Parameter	Notation	Value		
		Min V	Nom V	Max V
All requirements in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential output voltage. Measurement setup according to Figure 2 $R_L > 10^{10}$ (not present) $C_1 = 0$ pF (not present) $C_2 = 0$ pF (not present) $C_{RXD} = 0$ pF (not present)				

Table 6 specifies the recessive output characteristics, when bus biasing is inactive.

Table 6 — HS-PMA recessive output characteristics, bus biasing inactive

Parameter	Notation	Value		
		Min V	Nom V	Max V
Single ended output voltage on CAN_H	V_{CAN_H}	-0,1	0	+0,1
Single ended output voltage on CAN_L	V_{CAN_L}	-0,1	0	+0,1
Differential output voltage	V_{Diff}	-0,2	0	+0,2
See 5.10, Bus biasing, to determine when bias shall be inactive. Measurement setup according to Figure 2 $R_L > 10^{10}$ (not present) $C_1 = 0$ pF (not present) $C_2 = 0$ pF (not present) $C_{RXD} = 0$ pF (not present)				

The implementation of a HS-PMA may limit the duration of dominant transmission in order not to prevent other CAN nodes from communication when the TXD input is permanently asserted. The HS-PMA implementation should implement a timeout within the limits specified in Table 7.

Table 7 — Optional HS-PMA transmit dominant timeout

Parameter	Notation	Value	
		Min ms	Max ms
Transmit dominant timeout, long	t_{dom}	0,8	10,0
Transmit dominant timeout, short	t_{dom}	0,3	5,0

NOTE There is a relation between the t_{dom} minimum value and the minimum bit rate. A t_{dom} minimum value of 0,8 ms accommodates 17 consecutive dominant bits at bit rates greater than or equal to 21,6 kbit/s and 36 consecutive dominant bits at bit rates greater than or equal to 45,8 kbit/s. The value 17 reflects PMA implementation attempts to send a dominant bit and every time sees a recessive level at the receive data input. The value 36 reflects six consecutive error frames when there is a bit error in the last bit of the first five attempts.

5.4 Receiver characteristics

The receiver uses the transmitter output signals CAN_H and CAN_L as differential input. Figure 2 shows the definition of the voltages at the connections of the HS-PMA's implementation.

When the HS-PMA implementation is in its low-power mode and bus biasing is active, then the recessive and dominant state differential input voltage ranges according to Table 8 apply.

Table 8 — HS-PMA static receiver input characteristics, bus biasing active

Parameter	Notation	Value		Condition
		Min V	Max V	
Recessive state differential input voltage range[a]	V_{Diff}	-3,0	+0,5	-12,0 V ≤ V_{CAN_L} ≤ +12,0 V -12,0 V ≤ V_{CAN_H} ≤ +12,0 V
Dominant state differential input voltage range	V_{Diff}	+0,9	+8,0	-12,0 V ≤ V_{CAN_L} ≤ +12,0 V -12,0 V ≤ V_{CAN_H} ≤ +12,0 V
Measurement setup according Figure 2. V_{CAN_L}, V_{CAN_H} according to Table 9. R_L > 10^{10} (not present) C_1 = 0 pF (not present) C_2 = 0 pF (not present) C_{RXD} = 0 pF (not present) Note: A negative differential voltage may temporarily occur when the HS-PMA is connected to a media in that common mode chokes and/or unterminated stubs are present. The maximum positive differential voltage may temporarily occur when the HS-PMA is connected to a media while more than one HS-PMA is sending dominant and concurrently a ground shift between the sending HS-PMAs is present.				

When the HS-PMA implementation is in its low-power mode and bus biasing is inactive, then the recessive e and dominant state differential input voltage ranges according to Table 9 apply.

Table 9 — HS-PMA static receiver input characteristics, bus biasing inactive

Parameter	Notation	Value		Condition
		Min V	Max V	
Recessive state differential input voltage range	V_{Diff}	-3,0	+0,4	-12,0 V ≤ V_{CAN_L} ≤ +12,0 V -12,0 V ≤ V_{CAN_H} ≤ +12,0 V
Dominant state differential input voltage range	V_{Diff}	+1,15	+8,0	-12,0 V ≤ V_{CAN_L} ≤ +12,0 V -12,0 V ≤ V_{CAN_H} ≤ +12,0 V
Measurement setup according Figure 2 R_L >10^{10} (not present) C_1 = 0 pF (not present) C_2 = 0 pF (not present) C_{RXD} = 0 pF (not present) Note: A negative differential voltage may temporarily occur when the HS-PMA is connected to a media in that common mode chokes and/or unterminated stubs are present. The maximum positive differential voltage may temporarily occur when the HS-PMA is connected to a media while more than one HS-PMA is sending dominant and concurrently a ground shift between the sending HS-PMAs is present.				

5.5 Receiver input resistance

The implementation of a HS-PMA shall have an input resistance according to Table 10. Furthermore the internal resistance shall meet the requirement given in Table 11. Figure 4 shows an equivalent circuit diagram:

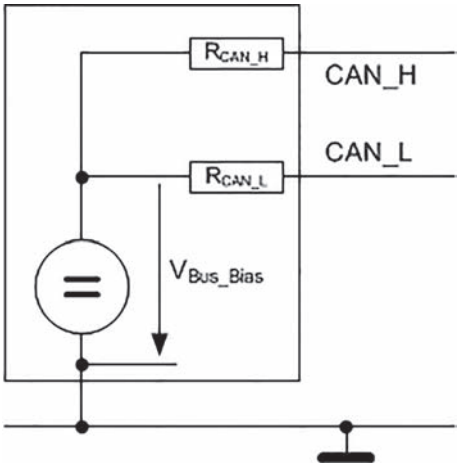


Figure 4 — Illustration of HS-PMA internal differential input resistance

Table 10 — HS-PMA receiver input resistance

Parameter	Notation	Value	
		Min k	Max k
Differential internal resistance	R_{Diff}	12	100
Single ended internal resistance	R_{CAN_H}, R_{CAN_L}	6	50
$R_{Diff} = R_{CAN\_H} + R_{CAN\_L}$			

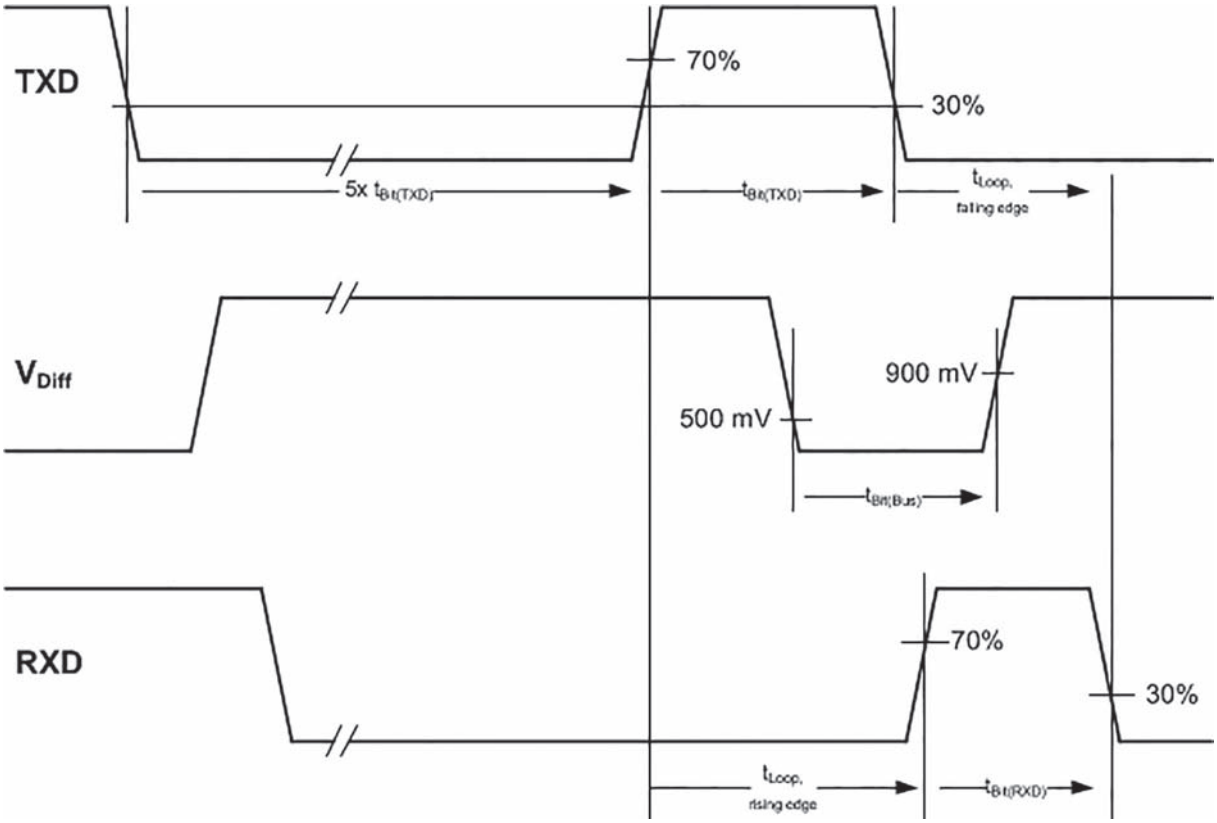
Table 11 — HS-PMA receiver input resistance matching

Parameter	Notation	Value	
		Min	Max
Matching [a] of internal resistance	m_R	-0,03	+0,03
[a] The matching shall be calculated as $m_R = 2 \times (R_{CAN\_H} - R_{CAN\_L}) / (R_{CAN\_H} + R_{CAN\_L})$			

5.6 Transmitter and receiver timing behaviour

The timing is defined under consideration of the test circuit that is shown in Figure 2. The parameters are given in Table 12, Table 13 and Table 14 shall be measured at the RXD output and TXD input of the HS-PMA implementation as well as on the differential voltage between CAN_H and CAN_L.

Figure 5 shows how to measure the timing in the signal traces.



Key

$t_{Bit(TXD)}$ = 1 000 ns if the implementation of the HSPMA supports bit rates of up to 1 Mbit/s

$t_{Bit(TXD)}$ = 500 ns if the implementation of the HS PMA supports bit rates of up to 2 Mbit/s

$t_{Bit(TXD)}$ = 200 ns if the implementation of the HS PMA supports bit rates of up to 5 Mbit/s

Figure 5 — HS-PMA implementation timing diagram

Table 12 — HS-PMA implementation loop delay requirement

Parameter	Notation	Value	
		Min ns	Max ns
Loop delay[a]	t_{Loop}	not defined	255
[a] Time span from signal edge on TXD input to next signal edge with same polarity on RXD output, the maximum of delay of both signal edges is to be considered. Measurement setup according to Figure 2: R_L = 60 Ω (tolerance ≤ ±1 %) C_1 = 0 pF (not present) C_2 = 100 pF (tolerance ≤ ±1 %) C_{RXD} = 15 pF (tolerance ≤ ±1 %) Measurement according to Figure 5: The input signal on TXD shall have rise- and fall times (10 % / 90 %) of less than 10 ns. Note: Limits for $t_{Bit(Bus)}$ and $t_{Bit(RXD)}$ are not defined for intended use with bit rates up to 1 Mbit/s.			

Table 13 — Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s and up to 2 Mbit/s

Parameter	Notation	Value	
		Min ns	Max ns
Transmitted recessive bit width @ 2 Mbit/s	$t_{Bit(Bus)}$	435	530
Received recessive bit width @ 2 Mbit/s	$t_{Bit(RXD)}$	400	550
Receiver timing symmetry @ 2 Mbit/s	Δt_{Rec}[a]	-65	+40
All requirements in this table apply concurrently. Therefore, not all combinations of $t_{Bit(Bus)}$ and Δt_{Rec} compliant with $t_{Bit(RXD)}$. [a] $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ Measurement setup according to Figure 2: R_L = 60 Ω (tolerance ≤ ±1 %) C_1 = 0 pF (not present) C_2 = 100 pF (tolerance ≤ ±1 %) C_{RXD} = 15 pF (tolerance ≤ ±1 %) Measurement according to Figure 5: The input signal on TXD shall have rise- and fall times (10 % / 90 %) of less than 10 ns. Note: Limits for $t_{Bit(Bus)}$ and $t_{Bit(RXD)}$ are not defined for intended use with bit rates up to 1 Mbit/s.			

Table 14 — Optional HS-PMA implementation data signal timing requirements for use with bit rates above 2 Mbit/s and up to 5 Mbit/s

Parameter	Notation	Value	
		Min ns	Max ns
Transmitted recessive bit width @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	155	210
Received recessive bit width @ 5 Mbit/s	$t_{Bit(RXD)}$	120	220
Receiver timing symmetry, @ 5 Mbit/s	Δt_{Rec}[a]	-45	+15
All requirements in this table apply concurrently. Therefore, not all combinations of $t_{Bit(Bus)}$ and Δt_{Rec} compliant with $t_{Bit(RXD)}$. [a] $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ Measurement setup according to Figure 2: R_L = 60 Ω (tolerance ≤ ±1 %) C_1 = 0 pF (not present) C_2 = 100 pF (tolerance ≤ ±1 %) C_{RXD} = 15 pF (tolerance ≤ ±1 %) Measurement according to Figure 5: The input signal on TXD shall have rise- and fall times (10 % / 90 %) of less than 10 ns. Note: Limits for $t_{Bit(Bus)}$ and $t_{Bit(RXD)}$ are not defined for intended use with bit rates up to 1 Mbit/s.			

5.7 Maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}

Table 15 reflects upper and lower limit static voltages, which may be connected to CAN_H and CAN_L without causing damage; while V_{Diff} stays within in its own maximum rating range.

Table 15 — HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}

Parameter	Notation	Value	
		Min V	Max V
Maximum rating V_{Diff} [a]	V_{Diff}	-5,0	+10,0
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H}, V_{CAN_L}	-27,0	+40,0
Optional: Extended maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H}, V_{CAN_L}	-58,0	+58,0
The maximum rating for V_{Diff} excludes that all combinations of V_{CAN_H} and V_{CAN_L} are compliant to this standard. $V_{Diff} = V_{CAN\_H} - V_{CAN\_L}$, see figure 2. [a] This is required regardless whether general or extended maximum rating for V_{CAN_H} and V_{CAN_L} is fulfilled			

5.8 Maximum leakage currents of CAN_H and CAN_L

An unpowered HS-PMA implementation shall not disturb the communication of other HS-PMAs that are connected to the same media. The required maximum leakage currents are given in Table 17.

Table 16 — HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered

Parameter	Notation	Value	
		Min µA	Max µA
Leakage current on CAN_H, CAN_L	I_{CAN_H}, I_{CAN_L}	-10	+10
V_{CAN_H} = 5 V, V_{CAN_L} = 5 V, all supply inputs are connected to GND. Positive currents are flowing into the implementation.			

5.9 Wake-up from low-power mode

5.9.1 Overview

When an implementation comprising one or more HS-PMAs implements a low-power mode, the HS-PMA shall be able to signal a wake-up event to its implementation. Table 18 lists the required Wake-up mechanism for defined types of HS-PMA implementations.

Table 17 — HS-PMA wake-up implementations

Type of HS-PMA implementation	Required wake-up mechanism
CAN wake-up, implementations without low-power mode	No wake-up
CAN wake-up, implementations with low-power mode but without selective wake-up	Either basic wake-up or wake-up pattern (WUP) wake-up
CAN wake-up, implementations with selective wake-up	Selective wake-up and wake-up pattern (WUP) wake-up

When more than one wake-up mechanism is implemented in a HS-PMA, the wake-up mechanism to be used shall be configurable.

5.9.2 Basic wake-up

Upon receiving once a dominant state for duration of at least t_{Filter}, a wake-up event shall happen.

5.9.3 Wake-up pattern wake-up

Upon receiving two consecutive dominant states each for duration of at least t_{Filter}, separated by a recessive state with a duration of at least t_{Filter}, a wake-up event shall happen. This method follows the description of activating the bus biasing as described in sub clause 5.10.3.

5.9.4 Selective wake-up

5.9.4.1 General

Upon detection of a Wake-up frame (WUF), a wake-up event shall happen. Acceptance of CAN frames in either CBFF or CEFF as a WUF is done by the HS-PMA. The acceptance procedure is described in detail in the following sub-clauses.

After the bias reaction time t_{Bias} has elapsed, the implementation may ignore up to four (or up to eight when bit rate higher than 500 kbit/s) frames in CBFF and CEFF and shall not ignore any following frame in CBFF and CEFF.

In case of erroneous communication, the HS-PMA shall signal a wake-up upon or after an overflow of the internal error counter.

5.9.4.2 Behaviour during transition from normal to low-power mode

If selective wake-up is enabled, decoding of CAN data and remote frames shall also be supported during mode transitions. If the received frame is a valid WUF, the transceiver shall indicate a wake-up.

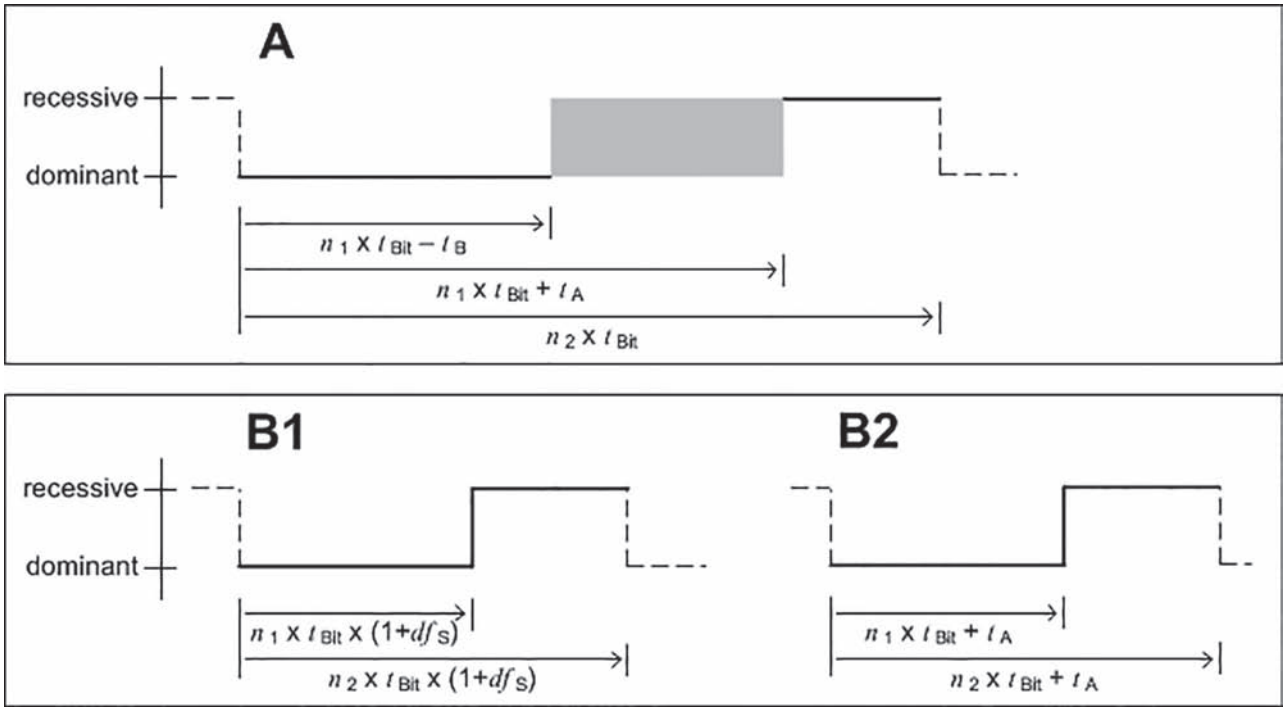
5.9.4.3 Bit decoding

A received Classical CAN frame shall be decoded correctly when the timing of the differential voltage between CAN_H and CAN_L complies with one of the two following types of signals:

— The bit stream consists of multiple instances of the signal shape A (to handle ringing);

— The bit stream can be assembled out of multiple instances of the signal shape B1 and one instance of signal shape B2 (to handle sender clock tolerance and loss of arbitration).

These two types of signals are specified in Figure 6.



Key

n_1 number of consecutive dominant bits {1, 2, 3, 4, 5}

n_2 number of bits between two falling edges {2, 3, …, 10}; n2 > n1

t_A $0 \le t_A \le 55$ % of t_{Bit} (product specific higher maximum values for t_A are allowed)

t_B $0 \le t_B \le 5$ % of t_{Bit} (product specific higher maximum values for t_B are allowed)

t_{Bit} nominal bit time (Note: often used values for t_{Bit} are 2 µs, 4 µs and 8 µs)

df_S transceivers according to this document shall tolerate sender clock frequency deviations up to at least 0,5 %

Figure 6 — Signal shape A and B of V_{Diff} for bit reception

Edges in the time span from "n1 x t_{Bit} – t_B" to "n_1 x t_{Bit} + t_A" of signal shape A shall be ignored and shall not cause decoding errors.

5.9.4.4 Wake-up frame evaluation

If all of the following conditions are met, a valid Classical CAN frame shall be accepted as a valid WUF.

a) The received frame is a Classical CAN data frame when DLC matching (see bullet point c) in this list) is not disabled. The frame may also be a remote frame when DLC matching is disabled.

b) The ID (as defined in 8.4.2.2 in ISO 11898-1) of the received Classical CAN frame is exactly matching a configured ID (in the HS-PMA implementation) in the relevant bit positions. The relevant bit positions are given by an ID-mask (in the HS-PMA implementation). See this mechanism illustrated in 5.9.4.7

c) The DLC (as defined in 8.4.2.4 in ISO 11898-1) of the received Classical CAN data frame is exactly matching a configured DLC. See this mechanism illustrated in sub clause 5.9.4.8. Optionally this DLC matching condition may be disabled by configuration in the HS-PMA implementation.

d) When the DLC is greater than 0 and DLC matching is enabled, the data field (as defined in 8.4.2.5 in ISO 11898-1) of the received frame has at least one bit set in a bit position which corresponds to a set bit in the configured data mask. See this mechanism illustrated in 5.9.4.9.

e) A correct cyclic redundancy check (CRC) has been received, including a recessive CRC delimiter and no error (according to 10.11 in ISO 11898-1) is detected prior to the acknowledgement (ACK) Slot. Figure 7 depicts the bits, which are considered as “don’t care”.

NOTE There is no requirement for the SRR bit to be received as dominant in CEFF to recognize the frame as a valid WUF.

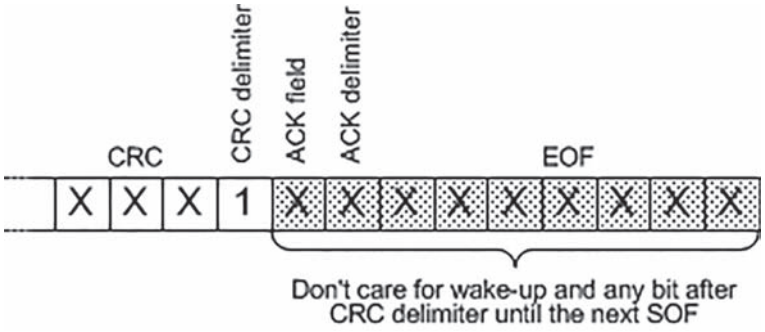


Figure 7 — Don’t care bits for frame decoding

5.9.4.5 Frame error counter mechanism

Upon activating the selective wake-up function (by e.g. a connected microcontroller) and also on expiration of $t_{Silence}$, the counter for erroneous CAN frames shall be set to zero. The initial value of the counter is zero. This counter shall be incremented by one when a bit stuffing, CRC, or CRC delimiter form error (according to ISO 11898-1) is detected. If a Classical CAN frame has been received, which is valid according to the definition in 5.9.4.4, and the counter is not zero, then the counter shall be decremented by one. Dominant bits between the CRC delimiter and the end of the intermission field shall not increase the frame error counter.

On each increment or decrement of this counter, the decoder unit in the HS-PMA shall wait for at least 6 and at most 10 recessive bits before considering a dominant bit as a start of frame. Figure 8 depicts the position of the mandatory start of frame (SOF) detection when a Classical CAN frame was received and in case of an error scenario.

Figure 8 — Mandatory SOF detection after Classical CAN frames and error scenarios

A wake-up shall happen immediately or upon the next received WUP when the counter has reached a threshold value. The default threshold value is 32, other values might be configurable.

Up to four (or up to eight when bit rate > 500 kbit/s) consecutive Classical CAN data and remote frames that start after the bias reaction time t_{Bias} has elapsed might be either ignored (no error counter increase of failure) or judged as erroneous (error counter increase even in case of no error).

Receiving a frame in CEFF with non-nominal reserved bits (SRR, r0) shall not lead to an increase of the error counter.

5.9.4.6 Tolerance to CAN FD frames (optional)

After receiving a recessive FDF bit followed by a dominant res bit, the decoder unit in the HS-PMA shall wait for at least 6 and at most 10 recessive bits before considering a further dominant bit as a start of frame. Figure 8 depicts the position of the mandatory start of frame (SOF) detection when a CAN FD frame was received and in case of an error scenario.

If bit FDF is received recessive and the following bit position is also received recessive, then this is not in the scope of this part.

Receiving a frame in FBFF or FEFF shall not lead to an increase of the error counter when the data bit rate is less or equal to four times the arbitration bit rate or 2 Mbit/s, whichever is lower. In this case dominant signals less than or equal to 5% of the arbitration bit time in duration shall not be considered to be a valid bit and shall not restart the recessive bit counter. Dominant signals longer than or equal to 17,5 % of the arbitration bit time in duration shall restart the recessive bit counter.

Alternatively or additionally a data bit rate less or equal to ten times the arbitration bit rate or 5 Mbit/s, whichever is lower, shall be supported. In this case dominant signals less than or equal to 2,5 % of the arbitration bit time in duration shall not be considered to be a valid bit and shall not restart the recessive bit counter. Dominant signals longer than or equal to 8,75 % of the arbitration bit time in duration shall restart the recessive bit counter.

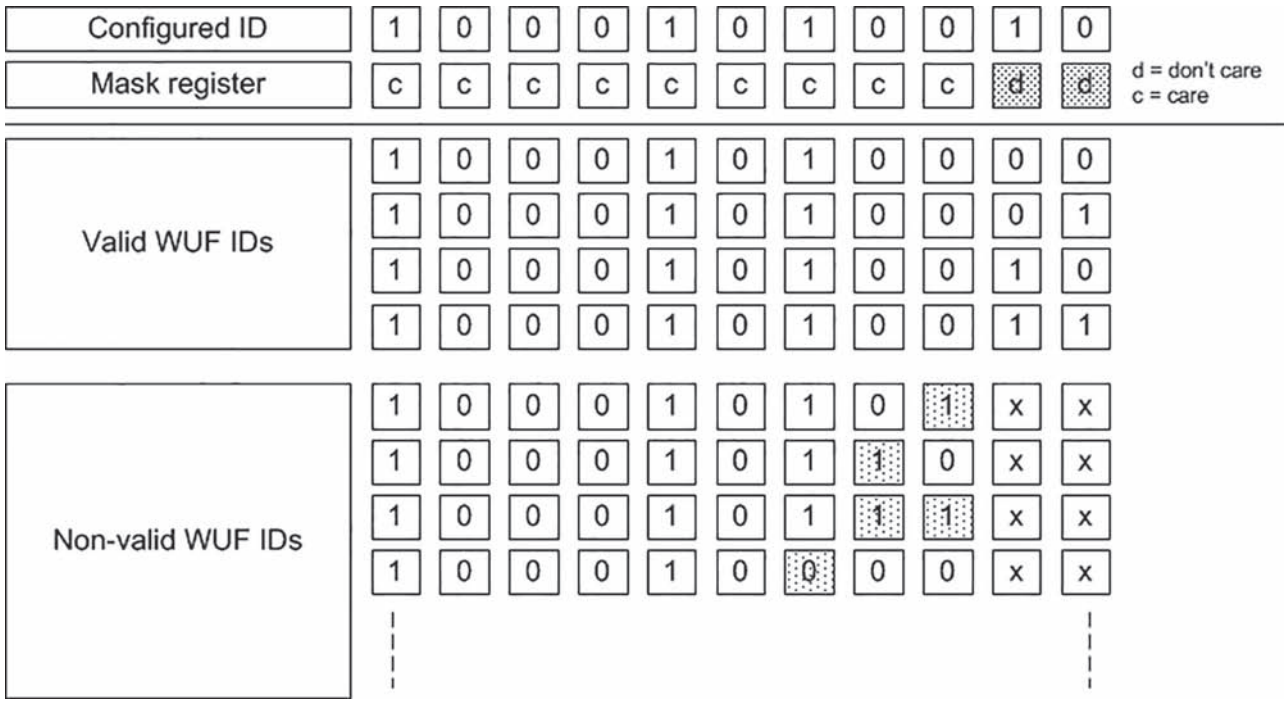
5.9.4.7 Wake-up frame ID evaluation

A CAN-ID mask mechanism shall be supported to exclude ID-bits from comparison. 11-bit and 29-bit CAN-IDs and ID-masks shall be supported. The user selects whether a WUF has to appear in CBFF or CEFF. The IDE bit is not part of the ID-mask. It has to be evaluated in any case.

All masked ID-bits except “don’t care” shall match exactly the configured ID-bits. If the masked ID-bits are configured as “don’t care”, then both “1” and “0” shall be accepted.

The masking mechanism is implementation dependent.

Figure 9 shows an example for valid WUF IDs corresponding to the ID-mask register.



Key

d Don't care

c Care

Figure 9 — Example for ID masking mechanism

5.9.4.8 Wake-up frame DLC evaluation

If the DLC matching condition is enabled, then a Classical CAN frame can only be a valid WUF when the DLC of the received frame matches exactly the configured DLC.

If the DLC matching condition is disabled, then the DLC and data field are not evaluated and a Classical CAN frame is already a valid WUF when the identifier matches (see 5.9.4.7) and the CRC is correct.

5.9.4.9 Wake-up frame data field evaluation

If the DLC matching condition is enabled, then a Classical CAN frame can only be a valid WUF if at least one logic 1 bit within the data field of the received WUF matches to a logic 1 bit of the data field within the configured WUF.

If the DLC matching condition is disabled, then the DLC and data field are not evaluated and a Classical CAN frame is already a valid WUF when the identifier matches (see 5.9.4.7) and the CRC is correct.

Figure 10 shows an example with a non-matching and a matching ID field.

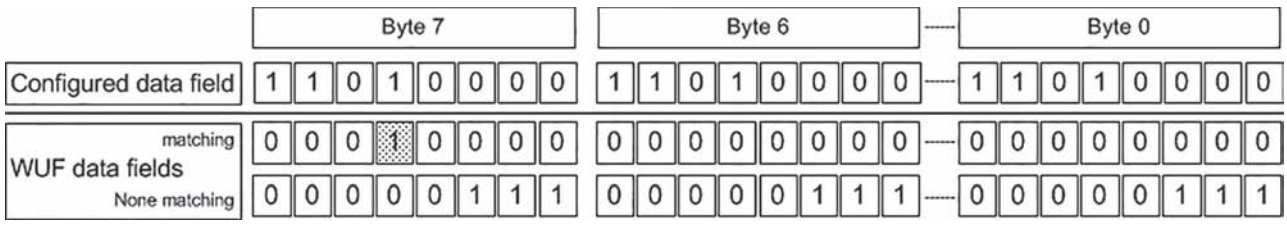


Figure 10 — Example of the data field within a received Classical CAN data frame

With this mechanism, it is possible to wake-up up to 64 independent groups of ECUs with only one wake-up frame.

5.10 Bus biasing

5.10.1 Overview

The HS-PMA implementation shall bias CAN_H and CAN_L according to Table 5 and Table 6.

When the HS-PMA implementation features a low-power mode and selective wake-up, automatic voltage biasing is required. For all other implementation either normal biasing or automatic voltage biasing shall be implemented.

5.10.2 Normal biasing

Normal biasing means: bus biasing is active in normal mode and inactive in low-power mode.

5.10.3 Automatic voltage biasing

Automatic voltage biasing means: bus biasing is active in normal mode and is controlled by the differential voltage between CAN_H and CAN_L in low-power mode. The following state machine illustrates the mechanism:

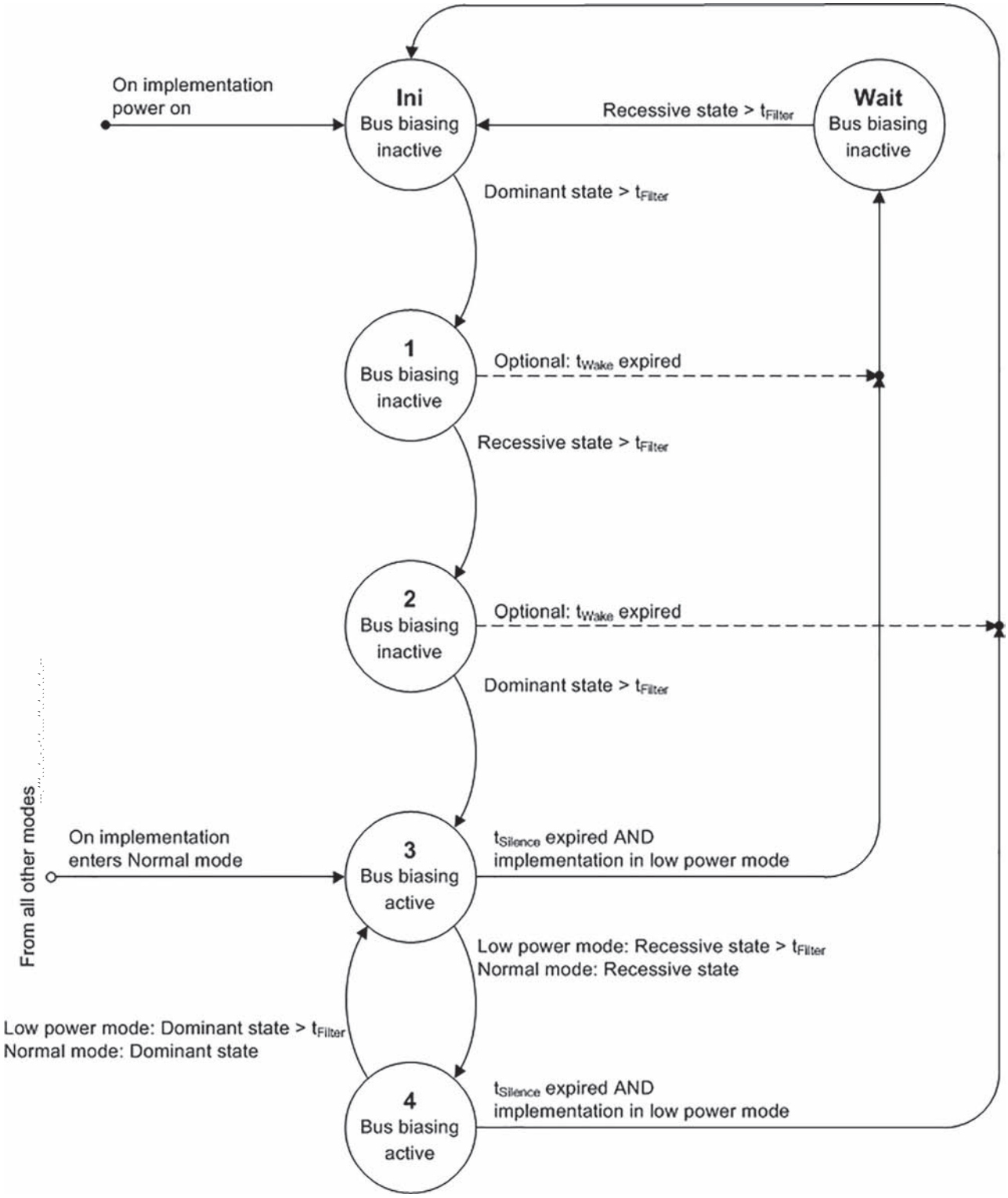


Figure 11 — Bus biasing control for automatic voltage biasing

The state-machine in Figure 11 defines the bus biasing behaviour for all operation modes. When entering state 1, the optional timer t_{Wake} shall be reset and restarted; when entering state 3 or 4, the timer $t_{Silence}$ shall be reset and restarted. Mind that in low-power mode the filter time t_{Filter} shall be applied for detection of "dominant state" and "recessive state".

Table 19 specifies the bus biasing control timings and Figure 12 the bias reaction time.

Table 18 — HS-PMA bus biasing control timings

Parameter	Notation	Value		Condition
		Min µs	Max µs	
CAN activity filter time, long [a]	t_{Filter}	0,5	5,0	Bus voltages according to table A.2
CAN activity filter time, short [b]	t_{Filter}	0,15	1,8	Bus voltages according to table A.2
Wake-up timeout, short [c]	t_{Wake}	350,0	10 000,0	Optional timeout parameter
Wake-up timeout, long [d]	t_{Wake}	800,0	10 000,0	Optional timeout parameter
Timeout for bus inactivity	$t_{Silence}$	0,6 *10^6	1,2 *10^6	Timer is reset and restarted, when bus changes from dominant to recessive or vice versa
Bus Bias reaction time	t_{Bias}	not defined	250,0	Measured from the start of a dominant-recessive-dominant sequence (each phase 6µs) until $v_{SYM} \geq 0,1$. See Figure 12 v_{SYM} as defined in Table 3

[a] The implementation does not need to meet this timing, in case the "CAN activity filter time, short" is met.

It should be noted that the maximum filter time has an impact to the suitable wake-up messages, especially at high bit rates. For example, a 500 kBit/s system, a message must carry at least three similar bit levels in a row in order to safely pass the wake-up filter. Shorter filter time implementations might increase the risk for unwanted bus wake-ups due to noise. The specified range is a compromise between robustness against unwanted wake-ups and freedom in message selection.

[b] The implementation does not need to meet this timing, in case the "CAN activity filter time, long" is met

[c] Preferred for intended use with bit rates up to 1 Mbit/s

[d] Preferred for intended use with bit rates above 1 Mbit/s

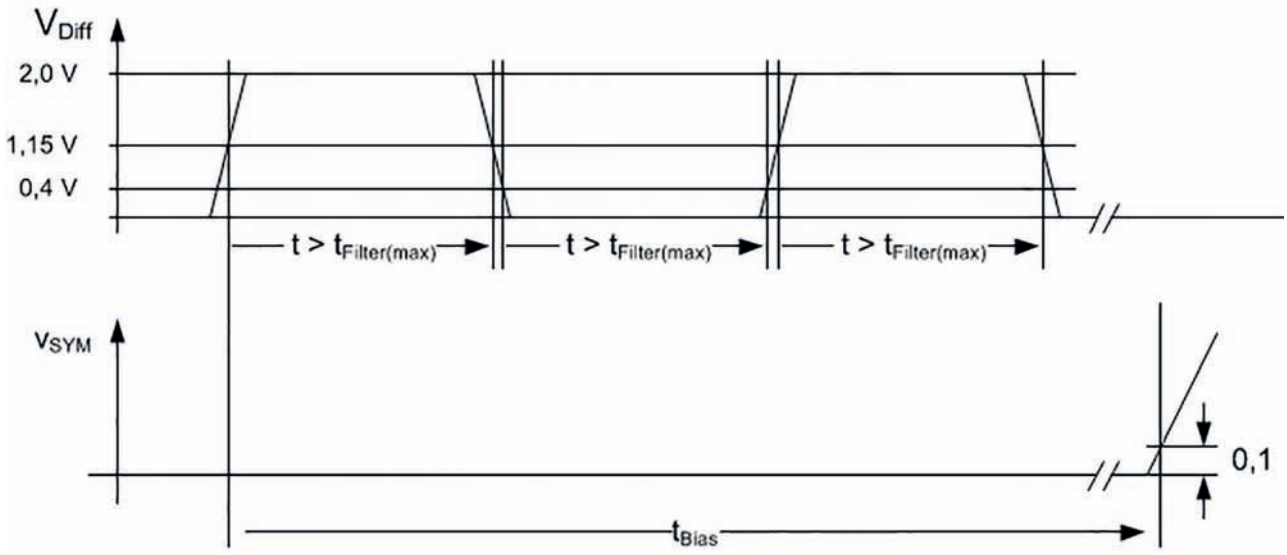


Figure 12 — Test signal definition for bias reaction time measurement

6 Conformance

The conformance test case definition and measurement setups to derive the parameters are not in the scope of this part of ISO 11898. A conformance test plan is given in ISO 16845-2.

For an implementation to be compliant with this part of ISO 11898, the HS-PMA implementation shall comply with all mandatory specifications and values given in this part of ISO 11898. If optional specifications and values are implemented, they shall comply, too. More information is given in Annex A.4.

Annex A
(informative)

ECU and network design

A.1 Mapping of OSI layers to an exemplary CAN interface implementation

Figure A.1 shows an exemplary CAN interface implementation for a MAU compliant with this part of ISO 11898.

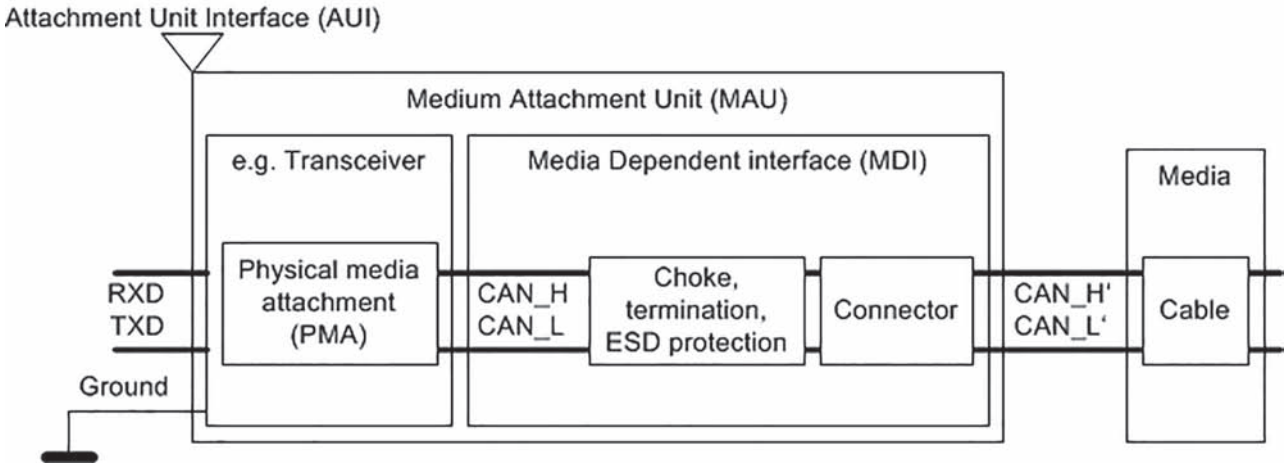


Figure A.1 — Mapping of OSI layers to an exemplary CAN interface implementation

A.2 Expectations on a CAN network

This section outlines, which input voltages on V_{CAN_L} and V_{CAN_H} are recommended for proper operation of HS-PMA implementations connected to a media.

Table A.1 shows the CAN interface voltage parameters for the reception of recessive state.

Table A.1 — Input voltage parameters for reception of recessive state

Parameter	Notation	Value			Condition
		Min V	Nom V	Max V	
Operating input voltage	V_{CAN_H}	-12,0	+2,5	+12,0	Measured with respect to the individual ground of each CAN node
	V_{CAN_L}	-12,0	+2,5	+12,0	
Differential input voltage	V_{Diff}	-3,0	0	+0,012	Measured at each CAN node connected to the media
The differential input voltage is determined by a combination of the recessive state output voltages of the individual CAN nodes present. Therefore V_{Diff} is approximately zero.					

Figure A.2 shows the voltages V_{CAN_H} and V_{CAN_L} in their interdependency during recessive state.

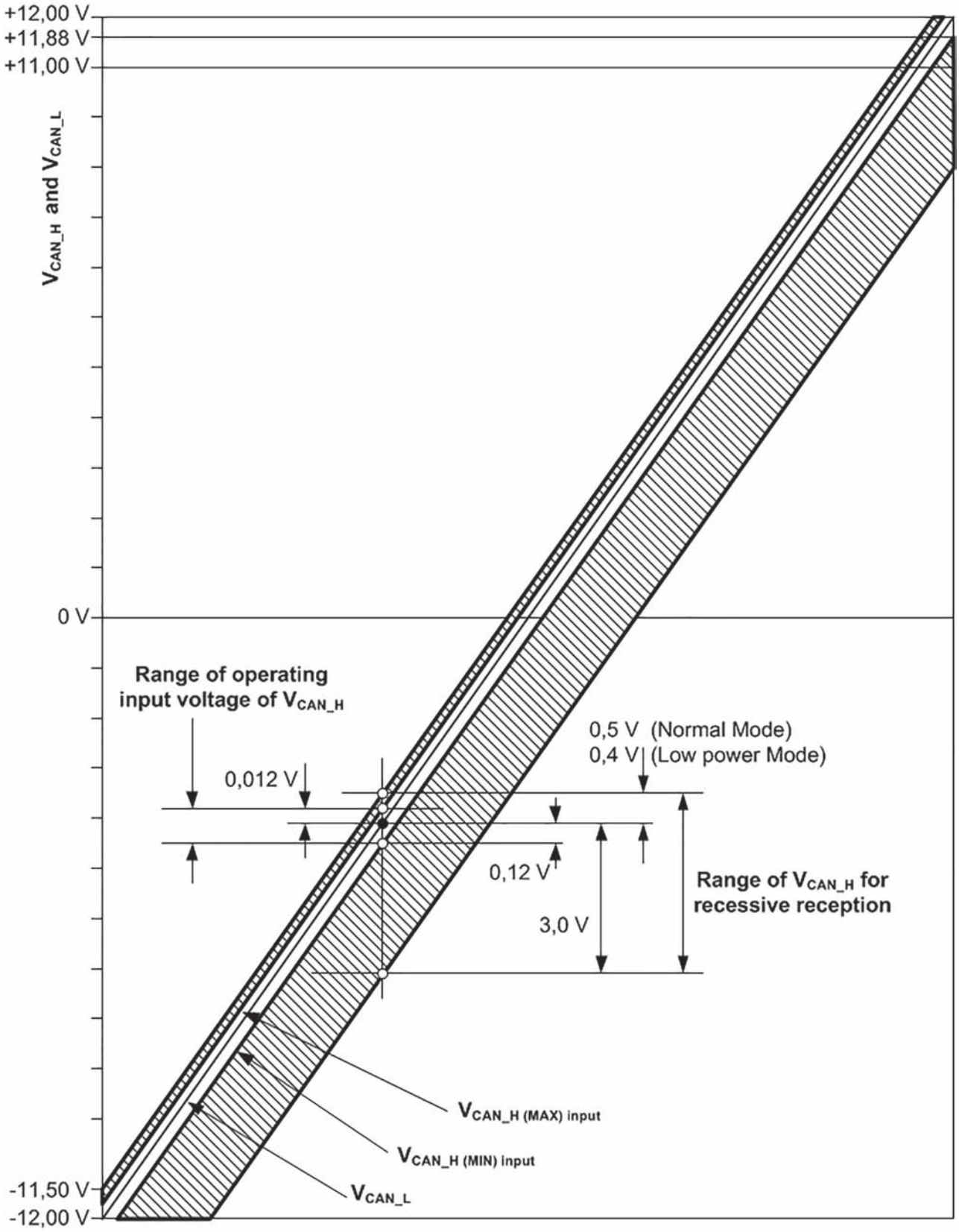


Figure A.2 — Valid voltage range of V_{CAN_H} for recessive state, when V_{CAN_L} varies from minimum to maximum common mode range

Table A.2 shows the CAN interface voltage parameters for reception of dominant state.

Table A.2 — Input voltage parameters for reception of dominant state

Parameter	Notation	Value			Condition
		Min	Nom	Max	
		V	V	V	
Common mode voltage	V_{CAN_H}	-10,8	+3,5	+12,0	Measured with respect to the individual ground of each CAN node
	V_{CAN_L}	-12,0	+1,5	+10,8	
Differential voltage [a]	V_{Diff}	+1,2	+2,0	+3,0	Measured at each CAN node connected to the media
The minimum value of V_{CAN_H} is determined by the minimum value of V_{CAN_L} plus the minimum value of V_{Diff}. The maximum value of V_{CAN_L} is determined by the maximum value of V_{CAN_H} minus the minimum value of V_{Diff}. The busload increases as CAN nodes are added to the media by R_{Diff}. Consequently, V_{Diff} decreases. The minimum value of V_{Diff} determines the number of CAN nodes allowed to be connected to the media. Also the cable material, length and cross-section between the HS-PMA implementations, as well as connectors impact the V_{Diff} that can be measured at the receiving HS-PMA's input. [a] normal bus load range, no arbitration					

Figure A.3 and Figure A.4 show the voltages V_{CAN_H} and V_{CAN_L} in their interdependency during dominant state according to Table A.2

Table A.3 — Input voltage parameters for reception of dominant state during arbitration

Parameter	Notation	Value		Condition
		Min	Max	
		V	V	
Common mode voltage	V_{CAN_H}	-10,8	+12,0	Measured with respect to the individual ground of each CAN node
	V_{CAN_L}	-12,0	+10,8	
Differential voltage	V_{Diff}	+1,2	+8,0	Measured at each CAN node connected to the media
The minimum value of V_{CAN_H} is determined by the minimum value of V_{CAN_L} plus the minimum value of V_{Diff}. The maximum value of V_{CAN_L} is determined by the maximum value of V_{CAN_H} minus the minimum value of V_{Diff}. The maximum value of V_{Diff} is specified by the upper limit during arbitration plus a ground shift of up to 3 V.				

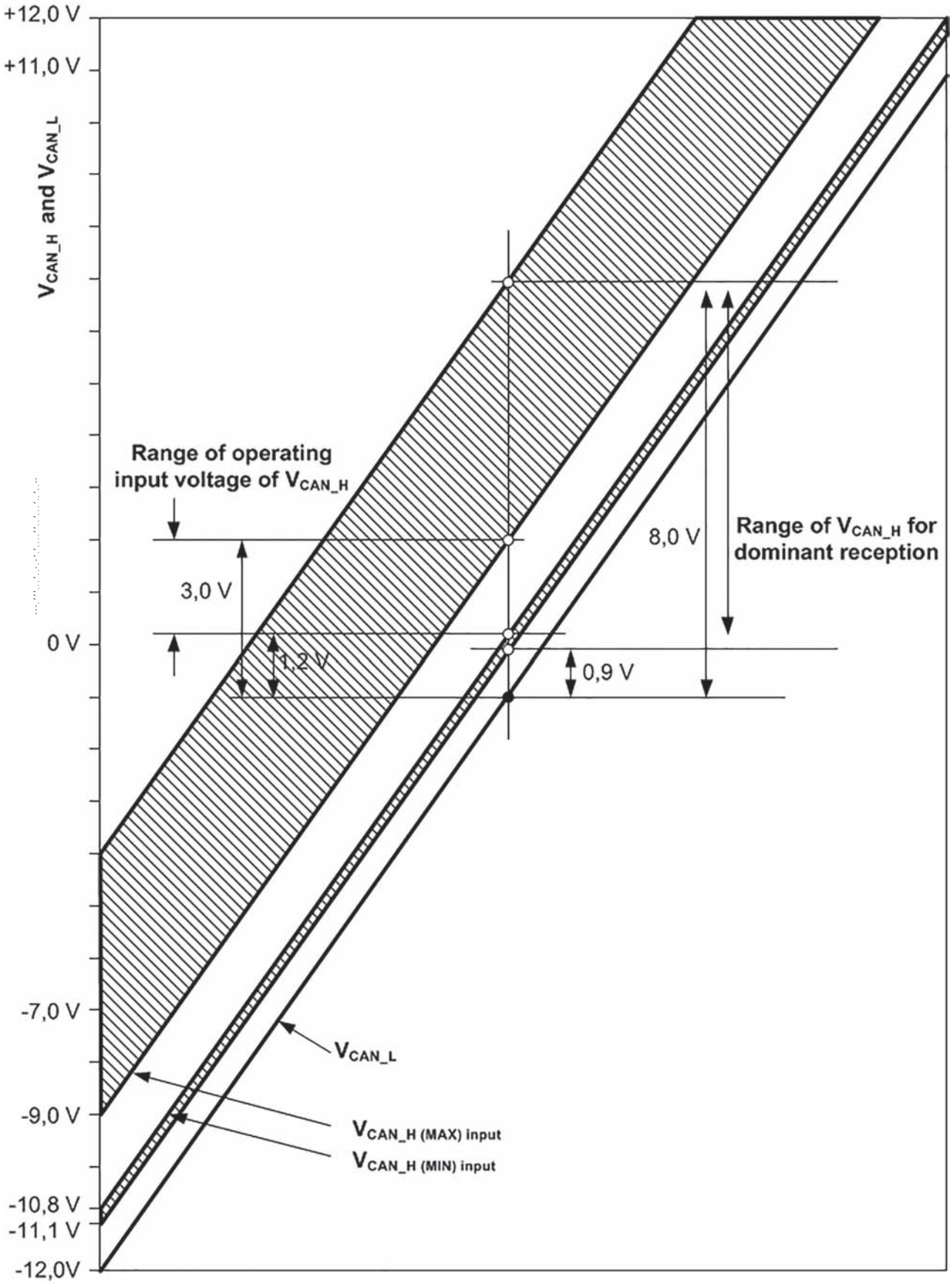


Figure A.3 — Valid voltage range of V_{CAN_H} for monitoring dominant state, when V_{CAN_L} varies from minimum to maximum common mode range during normal mode, arbitration free scenario

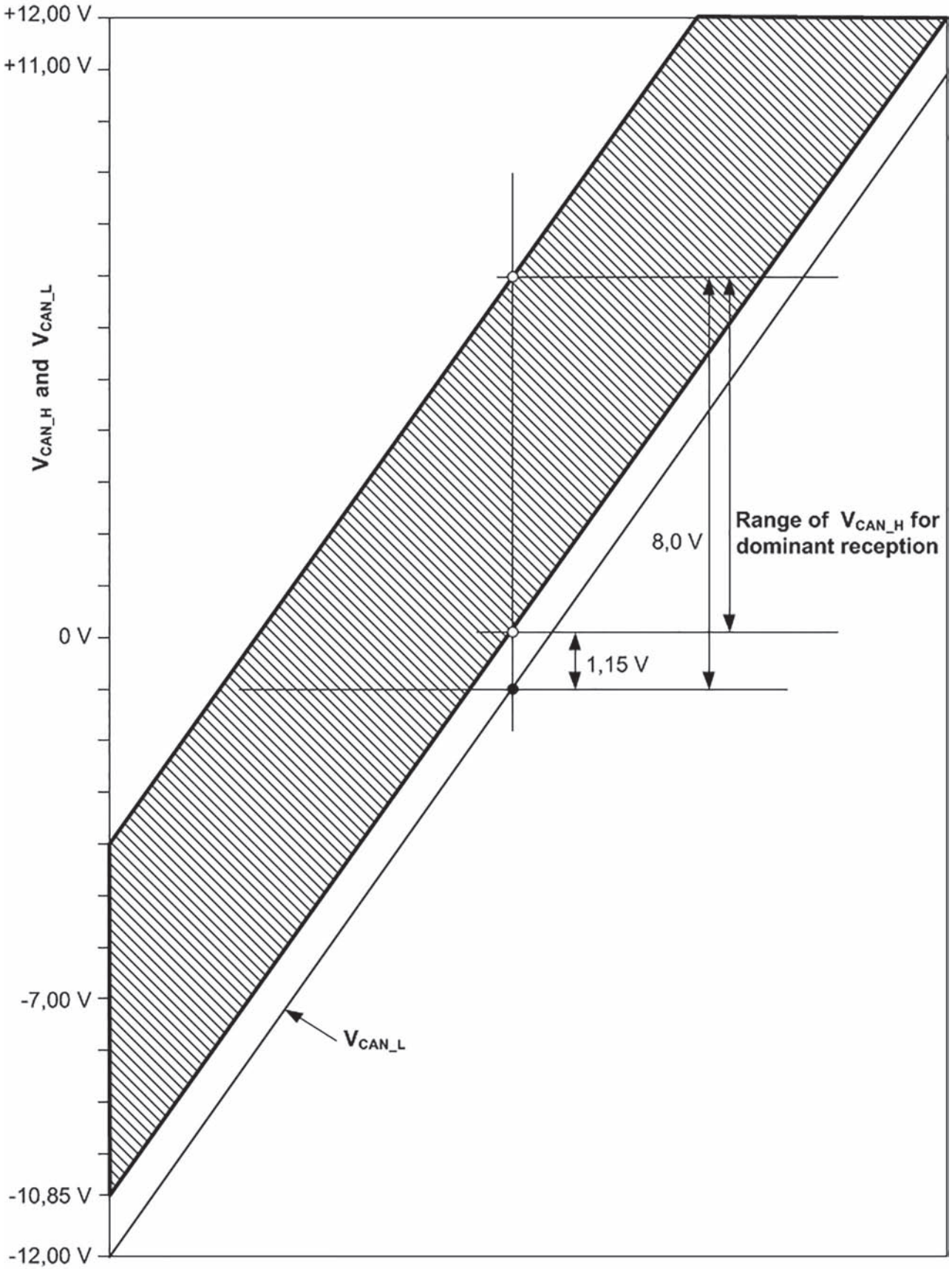


Figure A.4 — Valid voltage range of V_{CAN_H} for monitoring dominant state while the HS_PMA is not connected to the media, when V_{CAN_L} varies from minimum to maximum common mode range during low-power mode

A.3 Expectations on a datasheet of a HS-PMA implementation

The datasheet needs to state the maximum supported bit rate according to the bit time requirements given in Table 13 and Table 14 in this part of ISO 11898.

The datasheet needs to state the supported arbitration bit rates for partial networking in case selective wake-up functionality is implemented.

In case the implemented selective wake-up functionality is tolerant to frames in FBFF and FEFF, the maximum supported ratio of data bit rate and arbitration bit rate needs to be stated, as well as the absolute maximum data bit rate.

The data sheet needs to state which of the functionalities classified as optional in this standard are implemented in the particular HS-PMA implementation (e.g. extended bus load range, transmit dominant timeout, CAN activity filter time, etc.)

A.4 Overview of optional features and implementation choices

This part of ISO 11898 offers the following options for a HS-PMA. Table A.4 lists functional options that are specified in this part of ISO 11898.

Table A.4 — Optional features and functions

No.	Option	Reference
1	Support of extended bus load range	5.3, Table 2
2	Transmit dominant timeout function	5.3, Table 7
3	Support of bit rates above 1 and up to 2 Mbit/s	5.6, Table 13
4	Support of bit rates above 2 and up to 5 Mbit/s	5.6, Table 14
5	Support of extended maximum ratings for CAN_H and CAN_L	5.7, Table 15
6	Support of Wake-up	5.9, Table 17

In case the HS-PMA implementation implements low-power mode(s), then a Wake-up mechanism according to Table 18 needs to be implemented. Each Wake-up mechanism has options and alternatives, which are summarized in Tables A.5, A.6, A.7 and A.8.

Table A.5 — Alternative timings within the wake-up features

No.	Alternative 1	Alternative 2	Alternative 3	Reference
1	CAN activity filter time, long	CAN activity filter time, short	CAN activity filter time, long and CAN activity filter time, short	5.9, Table 17
2	Wake-up timeout, short	Wake-up timeout, long	No Wake-up timeout	5.9, Table 17

Table A.6 — Options of the selective wake-up functions

No.	Option	Reference
1	Support of disabling DLC matching	5.9.4.4.

Table A.7 — Alternative for handling of CAN FD frames by the selective wake-up function

No.	Alternative 1	Alternative 2	Alternative 3	Reference
1	No tolerance (not recommended for new designs)	Tolerance to CAN FD frames with bit rate ratio of up to 1:4 or maximum 2 Mbit/s in data phase	Tolerance to CAN FD frames with bit rate ratio of up to 1:10 or maximum 5 Mbit/s in data phase	5.9.4.6

Table A.8 — Alternatives for TXD dominant timeout function

No.	Alternative 1	Alternative 2	Alternative 3	Reference
1	No timeout	Timeout, short	Timeout, long	5.3

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