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Implementation of G.723.1Decoder on Zynq FPGA using HLS

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***Abstract*— For the speech communication techniques there is a lot of scope nowadays. Due to number of applications increasing, there is a need for the approach for the data compression techniques which uses bandwidth and storage space. In this MP-MLQ excitation which has high rate working mode ITU-T G723.1 algorithm is implemented. The G723.1 Decoder is implemented through HLS on to the Zynq-7 ZC706 FPGA Evaluation Board. The comparison of the area utilization is done at C-synthesis level, post-synthesis level, post-implementation level.**

Keywords—Vivado HLS, Vivado, Zynq-7 ZC706 Evaluation Board, MPC-MLQ,G723.1, High Level Synthesis(HLS).

I. INTRODUCTION

In the recent years, there is demand for high quality communications. Speech compression is utilized in VoIP networks and also digital satellite systems. The G.723.1 was designed for standardizing the telephony and video conference over the public telephone lines and it is a ITU H.234 standard.

G.723.1 is widely used in Voice Over IP(VOIP) applications because it uses low bandwidth.
Computational complexity, algorithmic delay, speech quality degradation are the problems occurred in Code Excitation Linear Prediction(CELP). G.723.1 codec overcomes all the problems of CELP codec. It is an audio codec which compresses the audio in 30ms frames. It operates in two different bit rates hence the name Dual rate speech coder.

The two different bit rates are:-
- 6.3kbit/s uses a MPC-MLQ algorithm
- 5.3kbit/s uses an ACELP algorithm

II. G.723.1 CODEC

G.723.1 codec with bit rate 6.3kbit/s which uses a Multi-pulse Maximum Likelihood Quantization (MPC-MLQ) algorithm is implemented. This MPC-MLQ algorithm is implemented for Multi-pulse Mode. The main application of this is used in Voice over IP applications because its having a low bandwidth requirement. The block diagram of G.723.1 codec is showed in Fig 1.

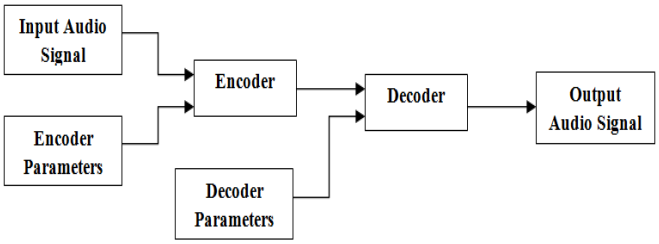

Fig 1:- Block Diagram of G.723.1 Codec

The audio signal is fed to the G.723.1 encoder and also the encoder parameters are also fed into the encoder. The encoder generates the bit-stream which will be stored as a binary data file. This data file along with the decoder parameters are fed into the decoder, after processing it gives a reconstructed audio signal as a output.

III. G.723.1 DECODER

At the encoder, the bit stream is generated and will be stored as a binary data file. Each frame of the data is preceded by a two-bit code indicating the type of mode to be selected. The block diagram of G.723.1 Decoder is shown in Fig 2.
Once the mode is selected, it starts processing that particular mode and the output of that mode is passed on to the LP filter for filtering and later the filtered output is passed on to the formant post filter and then the reconstructed speech or audio signal will be the output of the decoder.

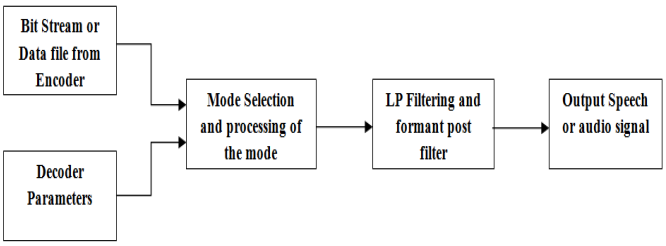

Fig 2:- Block Diagram of G.723.1 Decoder

Before processing the mode, a particular mode is to be slected based on the frame code. The Table.1 shows the frame code and mode selection for that particular frame code.

Table 1:- Mode Selection based on frame code

Frame Code	Mode Selection/ Frame Type
00	Multi-pulse
01	ACELP
10	SID
11	Null

Fig.3 shows the different types of modes in G.723.1 codec. It has 5 different types of modes and are:-
-Multi-pulse(MP) mode
-Algebraic Code Excited Linear Prediction(ACELP) mode
-Silence Insertion Descriptor (SID) mode
-Null mode
-Packet Loss Concealment (PLC) mode

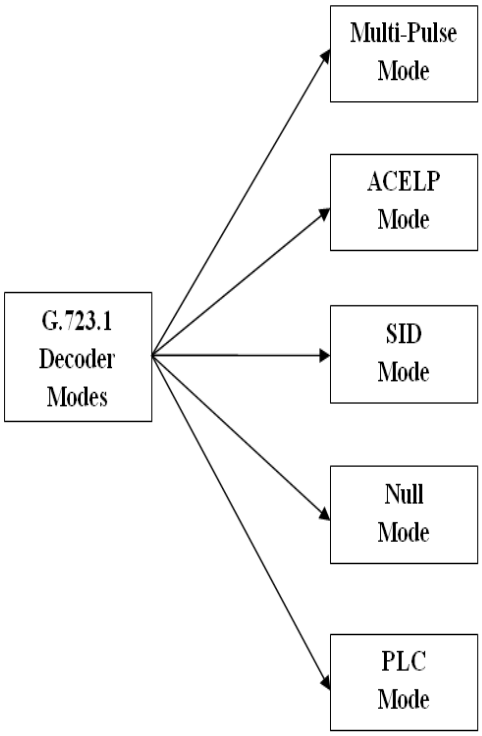

Fig 3:- Types of Modes in G.723.1

A. Multi-pulse Mode

For this mode to be selected, the frame code should be 00. The total number of data bits used in this mode is 190bits. Out of which 24bits are used for LSF parameters, 18bits for the adaptive codebook lags, 48bits for combined gain code, 4bits for MP grid codes, 1bit is reserved, 73bits for MP position codes, 22bits for MP signs, 2bits for the frame selection. It uses 24bytes per frame.

B. ACELP Mode

For this mode to be selected, the frame code should be 01. The total number of data bits used in this mode is 160bits. Out of which 24bits for LSF parameters, 18bits for codebook lags, 48bits for combined gain codes, 4bits for ACELP grid codes, 48bits for ACELP position codes, 16bits for ACLEP signs.
It uses 20bytes per frame.

C. SID Mode

For this mode to be selected, the frame code should be 10. The total number of data bits used in this mode is 32bits. Out of which 24bits is used for LSF parameters, 6bits for SID gain code, 2bits for the mode selection. It uses 4bytes per frame.

D. Null Mode

For this mode to be selected, the frame code should be 11. The total number of bits used in this mode is 2bits. These 2bits are already used for the frame selection. It uses 1byte per frame.

E. PLC Mode

These are estimated only for the LPC residual of voiced frames using Fast Fourier Transform (FFT) [7]. Most of the parameters are not transmitted for the unvoiced frames which includes the Fourier magnitude, aperiodic flag, and the voicing for bands 1 to 4. These 13 bits will be used for error correction coding.

IV. IMPLEMENTATION

The G.723.1 Decoder codec algorithm is coded in C using Vivado HLS and it's been synthesized and converted to Verilog. The Verilog code is taken into Vivado and then constraints is written for this. For the same, if IP cores is used then all the IP cores in the design are added to it and then it is synthesized. Once synthesis is completed without errors, then implementation process is started where the logic is placed on the FPGA board. The FPGA board selected is Zynq ZC706.
There are several blocks in the Encoder and the complete block diagram along with the modules/functions used at particular block/phase is shown.

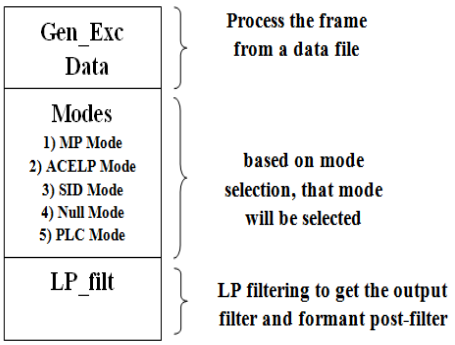

Fig 4:- Modules/Functions used in G.723.1 Decoder

V. RESULTS

The G.723.1 Speech Decoder algorithm is implemented in Vivado HLS by coding it in C. The Vivado HLS produces the area and latency results. Using the Vivado HLS, the P Encoder is converted into RTL and then the design is synthesized using Vivado. The post-synthesis and post-implementation area utilization results are obtained which are better than the utilization results obtained in HLS.
Latency is defined as the number of clock cycles used by the design.

The Table.1 shows the total number of clock cycles used by each module/function which is obtained in Vivado HLS.

Table 1:- No. of Clock Cycles used by each module

Modules	Latency		Interval	
	Min	Max	Min	Max
Multi pulse Mode	28978	31947	28978	31947
SID Mode	41956	44162	41957	44163
Null Mode	38763	40661	38764	40662
PLC Mode	1568	7368	1569	7369

The Table.2 shows the area utilization of each modules in the G.723.1 Decoder. These results are obtained after C-synthesis is finished

Table 2:- Area Utilization of Sub-modules at C-Synthesis stage

Modules	Area Utilization(No.)			
	BRAM _18K	DSP48 E	Flip Flop	LUT
Multi pulse Mode	24	96	29246	43130
SID Mode	213	185	26809	50351
Null Mode	208	181	26389	49130
PLC Mode	9	7	1793	3273

Once C-synthesis is finished, the Verilog, VHDL, System-C codes are generated automatically by the Vivado HLS tool itself[8]. In this we have taken Verilog Code and post-synthesis is done. The tool used from this stage is Vivado[9].

The Table.3 shows the area utilization of all the sub-modules which are obtained from the post-synthesis step.

Table 3:- Area Utilization of Sub-modules at Post-Synthesis Stage

Modules	Post-Synthesis Area Utilization(No.)			
	BRAM _18K	DSP48 E	Flip Flop	LUT
Multi pulse Mode	13	6	20581	18319
SID Mode	12	8	16803	16259
Null Mode	12	5	16594	16021
PLC Mode	5	-	1094	1186

So, compare the results of the area utilization at C-synthesis stage (Table.2) and at the post-synthesis stage (Table.3). This comparison exactly tells us the results obtained at the post-synthesis stage using a Verilog code uses less resources.

As the post-synthesis step is completed, next the constraints for the design has to be written and this will be used in the implementation process. The Table.4 shows the area utilization of all the sub-modules during the post-implementation stage.

Table 4:- Area utilization of all sub-modules at the post-implementation stage

Modules	Post-Implementation Area Utilization(No.)			
	BRAM _18K	DSP48 E	Flip Flop	LUT
Multi pulse Mode	13	76	24396	25000
SID Mode	15	173	22766	24969
Null Mode	15	132	23692	25586
PLC Mode	5	5	1427	1552

Comparing the results of area utilization of sub-modules at C-synthesis stage (Table.2) and at the post-implementation stage (Table.4). This depicts that, results of post-implementation are better compared to that at the C-synthesis stage.

The Fig.7 which shows the G.723.1 Decoder C-synthesis area utilization report for the Zynq-7 ZC706 Evaluation board and the family is xc7z045ffg900-2.

In the Fig.7 for some of the parameters there is a red indication where it tells its using more resources than the total no. of resources in that FPGA board. These results are obtained from Vivado HLS after C-synthesis process is finished. This will be further optimized and will be one of our future enhancement.

VI. Conclusion

The G.723.1 Decoder is implemented on Zynq-7 ZC706 FPGA Evaluation Board. The tools used are Vivado HLS and Vivado. The area utilization of sub-modules at C-synthesis level, post-synthesis level and post-implementation level are obtained. The total area of the G.723.1 Decoder at different levels are compared. The future enhancement is to optimize the area at all the three different levels and also further timing analysis of the G.723.1 Decoder to be done.

Acknowledgment

We would like to thank Mr. P Kabal for the MATlab source code.

References

[1] ITU-T G723.1 "Dual Rate Speech Coder For Multimedia Communications Transmitting at 5.3 and 6.3 kbitsh", 1996)

[2] ITU-T Recommendation G.729, 'Coding of speech at 8 kbits/s using conjugate-structure algebraic-code-excited linear-prediction (CSACELP)',3/96.

[3] S. Chang, J. Hu, 'Real-time implementation of G723.1 speech codec on a 16-bit DSP processor', Department of electronic and control engineering, National Chiao Tung Univesity, Hsinchu, Taiwan, R.O.C

[4] M. Soler, A. Andre, E. Closse, J. Laval, F. Balestro, D. Morche, P. Senn, 'An embedded DSP platform for multi-standard ITU G728, G729 & G723.1 audio compression', France Telecom, CNET

[5] http://en.wikipedia.org/wiki/G.723.1

[6] Wai C. chu, "Speech Coding Algorithm", Wiley Publication.

[7] Vivado HLS Tutorial Manual.

[8] Vivado Tutorial Manual.