Real-Time Hardware-in-the-Loop Simulation of Permanent-Magnet Synchronous Motor Drives Under Stator Faults

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***Abstract*—Hardware-in-the-loop (HIL) testing methods can facilitate the development of control strategies in a safe and inexpensive environment particularly when extreme operating conditions such as faults are considered. HIL methods rely on accurate real-time emulation of the equipment under investigation. However, no validated tools for real-time emulation of electrical drives under fault conditions are available. This paper describes the implementation of a high-fidelity real-time emulator of a permanent-magnet synchronous motor drive in a platform suitable for HIL tests. The emulator is capable of representing the drive operation under both healthy conditions and during interturn stator winding faults. Nonlinearities due to saturation, higher order harmonics, slotting effects, etc., are accounted for using four-dimensional look-up tables (LUTs) obtained by finite element analysis. The proposed model is computationally efficient and capable of running in real time in a field programmable gate array platform and is validated against simulations and experimental results in a wide range of operating conditions. Potential applications of the proposed emulation environment to the development of drive control, fault detection, and diagnostic algorithms are proposed.**

***Index Terms*—Fault field programmable gate array (FPGA), hardware-in-the-loop (HIL), modeling, permanent-magnet synchronous motor (PMSM).**

Nomenclature

i_d	d-axis current.
i_q	q-axis current.
i_f	Fault current.
Ψ_d	d-axis flux linkage.
Ψ_q	q-axis flux linkage.
Ψ_f	Flux linkage in faulted turns.
μ	Ratio of faulted turns to total number of turns.
R_s	Stator phase resistance.
R_f	Fault resistance.
ω_e	Angular electrical speed.
θ_e	Electrical rotor angle.

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I. Introduction

HARDWARE-IN-THE-LOOP (HIL) methodologies, whereby a piece of hardware is substituted by an accurate real-time emulation, have gained widespread acceptance as a tool for rapid testing and development of data acquisition systems, electronics and control strategies in a large number of industrial applications including automotive, energy, or aerospace sectors where safety implications, cost, and complexity of full-scale prototyping might be significant. HIL methods can be used as tools to develop control strategies for components and systems in all operating conditions including extreme conditions such as those resulting from faults in a safe, nondestructive environment. Due to the increasing use of permanent-magnet synchronous motor (PMSM) drives in safety critical applications such as automotive traction and aerospace actuation, HIL methods capable of accurately emulating motor drives in all operating modes including faulty conditions can provide drive systems integrators with a useful and relatively inexpensive tool for the development and testing of fault detection, diagnostic techniques, and postfault control actions.

Although many motor drive emulators for HIL testing have recently been proposed in academic research and by commercial vendors, so far no validated method capable of accurately emulating in real time the dynamics of a machine under faulty conditions has been demonstrated. The main contribution of this paper is demonstrating a novel real-time emulation of PMSM drives suitable for HIL testing of both healthy and faulty conditions, considering in particular interturn stator short-circuit faults, which have been identified as a major cause of electrical failure in a machine [1]. Short-circuit faults typically start with interturn faults [2], which can eventually result in demagnetization or further catastrophic failure due to large circulating currents [3].

The degree of fidelity by which HIL systems emulate the physical behavior of the device under testing in realistic operating conditions depends on the availability of an accurate representation of the physical system under investigation. Although detailed models such as those based on time-domain

cosimulation of finite elements (FEs) provide a high degree of fidelity, their computational complexity prevents their applicability to the real-time computation required for HIL simulation. Real-time simulation of electric motor drives is particularly challenging due to the fast nature of the dynamics involved. Commutation of pulse width modulated (PWM) signals at tens of kHz requires sampling rates in the order of several MHz in order to obtain reasonable accuracy. Field programmable gate arrays (FPGAs) are emerging as the platform of choice for complex real-time simulations due to their ability to process data in parallel allowing for sampling rates and execution up to the MHz range.

HIL emulation of electric machines and drives has been proposed for induction motors (IMs) [4]–[10] and PMSM [9]–[19]. Due to the requirements for computational efficiency, most of the published methods for real-time emulation of electric machines rely on analytical models with various degrees of simplifications. An HIL model for IM based on permeance network (PN) is presented in [5]. A similar approach based on nonlinear magnetic equivalent circuit (MEC) is employed to model IM in [7]. A unified framework for FPGA-based emulation of electrical machines based on state-space representation with constant inductances is presented in [10]. A real-time model based on the analytical solution of field equations to account for space harmonics in the air-gap flux density distribution of PMSM has been developed in [11] under the assumption of linear superposition.

While analytical models based on PN, MEC or analytical field solutions can achieve the computational efficiency required for real-time implementation, they might lack generality, requiring significant effort to adapt models to different topologies. Furthermore, analytical models are often based on simplifying assumptions of linearity/superposition, which might not be generally applicable. Models based on precalculated FE solutions and stored in look-up tables (LUTs) for real-time implementation have been proposed as an easier to implement and more general solution to take into account non-linearities in machine behavior [5], [12], [14], [15], [20]. A real-time PMSM model taking into account angular variation of phase inductances due to space harmonics and slotting effects has been proposed [12]. However, the use of constant inductance-based model lacks the ability to account for nonlinearities due to saturation of the magnetic circuit. Even if current dependent inductances are used, the separation of flux linkages in armature reaction and permanent magnet induced fluxes is only valid under linear conditions. Similar models based on pretabulated inductances and flux maps accounting for saturation and spatial harmonics have been proposed in [13]–[15]. However, these require proprietary tools and are based on variable inductances, which pose problems in real-time simulation in voltage-driven models as the nonlinear relation between flux linkages and currents may not be easily inverted in real-time calculations. The use of differential inductances and precalculated inversion of current-flux relationship is proposed in [21].

Although many of the solutions proposed in the literature successfully address the issues of accuracy and computational efficiency for real-time emulation of a drive system in healthy conditions, no general method capable of accurately emulating the dynamics of a machine under faulty conditions has been presented. Models of stator winding interturn short circuits for PMSM have been proposed based on a number of analytical modeling techniques including the use of dynamic mesh reluctances model [22], PN [23], and constant inductances [24], [25]. Besides the relative complexity in the derivation of the model and the inevitable simplifying assumptions required in most analytical models, the difficulty in accounting for the angular variation of flux linkages due to high-order harmonics in the back electromotive force or slotting effects in these models has led to the development of machine models based on the extraction of flux linkage maps from FE magnetostatic computations as function of stator currents and rotor position [20], [26]. The model accounts for often neglected dependence of flux linkages on rotor angular position and can easily be extended to account for operation under interturn short circuits [27]. The rest of the paper describes the real-time implementation of a high-fidelity nonlinear model of PMSM drive under both healthy and interturn stator winding short-circuit conditions. The method, based on [27], results in an accurate, yet computationally efficient modeling technique since the terminal current versus stator flux linkages relationships are precalculated offline and stored in LUTs during real-time operation. Practical implementation in an FPGA-based platform is illustrated and validation of the proposed emulation is presented both against FE simulations and experimental tests over a wide range of operating conditions. Results show a good degree of accuracy on the real-time emulation while maintaining a low computational complexity for implementation on low-cost hardware.

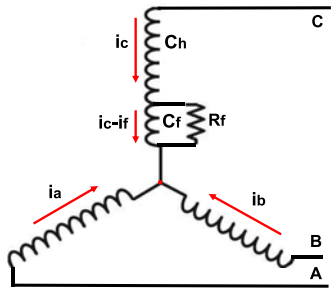


Fig. 1. Three-phase stator winding with interturn short circuit fault.

II. High-Fidelity Fault Model of PMSM

The proposed modeling framework for PMSM under interturn short-circuit fault is adapted from [27] and illustrated with reference to Fig. 1. Without loss of generality, the turn fault is assumed to be in phase C divided into a healthy and a faulty coils denoted as C_h and C_f, respectively. The fault is modeled by a fault resistance R_f, and the fault current is denoted by i_f. The ratio of short-circuited turns to the total number of turns in the phase winding is indicated with μ.

A. Analytical Model in dq-Frame

In the synchronous dq reference frame, the voltage equations describing the stator flux linkages dynamics can be

demonstrated to be [27]

$$v_d = R_s i_d + \frac{d\psi_d}{dt} - \omega_e \psi_q - \frac{2}{3}\mu R_s \sin\left(\theta_e + \frac{2}{3}\pi\right) i_f \quad (1a)$$

$$v_q = R_s i_q + \frac{d\psi_q}{dt} + \omega_e \psi_d - \frac{2}{3}\mu R_s \cos\left(\theta_e + \frac{2}{3}\pi\right) i_f \quad (1b)$$

whereas the voltage across the shorted turns is given by

$$v_f = R_f i_f = \mu R_s \big(i_d \sin(\theta_e + 2\pi/3) + i_q \cos(\theta_e + 2\pi/3) - i_f\big) + \frac{d\Psi_f}{dt}. \quad (2)$$

The relationships between stator flux linkages, stator currents, and rotor mechanical angular position θ_m are given by the nonlinear four-dimensional (4-D) maps

$$\Psi_d = f_d(i_d, i_q, i_f, \theta_m) \quad (3)$$

$$\Psi_q = f_q(i_d, i_q, i_f, \theta_m) \quad (4)$$

$$\Psi_f = f_f(i_d, i_q, i_f, \theta_m) \quad (5)$$

which can be extracted from a set of magnetostatic FE computations and stored in LUTs. Saturation, spatial saliency, and harmonics are accounted for. Although neglected here, iron losses and thermal effects can also be included in the same modeling framework [28]. Integration of (1) and (2) requires the inversion of the flux maps (3)–(5) to give

$$i_d = f_d^{-1}(\Psi_d, \Psi_q, \Psi_f, \theta_m) \quad (6)$$

$$i_q = f_q^{-1}(\Psi_d, \Psi_q, \Psi_f, \theta_m) \quad (7)$$

$$i_f = f_f^{-1}(\Psi_d, \Psi_q, \Psi_f, \theta_m). \quad (8)$$

While this inversion could in principle be achieved in dynamic simulations using, e.g., iterative algorithms, given the nonlinearity of (3)–(5), it would result in computationally intensive calculations, which could be very challenging for real-time implementation. Instead, the current maps (6)–(8) are precalculated offline and stored in 4-D LUTs.

B. FE Model

Validation of the proposed modeling methodology is performed with reference to a three-phase, 6-pole, and 36-slot permanent magnet assisted synchronous reluctance machine designed to maximize reluctance torque, whose cross section is shown in Fig. 2. The machine has two slots per pole per phase and incorporates a three-step rotor skew of 7° (mech) modeled according to the method described in [27]. Laminations were manufactured by a process of laser cutting whose detrimental effect on machine performance is taken into account in the FE model by addition of extra air gaps.

Two turns in phase C have been modeled discretely to allow for interturn short-circuit emulation. Faults in any other phase can be easily simulated without the need to run any further FE computation, by simply shifting the rotor electrical angle as

$$\theta_e = \begin{cases} \theta_e - 2/3\pi\,, & \text{fault in phase a} \\ \theta_e - 4/3\pi, & \text{fault in phase b} \\ \theta_e\,, & \text{fault in phase c.} \end{cases} \quad (9)$$

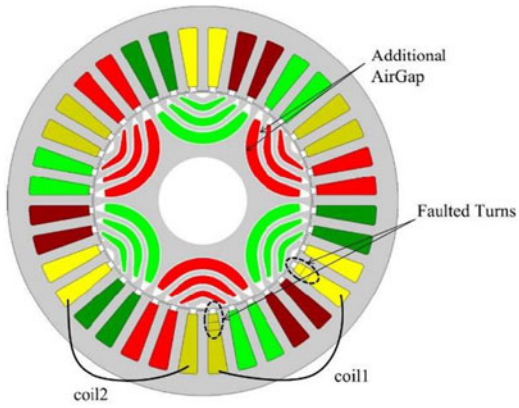


Fig. 2. Full FE model of the employed IPM machine.

III. Hardware Implementation

Real-time implementation requires discretization of (1) and (2). The chosen algorithm could have implications on accuracy and stability of the numerical simulation depending on the discretization time step [29]. The computational efficiency of the model allows the choice of relatively small time step ($\sim$1 μs) compared to the electrical time constants guaranteeing stability and accuracy. For simplicity in implementation, the forward Euler discretization is used resulting in

$$\psi_d(k+1) = \psi_d(k) + \Delta t\Big[v_d(k) - R_s i_d(k) + \omega_e(k)\psi_q(k) + \frac{2}{3}\mu R_s \sin(\theta_e(k) + 2/3\pi) i_f(k)\Big] \quad (10a)$$

$$\psi_q(k+1) = \psi_q(k) + \Delta t\Big[v_q(k) - R_s i_q(k) - \omega_e(k)\psi_d(k) + \frac{2}{3}\mu R_s \cos(\theta_e(k) + 2/3\pi) i_f(k)\Big] \quad (10b)$$

$$\psi_f(k+1) = \psi_f(k) + \Delta t\Big[v_f(k) - \mu R_s\big(i_d(k)\sin(\theta_e(k) + 2\pi/3) + i_q(k)\cos(\theta_e(k) + 2/3\pi) - i_f(k)\big)\Big]. \quad (10c)$$

The developed model is implemented on a commercially available data acquisition and control platform NI cRIO-9082. The code is implemented on the Spartan-6 LX150 FPGA-based chassis and programmed through LabVIEW FPGA. The FPGA is clocked at 40 MHz. Six PWM gate drives digital inputs are sampled at 5 MHz. Output currents are generated with a digital-to-analog conversion at 115 kHz rate. A schematic of the proposed arrangement in a typical controller-in-the-loop testing is shown in Fig 3.

A 32-b fixed-point representation is used for the internal variables. A schematic diagram illustrating the emulation step is shown in Fig. 4.

State variables and outputs of the model are the stator flux linkages, rotor angle and currents, respectively. Current output calculation is based on the 4-D current maps (6)-(8). Since

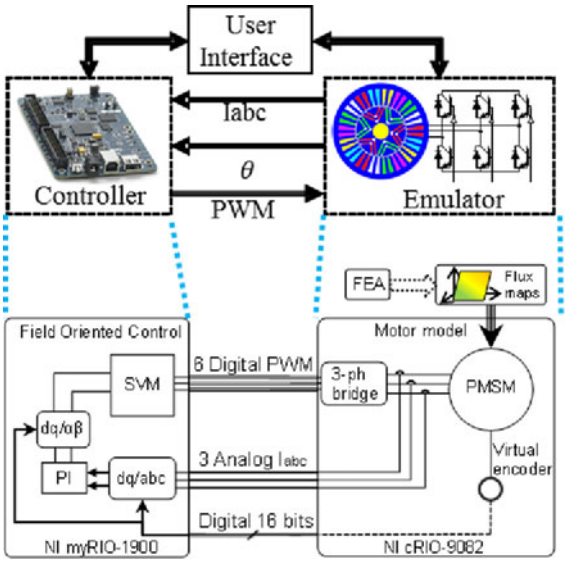


Fig. 3. Block diagram illustrating the HIL arrangement.

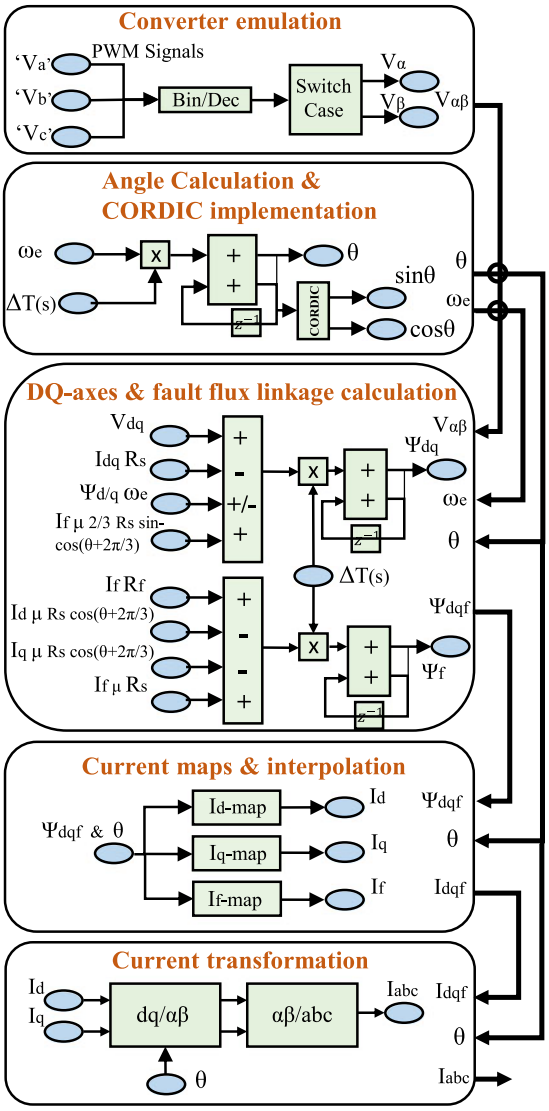


Fig. 4. HIL design configuration.

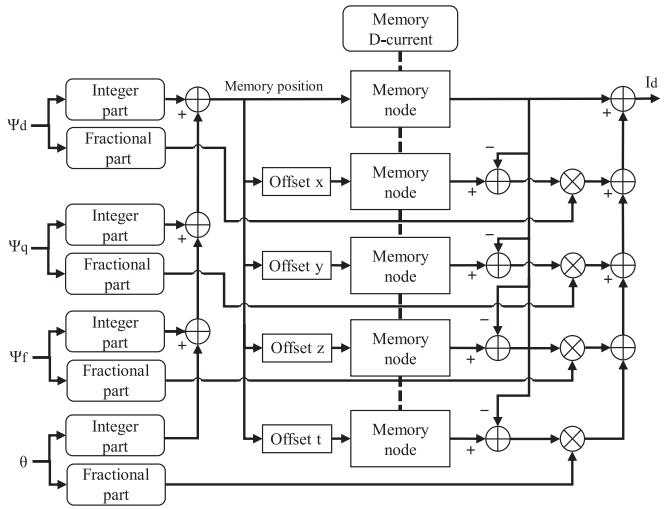


Fig. 5. Interpolation system block diagram.

FPGAs do not support multidimensional memory storage, the 4-D arrays containing dq-axes and fault currents as functions of $\psi_d, \psi_q, \psi_f, \theta$ have been rearranged in a 1-D array. A computationally efficient method of memory addressing based on 4-D linear interpolations on 1-D arrays of data has been implemented as schematically illustrated in Fig. 5. The 4-D LUT is based on the application of four successive 1-D interpolations. Appropriate offsets, depending on the spatial discretization in the $\psi_d, \psi_q, \psi_f, \theta$ space and the resulting number of elements in the tables, are required to access the correct position in the unidimensional memory array. For the case under study, there are 12 steps in d-axis flux, q-axis flux, and faulted coil flux and 61 steps in rotor position θ, resulting in 105 408 elements per current map. Given the relative complexity of such system, pipelining must be employed for parallel data processing.

For computational efficiency and speed of execution only FPGA's internal block RAM is used for data storage of the LUTs. The use of incremental inductances proposed, e.g., in [21] might have increased storage requirements resulting in the need for additional external memory with additional overhead in terms of access time.

Three-phase converter emulation has been carried out considering only eight switching states including two zero states, as shown in Table I. Dead times are not considered for this application but can be easily included.

Table II lists the FPGA resource usage for the proposed model. The most demanding subsystem in terms of resources is the LUT allocation, which results in 99% usage of the available block RAM. Most of the arithmetic calculations based on adders/multiplier and accumulator are implemented using the available DSP48 blocks. Higher resolution in the current/flux maps, and hence bigger LUTs, can easily be obtained with bigger and more expensive FPGAs or using external RAM.

Table III lists the rate of execution of each subsystem of the real-time simulation. In particular, the table shows the number of cycles of the 40-MHz clock required for the calculation of each subsystem. The most demanding is the current maps interpolation. Since all parts are executed in parallel, the total

TABLE I
THREE-PHASE CONVERTER SWITCHING STATES

Switching state	Switches ON	Space vector	Va	Vb	Vc
0	Q_2, Q_4, Q_6	$V_1(0,0,0)$	0	0	0
1	Q_1, Q_4, Q_6	$V_2(1,0,0)$	$\frac{2}{3}$ Vdc	$-\frac{1}{3}$ Vdc	$-\frac{1}{3}$ Vdc
2	Q_1, Q_3, Q_6	$V_3(1,1,0)$	$\frac{1}{3}$ Vdc	$\frac{1}{3}$ Vdc	$-\frac{2}{3}$ Vdc
3	Q_2, Q_3, Q_5	$V_4(0,1,0)$	$-\frac{1}{3}$ Vdc	$\frac{2}{3}$ Vdc	$-\frac{1}{3}$ Vdc
4	Q_2, Q_4, Q_5	$V_5(0,1,1)$	$-\frac{2}{3}$ Vdc	$\frac{1}{3}$ Vdc	$\frac{1}{3}$ Vdc
5	Q_1, Q_4, Q_5	$V_6(0,0,1)$	$-\frac{1}{3}$ Vdc	$-\frac{1}{3}$ Vdc	$\frac{2}{3}$ Vdc
6	Q_1, Q_4, Q_5	$V_7(1,0,1)$	$\frac{1}{3}$ Vdc	$-\frac{2}{3}$ Vdc	$\frac{1}{3}$ Vdc
7	Q_1, Q_3, Q_5	$V_8(1,1,1)$	0	0	0

TABLE II
HARDWARE RESOURCES EMPLOYED IN REAL-TIME SIMULATION

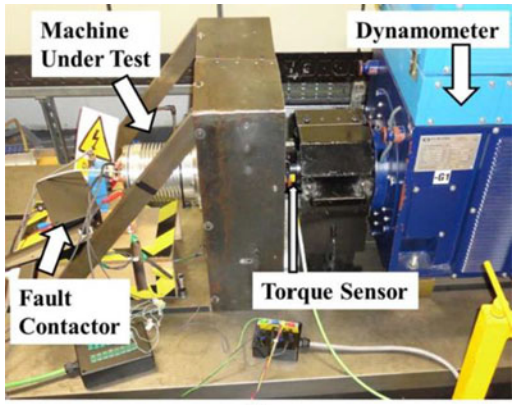
Resources	Slice registers	Slice LUTs	Block RAMs	DSP48 blocks
Total	7235/184 304	14622/92 152	265/268	166/180
emulator	3.9%	15.9%	98.9%	92.2%
DQ to ABC	1039/184 304	794/92 152	0/268	4/180
transformation	0.6%	0.9%	0%	2.2%
Current maps	1218/184 304	1646/92 152	265/268	0/180
and interpolation	0.7%	1.8%	98.9%	0%
Flux	1668/184 304	1487/92 152	0/268	16/180
equations	0.9%	1.6%	0%	8.9%
Angle	1675/184 304	2074/92 152	0/268	30/180
calculation	0.9%	2.3%	0%	16.7%
Output	1617/184 304	1617/92 152	0/268	1/180
and measure	0.9%	1.8%	0%	0.6%

TABLE III
NUMBER OF CYCLES AND RATE OF EXECUTION OF REAL-TIME SIMULATION

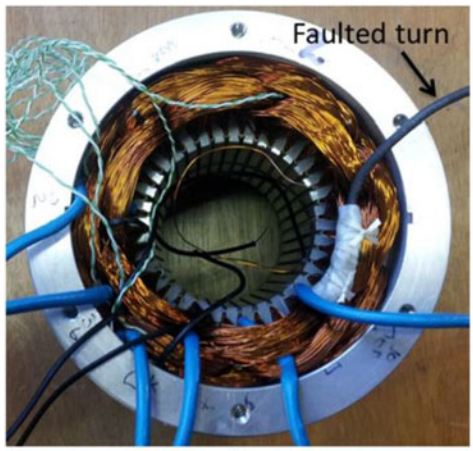
Cycles and execution	Number of cycles	Rate of execution
DQ to ABC transformation	10	250 ns
Current maps and interpolation	50	1.25 μs
Flux equations	8	200 ns
Angle calculation	43	1.075 μs
Output and measure	349	8.725 μs

rate of execution is determined by the slowest, i.e., the current interpolation that requires 1.25 μs. Digital to analog conversion for outputting current waveforms is executed in parallel at 115 kS/s as limited by the available digital-to-analog converter (DAC). Faster DACs can in principle be used.

The proposed method based on interpolation over 4-D LUTs result in significantly shorter execution time compared with iterative methods required for solving the nonlinearities resulting from iron saturation effects. As an example, several hundreds μs with a 100-MHz clock are required in [7] for solving the nonlinear PN with an iterative Newton–Raphson algorithm. Similar latencies to those shown in Table III are reported in other publications that use analytical models or LUTs, e.g., [10], [11], and [15].



(a)



(b)

Fig. 6. (a) Experimental setup and (b) stator winding with interturn short-circuit fault in phase C.

IV. EXPERIMENTAL SETUP

Extensive experimental validations against the prototype machine have been performed using the dynamometer test rig, as shown in Fig. 6(a).

The prototype interior permanent-magnet (IPM) machine used for validation is based on the design described in Section III. The machine stator windings shown in Fig. 6(b) allow for the short circuiting of two turns in phase C through external contactors for emulation of the interturn fault. In particular, a three-phase contactor connected to the faulted turns was triggered using a timer circuit tor turn for a relatively short time in the range of hundreds of milliseconds to prevent any machine damage due to overheating. The extra resistance added by the contactor and cabling has been included in the model and adds up to approximately 5.5 mΩ.

V. VALIDATION RESULTS

Validation of the proposed model is performed with the machine driven at constant speed by the dynamometer and operating as generator supplying a three-phase resistive load. Fault transient tests have been performed in a wide range of operating conditions. As an example, Fig. 7 shows the fault current at 3500 r/min on a 2.2-Ω load. The comparison between FE sim-

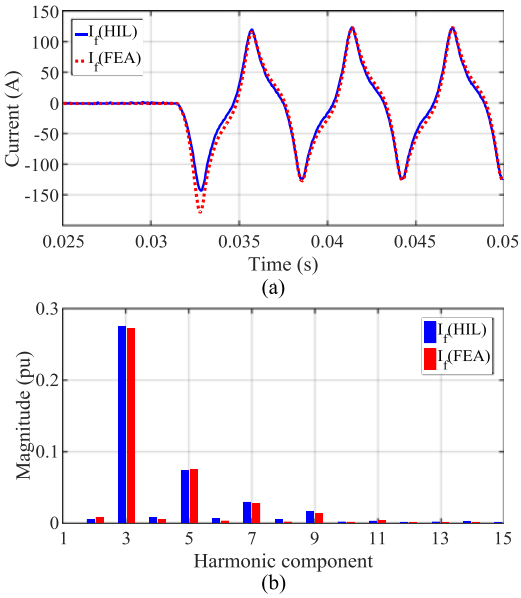


Fig. 7. Transient (a) time-domain comparison of FEA and HIL fault currents and (b) fast Fourier transform (FFT) comparison at 3500 r/min and 2.2-Ω load.

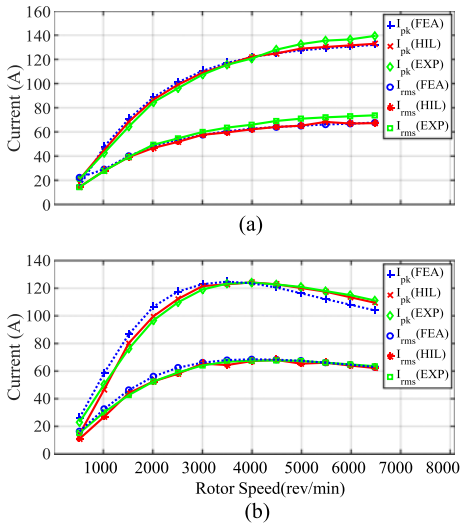


Fig. 8. Comparison of FE-based simulation, HIL, and experimental (EXP) rms and peak fault current values at various speeds at (a) no load (b) 2.2-Ω load.

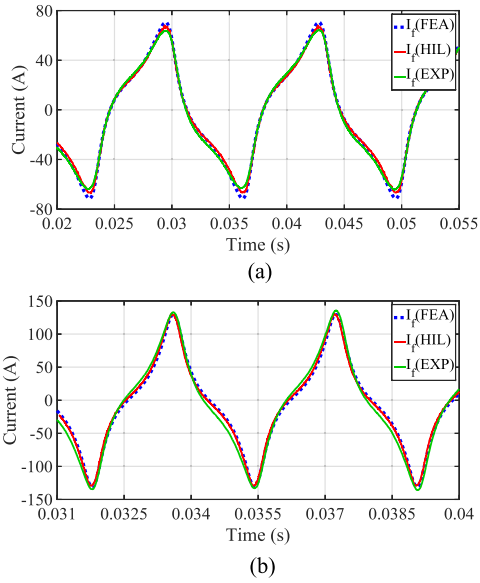


Fig. 9. Comparison of FE-based simulation, HIL, and experimental (EXP) fault currents at (a) 1500 r/min and no load and (b) 5500 r/min and no load.

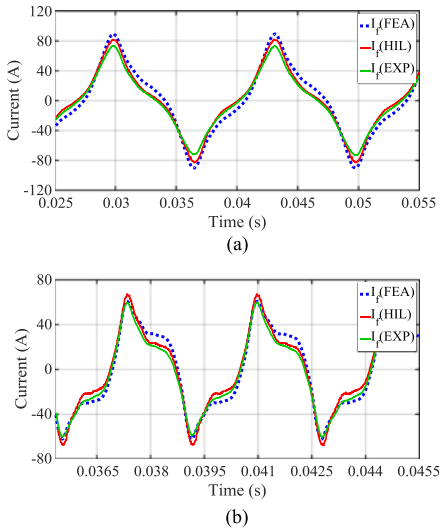


Fig. 10. Comparison of FE-based simulation, HIL, and experimental (EXP) fault currents at (a) 1500 r/min and 0.69-Ω load, and (b) 5500 r/min and 0.69-Ω load.

ulation and the results from the real-time HIL implementation is presented both in time and frequency domain, as shown in Fig. 7(a) and (b), respectively, showing an excellent agreement.

Peak and rms fault current results are compared for different speeds ranging from 500 to 6500 r/min and three different load conditions, as shown in Fig. 8. In general, a good match between finite element analysis (FEA), HIL, and experimental results is shown, with a maximum error below 15% occurring at lower rotor speeds and lower load resistance. The main cause of error is the poor repeatability of the contactor resistance, which varies from 2 to 2.5 mΩ (25% variation) at different contactor closures during the experiments. At lower speeds, the resistive component dominates the overall fault impedance compared with higher speeds, where the dominating contributor is inductance. Figs. 9 and 10 show measured and simulated fault current waveforms in four different conditions at rotor speeds of 1500 and 5500 r/min under no load and at 0.69-Ω load, respectively. Figs. 11 and 12 show comparisons in *d*- and *q*-axis current ripples in two different operating conditions at 5500 and 3500 r/min, respectively, confirming the good agreement between the proposed real-time modeling and the experimental measurements.

VI. Application

In order to demonstrate the application of the proposed real-time emulation to the development and test of fault detection

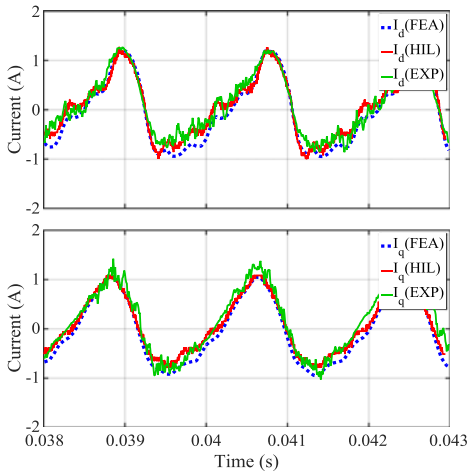


Fig. 11. Comparison of FE-based simulation, HIL, and experimental (EXP) *dq*-axes currents at 5500 r/min and 2.2-Ω load.

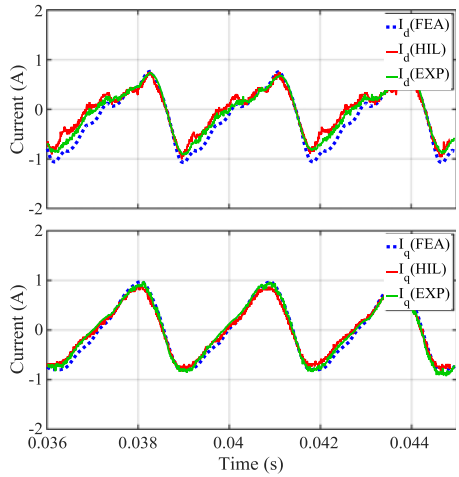


Fig. 12. Comparison of FE-based simulation, HIL, and experimental (EXP) *dq*-axes currents at 3500 r/min and 2.2-Ω load.

strategies, two fault transients cases are presented here. Fig. 13 shows the output currents following the interturn short-circuit fault when the machine is operated in generator mode supplying a 2.2-Ω resistive load. A frequency domain analysis of current in phase C, as shown in Fig. 14, demonstrates the potential application of a fault detection indicator based on tracking of the third harmonic in phase currents [30]. Although many different fault detection techniques exist in the literature [3], simple strategies as previously mentioned may be used as a proof of application. The purpose here is not to propose a novel fault detection method, but to provide a practical application example of the proposed emulation tool for the development of fault detection and classification strategies.

Similarly, Figs. 15 and 16 show a transient following the interturn short-circuit fault when the virtual machine is operated in motoring mode, driven by a virtual inverter operating at 10-kHz switching frequency and controlled with standard field-oriented control (FOC) using the platform on the left of Fig. 3.

The controller has been implemented on an NI sb-RIO platform based on Xilinx Zynq-7010 SoC. The interface between

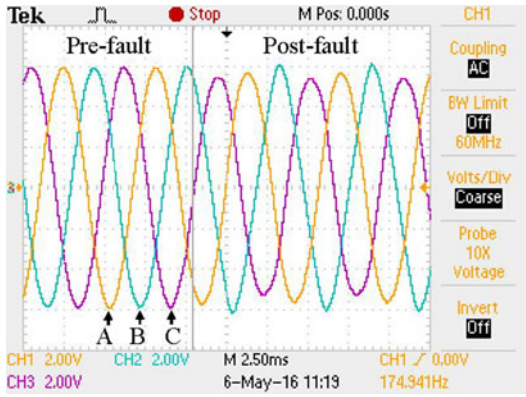


Fig. 13. Generator mode three-phase currents before and after the fault. Scale: 5 A/div.

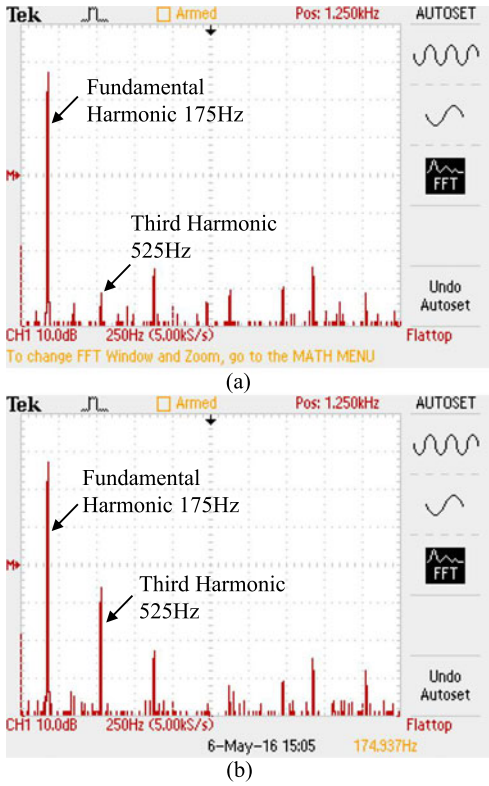


Fig. 14. Generator mode FFT of the faulted phase current I_c (a) before and (b) after the fault.

the emulator and the controller under test consist of two analog channels for phase currents, six digital I/Os for PWM signals, and eight bits digital outputs for angle position feedback.

Due to their relatively high bandwidth, the proportional–integral (PI) current controllers partially compensate for the distortion following the fault, making current signature-based fault detection more difficult. A potentially more robust fault detection method based on the extraction of the second harmonic in the *q*-axis current [31] has also been implemented using a single-frequency Fourier series tracking algorithm schematically illustrated in Fig. 17. The resulting fault indicator is shown in Fig. 18.

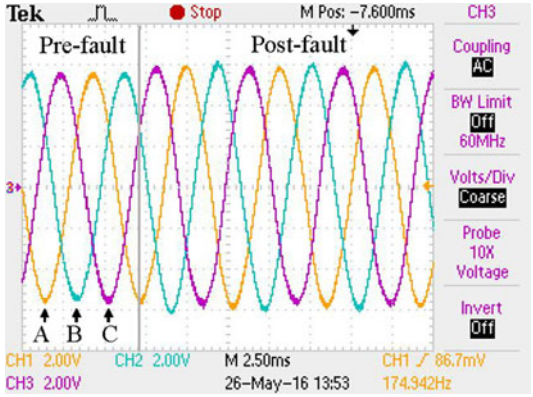


Fig. 15. Motoring mode three-phase currents before and after the fault. Scale: 5 A/div.

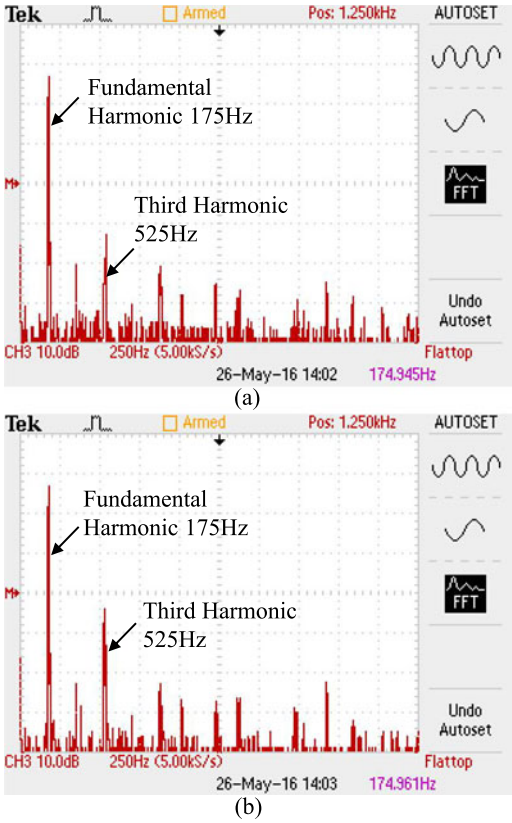


Fig. 16. Motoring mode FFT of the faulted phase current I_c (a) before and (b) after the fault appears.

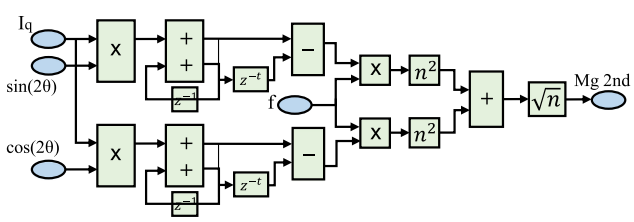


Fig. 17. Single-frequency Fourier series second harmonic component magnitude monitoring algorithm.

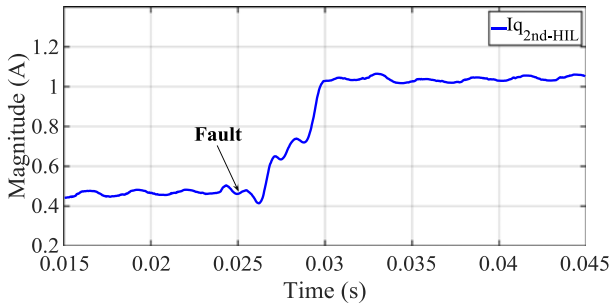


Fig. 18. *q*-axis current second harmonic component magnitude before and after the fault.

The postfault increase of third harmonics in phase currents results in an increase in the second harmonics in the synchronous *dq*- reference frame currents.

VII. Conclusion

This paper presented the real-time implementation of a high-fidelity model of PMSMs under both healthy and faulty conditions. In particular, the proposed real-time modeling was suitable for HIL development and tests of motor controllers and was capable of accurately representing machines both in healthy conditions and with stator winding interturn faults. Detailed description of modeling and its real-time hardware implementation on an FPGA platform was discussed, including implications on FPGA resources and execution time. Extensive experimental validation in a range of operating conditions, including several fault scenarios, was presented, demonstrating the accuracy of the proposed real-time modeling. Potential applications to the development of fault detection strategies were highlighted and demonstrated through practical examples.

The proposed HIL modeling framework represents a valuable platform for the development of drive control algorithms. The proposed method for modeling of stator faults provides a novel tool for developing fault detection and diagnostic algorithms in a safe and relatively inexpensive environment, in realistic operating conditions, and without significant loss of accuracy.

The model could also be further refined to account for thermal effects as well as additional fault conditions such as partial demagnetization and faults in inverter and sensors.

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