FPGA-Based Experimental Investigation of a Quasi-Centralized Model Predictive Control for Back-to-Back Converters

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***Abstract*—Voltage source back-to-back power converters are widely used in grid-tied applications. This paper presents a quasi-centralized direct model predictive control (QC-DMPC) scheme for back-to-back converter control without a dc-link outer-loop controller. Furthermore, the QC-DMPC is experimentally compared with a conventional proportional-integration (PI) dc-link controller-based DMPC (PI-DMPC) scheme. For the QC-DMPC scheme, the dc-link voltage is directly controlled by a grid-side predictive controller using a dynamic reference generation concept and load-side power estimation. For the PI-DMPC scheme, the dc-link voltage is controlled by an external PI controller. Both schemes are implemented on a field programmable gate array (FPGA)-based platform. Effectiveness of the proposed QC-DMPC is verified by both simulation and experimental data. Moreover, FPGA implementation issues (resource usage and timing information), dc-link control performance, and robustness to parameter variation of the two DMPC schemes are compared in detail. The results emphasize that the QC-DMPC may outperform the PI-DMPC scheme in normal operation but with a slightly higher usage of FPGA resources. However, PI-DMPC scheme is more robust when parameter variations are considered.**

***Index Terms*—Back-to-back converter, dc-link control, field programmable gate array (FPGA), proportional-integration (PI) dc-link controller-based DMPC (PI-DMPC), quasi-centralized direct model predictive control (QC-DMPC).**

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I. Introduction

BACK-TO-BACK voltage source power converters with grid-tied active-front-end (AFE) rectifier offer many advantages [1], [2], such as: bidirectional power flow, adjustable dc-link voltage, and a sinusoidal grid-side current with adjustable active and reactive power. This topology is widely employed in advanced drive systems and grid-tied renewable energy interfaces [3], [4].

Recently, four groups of schemes have been reported to control a back-to-back converter [5], [6]: 1) cascaded current control with modulator, 2) direct control with switching table; 3) direct control with modulator, and 4) model predictive control (MPC). Within MPC schemes, direct model predictive control (DMPC) [also named as finite-control-set model predictive control (FCS-MPC)] has received much attention. It exploits the finite switching states of power converters and combines current (torque) or power control and modulation into one computational step. Apart from fast dynamics, multiple nonlinear constraints can easily be included into the controller design by an appropriate cost function. Research on DMPC has spread out across various fields, for instance, renewable energy systems, matrix and multilevel converters, and motor drives [7]–[11].

In practice, heavy computational effort is an obstacle for applying DMPC schemes. Therefore, field programmable gate arrays (FPGAs) are more widely used [12], [13]. Thanks to their parallel processing capability, FPGA-based real-time systems achieve a much shorter calculation time. Besides, FPGA techniques potentially offer a more stable and cheaper system-on-the-chip level solution. Current FPGA program design environments have become more convenient and efficient than ever before, which allows for the use of high-level programming languages (e.g., Labview-FPGA) or coder generation (e.g., Matlab/Simulink). Thus, it is reasonable to predict that FPGA techniques will be even more widely used in power electronics and drive systems in the future.

DC-link voltage control represents a key part of back-to-back power converter-based systems. In [14], a feedback linearization scheme is first proposed for controlling the dc-link voltage of a back-to-back system with an extremely small dc-link capacitor. In [15], a similar feedback linearization idea is used for controlling a grid-tied AFE. In [16], a nonlinear controller that uses a new complex state-space modeling method is proposed and verified against a grid-tied AFE. In [17], the dc-link control is fulfilled by using a proportional-integration (PI)

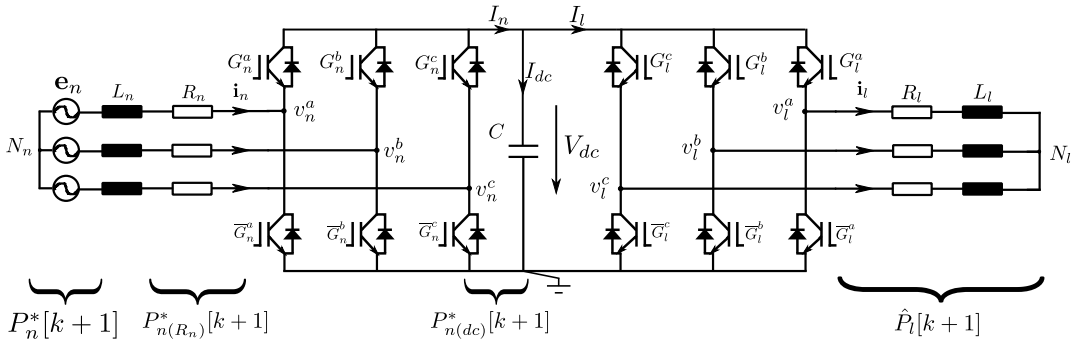


Fig. 1. Simplified power circuit of a voltage source back-to-back converter with *L* filter and *RL* load.

controller, which generates the reference for grid-side inner predictive power controller. For steady state, the dc-link voltage and grid-side active power are controlled nicely. However, a typical second-order fluctuation of sizable magnitude is observed during system transient phases. In [18], by using a dynamic reference generation concept, the dc-link voltage control is directly included into the grid-side predictive controller for a grid-tied AFE with a dc-link R-Load. In [19], a similar idea is applied to a diode clamped multilevel back-to-back converter-based AC motor drive system with only simulation results.

The comprehensive relation and performance comparison provide a platform not only to transform from one to another, but also to develop different dc-link controllers. Therefore, many efforts have been made to compare and study the different methods aforementioned. In [20], a state feedback control is analyzed and compared with a conventional cascaded control scheme for a single-phase ac/dc converter with respect to dc-link control; while in [21], the linear and nonlinear control strategies of a back-to-back converter with respect to dc-link voltage control is compared. However, few publications compare conventional PI controller and the newly proposed dynamic reference generation concept with regards to dc-link voltage control. This study further extends the dynamic reference generation concept proposed by [18] into a voltage source back-to-back power converter by feeding the load-side estimated power forward into a dc-link dynamic reference generator, resulting in a quasi-centralized direct model predictive control (QC-DMPC) scheme. The effectiveness of the QC-DMPC scheme is verified by *both* simulation *and* experimental results. Furthermore, dc-link voltage control performance and robustness under parameter variations are compared between the QC-DMPC and PI-DMPC schemes experimentally. The main contributions of this study are:

1) a quasi-centralized DMPC scheme (QC-DMPC) for controlling a back-to-back converter by using a dynamic reference generation concept and load-side power estimation is proposed and experimentally verified;
2) a thorough comparison between the conventional PI-DMPC and the proposed QC-DMPC is presented for the first time using both simulation and experimental data;
3) both schemes are implemented using a platform that is entirely based on FPGA. The implementation, timing, and FPGA resource usages are introduced in detail.

This paper is structured as follows: in Section II, the system predictive model is developed; in Section III, the principles of DMPC are revisited, and the conventional PI-DMPC scheme and a QC-DMPC scheme are presented. The FPGA implementation and comparison of these two schemes are detailed in Section IV. In Section V, simulation and experimental results are presented and analyzed. Finally, Section VI concludes this paper.

II. System Description and Modeling

A two-level voltage source back-to-back power converter is shown in Fig. 1. In this section, it is modeled (in orthogonal $\alpha\beta$ frame) [5].

A. Grid (Net) and Load-Side Current Dynamics

$$\frac{d\vec{i}_n^{\alpha\beta}}{dt} = \frac{1}{L_n}[\vec{e}_n^{\alpha\beta} - \vec{v}_n^{\alpha\beta}] - \frac{R_n}{L_n}\vec{i}_n^{\alpha\beta} \tag{1}$$

$$\frac{d\vec{i}_l^{\alpha\beta}}{dt} = \frac{1}{L_l}\vec{v}_l^{\alpha\beta} - \frac{R_l}{L_l}\vec{i}_l^{\alpha\beta} \tag{2}$$

where $\vec{i}_x^{\alpha\beta}$ and $\vec{v}_x^{\alpha\beta}$ are current and converter voltage vectors (x can be l or n, representing the load and grid sides, respectively); $\vec{e}_n^{\alpha\beta}$ is the grid-side source voltage vector. $\vec{v}_x^{\alpha\beta}$ is a function of switching vector $\vec{G}_x^{\mathrm{abc}}$ and dc-link voltage V_{dc}. It is given by [5]

$$\vec{v}_x^{\alpha\beta} = \sqrt{\frac{2}{3}} \cdot V_{\mathrm{dc}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \vec{G}_x^{\mathrm{abc}} \tag{3}$$

where $\vec{G}_x^{\mathrm{abc}} = [G_x, G_x, G_x]^T, G_x \in \{0, 1\}$.

B. Power and DC-Link Voltage Dynamics

The grid-side power $\vec{S}_n$ can be modeled in complex form by [22]

$$\vec{S}_n = P_n + jQ_n = \vec{e}_n^{\star\alpha\beta} \cdot \vec{i}_n^{\alpha\beta} \tag{4}$$

where * represents the conjugate operation of a vector and P_n and Q_n are the active and reactive power, respectively.

Assuming that the grid-side source voltage $\vec{e} = Ae^{j\omega_n t}$ with A and ω_n being the magnitude and frequency, respectively, then $\frac{d\vec{e}}{dt} = j\omega_n\vec{e}$. So the dynamics of the grid-side power can be

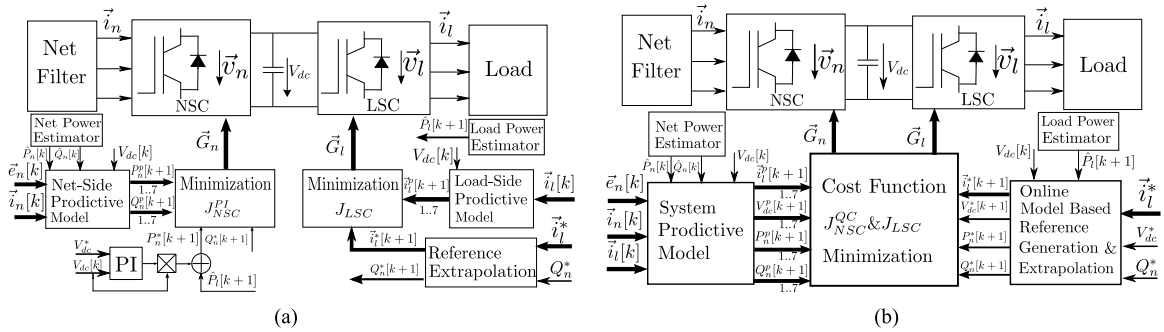


Fig. 2. Control structure of PI-DMPC and QC-DMPC. (a) PI dc-link based DMPC structure. (b) Dynamic reference generation-based DMPC structure.

obtained by

$$\frac{d\vec{S}_n}{dt} = \frac{1}{L_n}[(A^2 - \vec{v}_n^{\star\alpha\beta} \cdot \vec{e}_n^{\alpha\beta}) - (R_n - j\omega_n \cdot L_n)\vec{S}_n] \quad (5)$$

therefore, the active and reactive power dynamics are

$$\frac{dP_n}{dt} = \frac{1}{L_n}[A^2 - \Re(\vec{v}_n^{\star\alpha\beta}\vec{e}_n^{\alpha\beta})] - \frac{R_n}{L_n}P_n - \omega_n Q_n \quad (6)$$

$$\frac{dQ_n}{dt} = -\frac{1}{L_n}\Im(\vec{v}_n^{\star\alpha\beta}\vec{e}_n^{\alpha\beta}) - \frac{R_n}{L_n}Q_n - \omega_n P_n \quad (7)$$

where $\Re\{X\}$ and $\Im\{X\}$ are the real and imaginary parts of X, respectively.

Considering the current flow, the dc-link dynamic is

$$\frac{dV_{\rm dc}}{dt} = \frac{1}{C}I_{\rm dc} = \frac{1}{C}[I_n - I_l] \quad (8)$$

where $I_n = \vec{i}_n^{\rm abc} \cdot \vec{G}_n^{\rm abc}$ and $I_l = \vec{i}_l^{\rm abc} \cdot \vec{G}_l^{\rm abc}$ (see Fig. 1).

C. System Prediction Model

For applying DMPC, the prediction model containing the control variables in discrete format is required. Using a small enough sampling interval T_s (i.e., $T_s \ll 1[s]$), the first-order Euler approximation method of $\frac{dX}{dt} = \frac{X[k+1]-X[k]}{T_s}$ (with k being the sampling instant) can be reasonable [23], [24]. Therefore, the discrete system prediction model is

$$\vec{i}_l^{\alpha\beta}[k+1] = k_{1l} \cdot \vec{i}_l^{\alpha\beta}[k] + k_{2l} \cdot \vec{v}_l^{\alpha\beta}[k] \quad (9)$$

$$P_n[k+1] = k_{1n} \cdot P_n[k] + k_{2n} \cdot \{A^2 - \Re(\vec{v}_n^{\star\alpha\beta}[k] \cdot \vec{e}_n^{\alpha\beta}[k])\} - k_{3n} \cdot Q_n[k] \quad (10)$$

$$Q_n[k+1] = k_{1n} \cdot Q_n[k] - k_{2n} \cdot \Im(\vec{v}_n^{\star\alpha\beta}[k] \cdot \vec{e}_n^{\alpha\beta}[k]) + k_{3n} \cdot P_n[k] \quad (11)$$

$$V_{\rm dc}[k+1] = V_{\rm dc}[k] + k_{1dc} \cdot (I_n[k] - I_l[k]) \quad (12)$$

where $k_{1l} = (1 - \frac{R_l T_s}{L_l})$,$k_{2l} = \frac{T_s}{L_l}$, $k_{1n} = 1 - \frac{R_n T_s}{L_n}$, $k_{2n} = \frac{T_s}{L_n}$, $k_{3n} = \omega_n T_s$, and $k_{1\rm dc} = \frac{Ts}{C}$.

III. Control Algorithms

A. DMPC in General

A general DMPC (FCS-MPC) scheme simply evaluates a given cost function

$$J_{\rm DMPC}(\vec{s}_x) = \underbrace{\gamma_{{\rm TS}_x}|{\rm TS}_x^* - {\rm TS}_x^p(\vec{s}_x)|}_{=:J_{{\rm TS}_x}} + \underbrace{\gamma_{{\rm CS}_x}|{\rm CS}_x^* - {\rm CS}_x^p(\vec{s}_x)|}_{=:J_{{\rm CS}_x}} \quad (13)$$

for each switching state $\vec{s}_x$ of a finite admissible set $\mathcal{S}$ by using a prediction model. The subscript x stands for load l or grid/net n side and X^* represents the reference value of X. The cost function comprises two parts: $J_{{\rm TS}_x}$ and $J_{{\rm CS}_x}$, with their weighting factors of $\gamma_{{\rm TS}_x}$ and $\gamma_{{\rm CS}_x}$. $J_{{\rm TS}_x}$ represents subcosts for the *Target Set* ${\rm TS}_x$ (such as: reference tracking of current, or power, with their references being ${\rm TS}^*$). $J_{{\rm CS}_x}$ represents subcosts for the *Constraint Set* ${\rm CS}_x$ (such as: power or voltage/currents constraints, with their references being ${\rm CS}_x^*$). For a two-level converter, the switching vector $\vec{s}_x$ is chosen from the set

$$\vec{s}_x \in \mathcal{S} := \{000, 001, \ldots, 110, 111\} \quad (14)$$

of *eight admissible switching vectors*. The algorithm is given as pseudocode in Algorithm I. $M_{{\rm TS}_x}$ *and* $M_{{\rm CS}_x}$ are abbreviations for the *prediction model for the Target Set* TS_x and the *prediction model for the Constraint Set* CS_x, respectively. Meanwhile $f_{{\rm TS}_x}^{\rm ref}$ *and* $f_{{\rm CS}_x}^{\rm ref}$ stand for the reference generation or extrapolation mechanisms for Target Set ${\rm TS}_x$ *and* Constraint Set ${\rm CS}_x$, respectively.

Algorithm I: DMPC (FCS-MPC) Algorithm with $\vec{s}_x \in \mathcal{S}$ (eight switching vectors)

Step I: State prediction *and* state reference generation or extrapolation:
$\{ {\rm TS}_x^p(\vec{s}_x) = M_{{\rm TS}_x}(\vec{s}_x)$ and ${\rm CS}_x^p(\vec{S}_x) = M_{{\rm CS}_x}(\vec{s}_x)\}$
and $\{{\rm TS}_x^* = f_{{\rm TS}_x}^{\rm ref}({\rm TS}_x)$ and ${\rm CS}_x^* = f_{{\rm CS}_x}^{\rm ref}({\rm CS}_x)\}$
Step II: Cost evaluation and selection of optimal switching vector:
$\{ \vec{s}_x^* = \arg\min_{\vec{s}_x \in \mathcal{S}} J_{\rm DMPC}(\vec{s}_x)$ with $J_{\rm DMPC}$ as in (13) $\}$
Step III: Application of optimal gate signal vector:
$\vec{G}_x = \vec{G}_x(\vec{s}_x^*)$

The main control objectives for a back-to-back converter shown in Fig. 1 are: 1) load-side current tracking, 2) dc-link voltage control, and 3) grid-side power control. The system must operate under certain current and power limits and constraints. In the following parts of this section, a conventional PI dc-link controller-based DMPC (PI-DMPC) scheme [see Fig. 2(a)] and a proposed quasi-centralized DMPC (QC-DMPC) scheme [see Fig. 2(b)] are introduced. For simplicity, the introduction of the two schemes follows the order of *Step II* to *Step I*, in *Algorithm I*.

B. PI DC-Link Controller-Based DMPC Scheme[17]

1) Cost Function Design: The cost functions that represent the control objectives of the load and grid side aforementioned are introduced as follows.

a) Load-Side Cost Function:

$$J_{\mathrm{LSC}} = \underbrace{\gamma_{i_l^\alpha}\left|i_l^{\alpha *}[k+1]-i_l^{\alpha p}[k+1]\right|+\gamma_{i_l^\beta}\left|i_l^{\beta *}[k+1]-i_l^{\beta p}[k+1]\right|}_{=:J_{\mathrm{TS_{LSC}}}} + \underbrace{\gamma_{\mathrm{CS}}^{i_l}\begin{cases}0, & \sqrt{(i_l^{\alpha p}[k+1])^2+(i_l^{\beta p}[k+1])^2}\le i_{l\max}\\ 1, & \sqrt{(i_l^{\alpha p}[k+1])^2+(i_l^{\beta p}[k+1])^2}> i_{l\max}.\end{cases}}_{=:J_{\mathrm{CS_{LSC}}}} \tag{15}$$

b) Grid-Side Cost Function:

$$J_{\mathrm{NSC}}^{\mathrm{PI}} = \underbrace{\gamma_{P_n}^{\mathrm{PI}}\left|P_n^*[k+1]-P_n^p[k+1]\right|+\gamma_{Q_n}^{\mathrm{PI}}\left|Q_n^*[k+1]-Q_n^p[k+1]\right|}_{=:J_{\mathrm{CS_{NSC}}}^{\mathrm{PI}}} + \underbrace{\gamma_{\mathrm{CS}}^{S_n}\begin{cases}0, & \sqrt{(P_n^p[k+1])^2+(Q_n^p[k+1])^2}\le S_{n\max}\\ 1, & \sqrt{(P_n^p[k+1])^2+(Q_n^p[k+1])^2}> S_{n\max}\end{cases}}_{=:J_{\mathrm{CS_{NSC}}}^{\mathrm{PI}}} \tag{16}$$

where $J_{\mathrm{TS_{LSC}}}$ and $J_{\mathrm{TS_{NSC}}}^{\mathrm{PI}}$ represent the *Targeting Set* (here the current and power tracking) of load and grid side; $J_{\mathrm{CS_{NSC}}}^{\mathrm{PI}}$, $J_{\mathrm{CS_{LSC}}}$ represent the *Constraint Set* (here the current and power limits) for load and grid side, respectively; $\gamma_{i_l^\alpha}$, $\gamma_{i_l^\beta}$,$\gamma_{\mathrm{CS}}^{i_l}$, $\gamma_{P_n}^{PI}$, $\gamma_{Q_n}^{PI}$ and $\gamma_{\mathrm{CS}}^{S_n}$ (all >0), are the weighting factors; and $S_{n\max}>0$ and $i_{l\max}>0$ are power and current limits.

2) System State Prediction and Reference Generation/Extrapolation

a) System states prediction: For a PI-DMPC scheme (see, e.g., [17]), the system states that are necessary to predict are load-side currents $\vec{i}_l^{\,p\alpha\beta}[k+1]$, grid-side active power $P_n^p[k+1]$, and reactive power $Q_n^p[k+1]$, which are given by (9)–(11), respectively.

b) Reference generation/extrapolation: The purpose of reference generation is to obtain the future system reference values. The references required by (15) and ((16)) are: load-side currents $\vec{i}_l^{\,*\alpha\beta}[k+1]$, grid-side active power $P_n^*[k+1]$, and reactive power $Q_n^*[k+1]$. In practice, the load-side current and grid-side reactive power at the current sampling instant of $x[k]$, and past instants of $x[k-1]$ and $x[k-2]$ can be recorded, thus allowing the future reference values to be obtained with a second-order extrapolation scheme [10] of

$$x^*[k+1]=3(x^*[k]-x^*[k-1])+x^*[k-2] \tag{17}$$

where x can be $\vec{i}_l^{\,\alpha\beta *}$ or Q_n^*. The active power reference is produced by an outer dc-link PI controller by [See Fig. 2(a)]

$$P_n^*(t)=V_{\mathrm{dc}}(t)\cdot\mathcal{L}^{-1}\{T_{\mathrm{PI}}(s)*(V_{\mathrm{dc}}^*(s)-V_{\mathrm{dc}}(s))\}+\hat{P}_l(t) \tag{18}$$

with $T_{\mathrm{PI}}(s)=\frac{K_p\cdot s+K_i}{s}$, where $\mathcal{L}^{-1}$ represents the inverse Laplace transformation, and $\hat{P}_l(t)$ is the estimated active power of the load side [see (23)]. Note that, with the presence of $\hat{P}_l(t)$ in (18), the power control forms a feed-forward structure, resulting in a much smaller dc-link voltage fluctuation during load change. The structure overview of PI-DMPC is given in Fig. 2(a).

C. Proposed QC-DMPC

1) Cost-Function Design: The load-side cost function for QC-DMPC scheme is, therefore, designed the same way as is given by (15), since the control objectives are same. However, the dc-link voltage for the proposed QC-DMPC is directly included into the grid-side predictive controller using a dynamic reference generation concept [18] and no outer PI control loop is required. The primary difference between this study and [18] is that work in [18] deals with an AFE with dc-link R load, and the load current is directly calculated through the measured dc-link voltage and the value of dc-link resistive load; this study deals with a back-to-back converter with *RL* load and the load-side current reflected at the dc-link part is obtained by using a load-side power estimation and a generated dc-link voltage reference [see (23) and (22)]. The cost function for the grid side is designed as

$$J_{\mathrm{NSC}}^{\mathrm{QC}} = \underbrace{\gamma_{P_n}^{\mathrm{QC}}|P_n^*[k+1]-P_n^p[k+1]|+\gamma_{Q_n}^{\mathrm{QC}}|Q_n^*[k+1] -Q_n^p[k+1]|+\gamma_{V_{\mathrm{dc}}}^{\mathrm{QC}}|V_{\mathrm{dc}}^*[k+1]-V_{\mathrm{dc}}^p[k+1]|}_{=:J_{\mathrm{TS_{NSC}}}^{\mathrm{QC}}} + \underbrace{\gamma_{\mathrm{CS}}^{S_n}\begin{cases}0, & \sqrt{(P_n^p[k+1])^2+(Q_n^p[k+1])^2}\le S_{n\max}\\ 1, & st\sqrt{(P_n^p[k+1])^2+(Q_n^p[k+1])^2}> S_{n\max}.\end{cases}}_{=:J_{\mathrm{CS_{NSC}}}^{\mathrm{QC}}} \tag{19}$$

2) System State Prediction and Reference Generation/Extrapolation:

a) System state ($\mathrm{TS^p}, \mathrm{CS^p}$) prediction: For the QC-DMPC scheme, the system states to predict are load-side currents $\vec{i}_l^{\,p\alpha\beta}[k+1]$, grid-side active power $P_n^p[k+1]$, reactive power $Q_n^p[k+1]$, and the dc-link voltage $V_{\mathrm{dc}}^p[k+1]$, which are obtained by (9)–(12), respectively.

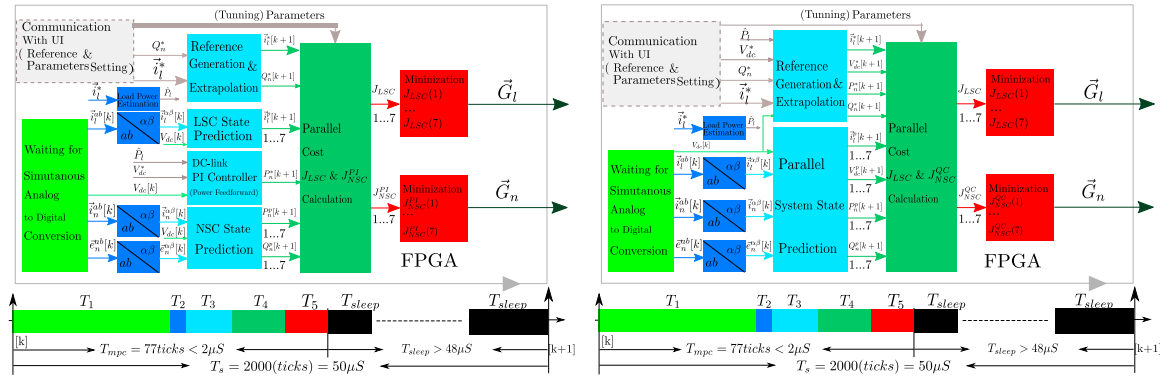


Fig. 3. FPGA implementation overview of PI-DMPC and QC-DMPC schemes. (a) FPGA implementation details of PI-DMPC. (b) FPGA implementation details of QC-DMPC.

TABLE I
FPGA DESIGN DETAIL

Timing	PI-DMPC	QC-DMPC	Resources	PI-DMPC	QC-DMPC
T_1	40 ticks	40 ticks	Slices	2755	2792
T_2	1 tick	1 tick	Reg.	1690	1710
T_3	7 ticks	9 ticks	LUTs	1838	1864
T_4	19 ticks	19 ticks	DSP48s	48	54
T_5	8 ticks	8 ticks			
T_s	50 μs	50 μs			
T_{mpc}	≤ 2 μs	≤ 2 μs			
T_{sleep}	≥ 48 μs	≥ 48 μs			

b) Reference generation/extrapolation: The same method for the load-side current and grid-side reactive power reference generation used in PI-DMPC scheme is again adopted for QC-DMPC [see (17)]. The dc-link voltage reference $V_{\mathrm{dc}}^*[k+1]$ and grid-side active power reference $P_n^*[k+1]$ are obtained here using a dynamic reference generation concept and load-side power estimation. The details are explained below.

(i) DC-link voltage reference generation: To obtain the *one step reference value* $V_{\mathrm{dc}}^*[k+1]$ of the dc-link voltage, a gradually approaching manner with a limited-step size is introduced by using $N_s(>1)$ to limit the charging and discharging current of the dc-link capacitor

$$V_{\mathrm{dc}}^*[k+1] := V_{\mathrm{dc}}[k] + \frac{1}{N_s}(V_{\mathrm{dc}}^* - V_{\mathrm{dc}}[k]) \tag{20}$$

where N_s defines how many control intervals it needs to reach the *general reference value* of V_{dc}^*.

(ii) Grid-side active power reference generation: Assuming that $V_{\mathrm{dc}}^*[k+1]$ is reached in the next sampling interval, the required capacitor charging (or discharging) current reference $I_{\mathrm{dc}}^*[k+1]$ can be calculated by

$$I_{\mathrm{dc}}^*[k+1] = \frac{C}{N_s T_s}(V_{\mathrm{dc}}^*[k+1] - V_{\mathrm{dc}}[k]). \tag{21}$$

By defining the estimated load-side current reflected at the dc-link part as $\hat{I}_l[k+1]$, the reference dc-link current on the grid side $I_n^*[k+1]$ can be calculated as

$$I_n^*[k+1] = I_{\mathrm{dc}}^*[k+1] + \hat{I}_l[k+1] \tag{22}$$

where in order to reduce the influences of the dc-link voltage measurement noises, $\hat{I}_l[k+1]$ in this study is calculated by $\hat{I}_l[k+1] = \frac{\hat{P}_l[k+1]+\hat{P}_l[k]}{V_{\mathrm{dc}}^*[k+1]+V_{\mathrm{dc}}[k]}$. The load-side power estimation $\hat{P}_l[k+1]$ is obtained by the proposed method of

$$\hat{P}_l[k+1] = \{(i_l^{\alpha *}[k+1])^2 + (i_l^{\beta *}[k+1])^2\} \cdot R_l. \tag{23}$$

The power reference $P_{n(\mathrm{dc})}^*[k+1]$ of the dc-link at grid side (see Fig. 1) can be calculated by (22) and (20) as

$$P_{n(\mathrm{dc})}^*[k+1] = I_n^*[k+1] \cdot V_{\mathrm{dc}}^*[k+1]. \tag{24}$$

By defining the power reference for the resistor at the grid-side filter as $P_{n(R_n)}^*[k+1]$ (see Fig. 1), the power reference $P_n^*[k+1]$ (see Fig. 1) to the grid-side predictive controller is

$$P_n^*[k+1] = P_{n(R_n)}^*[k+1] + P_{n(\mathrm{dc})}^*[k+1] \tag{25}$$

where $P_{n(R_n)}^*[k+1] = \frac{2R_n}{3A^2}\{(P_n^*[k+1])^2 + (Q_n^*[k+1])^2\}$.

Solving (25), the following is obtained:

$$P_n^{\mathrm{calc}*}[k+1] = \frac{3A^2}{4R_n} - \sqrt{\frac{9A^4}{16R_n^2} - \frac{3A^2}{2R_n} \cdot (P_{n(\mathrm{dc})}^*[k+1] + \frac{2R_n}{3A^2} \cdot (Q_n^*[k+1])^2}. \tag{26}$$

Note here, for safety concerns, the grid-side power reference has to be limited. To be more specific, the power reference $P_n^*[k+1]$ assigned to the predictive power controller is defined by the following function:

$$P_n^*[k+1] = \begin{cases} P_n^{\mathrm{calc}*}[k+1] & , \mid P_n^{\mathrm{calc}*}[k+1] \mid \leq P_n^{\max}[k+1] \\ P_n^{\max}[k+1] & , P_n^{\mathrm{calc}*}[k+1] > P_n^{\max}[k+1] \\ -P_n^{\max}[k+1] & , P_n^{\mathrm{calc}*}[k+1] < -P_n^{\max}[k+1]. \end{cases} \tag{27}$$

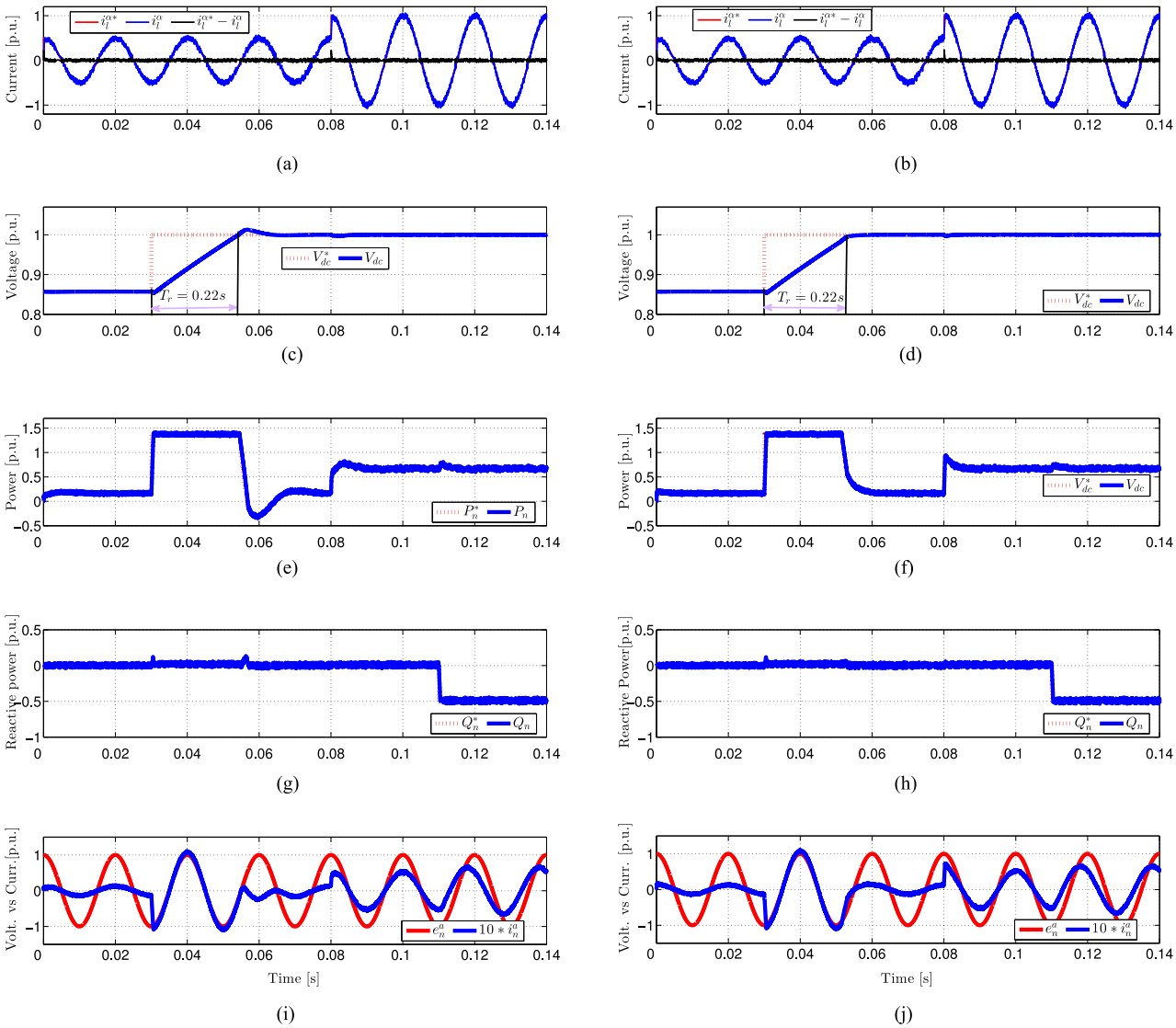


Fig. 4. Simulation results: performance comparison of PI-DMPC and QC-DMPC for a back-to-back converter. (a) Load-side current with PI-DMPC (base value, 20 A). (b) Load-side current with QC-DMPC (base value, 20 A). (c) DC-link voltage with PI-DMPC (base value, 700 V). (d) DC-link voltage with QC-DMPC (base value, 700 V). (e) Grid-side power with PI-DMPC (base value, 5000 VA). (f) Grid-side power with QC-DMPC (base value, 5000 VA). (g) Grid-side reactive power with PI-DMPC (base value, 5000 VA). (h) Grid-side reactive power with QC-DMPC (base value, 5000 VA). (i) Grid-side voltage and current with PI-DMPC (base value, 311 V/A). (j) Grid-side voltage and current with QC-DMPC (base value, 311 V/A).

TABLE II
SYSTEM CONFIGURATION

Parameters	Simulation	Experiment
Grid-side phase voltage e_{abc} [V] (peak)	250	70
Grid-side voltage frequency ω_n [rad/s]	100π	100π
Grid-side reactor resistor R_n [Ohm]	$1.56e-3$	$1.56e-3$
Grid-side reactor inductance L_n [H]	$16e-3$	$16e-3$
DC-link capacitor C [μF]	1100	1100
Load-side inductance L_l [H]	$10e-3$	$10e-3$
Load-side Resistor R_l []	10	10
Sampling frequency f_s [kHz]	20	20

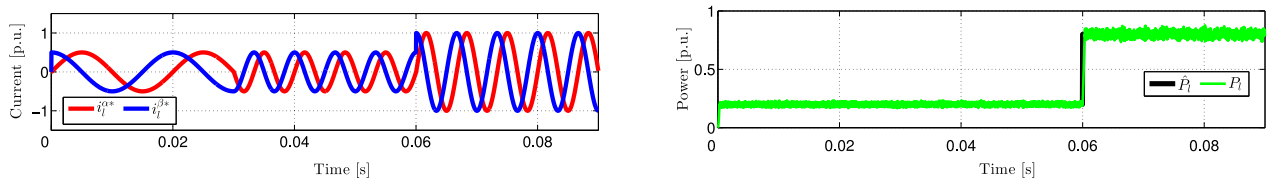
By defining the maximum grid-side power as $S_n^{\max}$ (obtained from the system hardware limits), the maximum admissible grid-side active power is calculated by

$$P_n^{\max}[k+1] = \sqrt{(S_n^{\max})^2 - (Q_n^*[k+1])^2}. \quad (28)$$

The overview structure of the proposed QC-DMPC is depicted in Fig. 2(b).

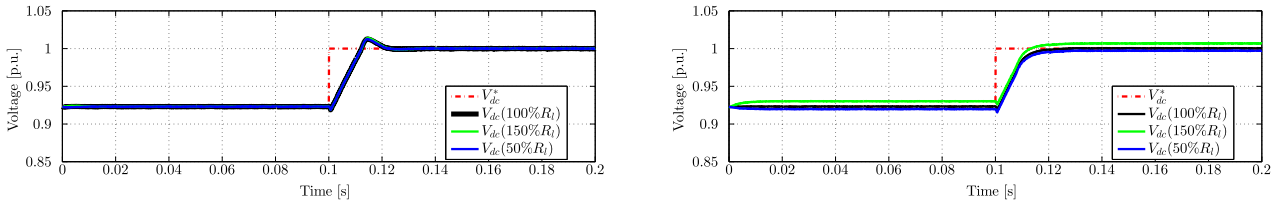
Some remarks on QC-DMPC and PI-DMPC schemes:

1) For the QC-DMPC scheme, theoretically no big over- or undershoot of the dc-link voltage will happen, which is due to: 1) the reference dc-link voltage is generated by using a gradually approaching manner [see (20)]. This leads to the *one-step-reference-value* [$V_{\mathrm{dc}}^*[k+1]$ in (20)] cannot be bigger (when positive) or smaller (when negative) than the *general-reference-value* [V_{dc}^* in (20)]. The *one-step-reference-value* is then tracked by the real value. 2) The power and current constraints are included inside



(a) (b)

Fig. 5. Simulation results: Load-side power estimation during load current changes. (a) Load-side current (base value, 20 A). (b) Load-side power estimation (base value, 8000 VA).



(a) (b)

Fig. 6. Simulation results: Robustness to system parameter (load resistor R_l) variation. (a) DC-link voltage control with PI-DMPC (base value, 650 V). (b) DC-link voltage control with QC-DMPC (base value, 650 V).

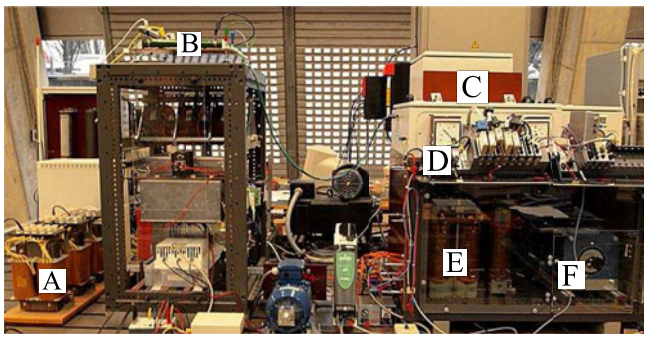


Fig. 7. Self-constructed Test-bench with (A) load-side inductance (L_l), (B) load-side resistor (R_l), (C) back-to-back two-level voltage source converter (constructed in the laboratory based on Infineon IGBT modules), (D) NI-cRIO FPGA-based controller, (E) Grid-side choke (inductance L_n and self-resistor R_n), and (F) grid-side Variac.

the cost function. So when the constraints are fully respected (by choosing a big enough weighting factor), no overlimit charging and discharging current occurs. Since big voltage over- or undershoot can be damaging to the dc-link capacitors, which are usually one of the most vulnerable parts of a real power converter. From this aspect, the QC-DMPC scheme is more suitable when considering the lifespan of the dc-link capacitors.

2) For the QC-DMPC scheme, at the dc-link part, only one parameter N_s is used; moreover, it can be chosen according to the specific charging or discharging current limit of the dc-link capacitor and the intended steps for reaching the dc-link voltage reference. This makes the tuning procedure considerably easier than PI-DMPC schemes.
3) The calculation of the dc-link and grid-side active power reference values involves all of the system parameters. The correct value of the load-side resistor is particularly important for the generated active power reference. Intuitively, the QC-DMPC scheme is more vulnerable to system parameter deviations. In terms of the computational efforts required, the QC-DMPC scheme is more demanding than the PI-DMPC scheme.
4) the selections of weighting parameters is still an open question, but there are some rule-of-thumbs (see, e.g., [25]). An "equal weighing" tuning method as is used in this paper is highly recommended due to its simplicity and effectiveness. "Equal weighting" means the targeted quantities [TS in (13)] are regarded as equally important, and the weighting factors for targeted quantities can be chosen with equal normalized value by

$$\frac{\gamma_i}{i_n} = \frac{\gamma_p}{p_n} \tag{29}$$

where γ_i and γ_p are the weightings for current and power, respectively. But for the constraints [CS in (13)], the weighting factors can be chosen with values big enough (exact requirements depends on the data type of the digital controller employed), to ensure all the constraints are respected.

IV. FPGA Implementation

In this study, an FPGA-based platform (NI-CRIO reconfigurable system) is employed to implement both control schemes. The implementation procedures, resource usage, and also the timing information are introduced in this section.

The overview of the FPGA implementations for the two schemes are depicted in Fig. 3, where different colors represent different calculation times. FPGA design implementation procedure is introduced here following the respective duration time of $T_1, T_2, \ldots, T_5, T_{\text{sleep}}$ in Fig. 3.

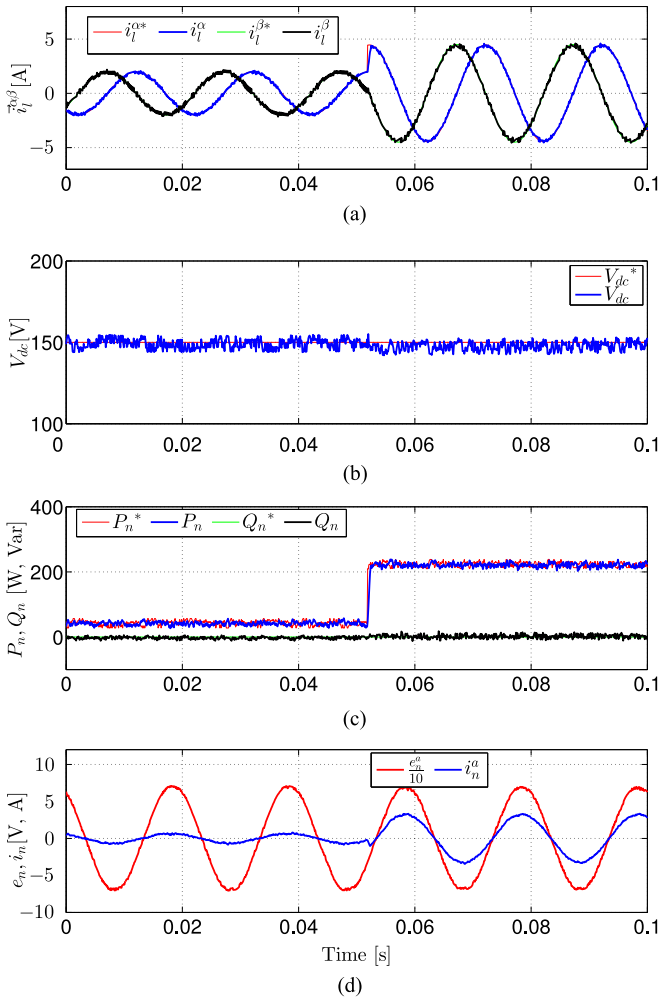


Fig. 8. Experimental results: performance of QC-DMPC for a back-to-back converter. (a) Load-side current: steady-state performance. (b) DC-link voltage control: transient-state performance. (c) Grid-side power: transient-state performance. (d) Grid-side voltage and current: transient-state performance.

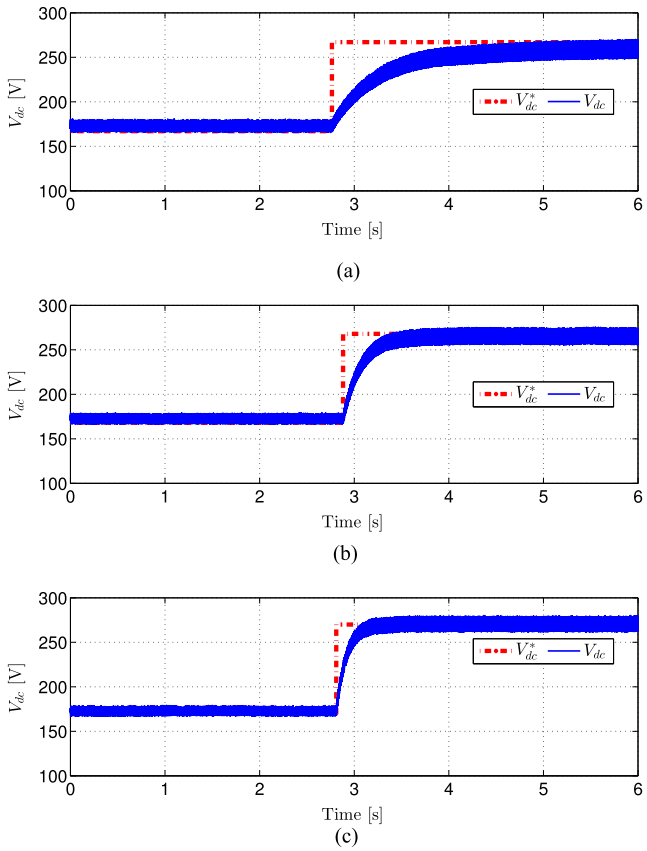


Fig. 9. Experimental results: effects of N_s for QC-DMPC. (a) Step changing of dc-link voltage: $N_s = 200$. (b) Step changing of dc-link voltage: $N_s = 160$. (c) Step changing of dc-link voltage: $N_s = 100$.

During T_1 (40 ticks, i.e., 1 μs)[1]: For both PI-DMPC and QC-DMPC, the analog-to-digital conversion (ADC) interface subroutine is executed and the feedback signals, which are $V_{\rm dc}$, $\vec{i}_l^{ab}$, $\vec{i}_n^{ab}$, and $\vec{e}_n^{ab}$, are obtained.

During T_2 (one tick): Measured signals of $\vec{i}_l^{ab}$, $\vec{i}_n^{ab}$, and $\vec{e}_n^{ab}$ are transformed into $\alpha\beta$ frame, using a so-called single-circle-timed-loop technique in parallel running subroutines. Meanwhile, the subroutine of load-side power estimation is executed in parallel, for both PI-DMPC and QC-DMPC (see Fig. 3).

During T_3 (seven ticks for PI-DMPC; nine ticks for QC-DMPC): 1) For PI-DMPC, the reference generation, load-side state prediction, dc-link PI controller, and grid-side state are implemented in parallel. Note that the heaviest parts in terms of computation are the load- and grid-state predictions which run in **seven ticks**. The PI controller itself only runs for **one tick** but a waiting routine (**six ticks**) is added for synchronizing purpose; 2) For QC-DMPC, the system-state prediction and reference generation subroutines are implemented in parallel and the time duration is **9 ticks**.

During T_4 and T_5 (19 ticks): For both schemes, the cost calculation (T_4) and minimization (T_5) parts are implemented in parallel in the same way, since no cross-interaction exists. For both, the durations of these two steps (cost calculation and minimization) are $T_4 = 19$ ticks and $T_5 = 8$ ticks.

During $T_{\rm sleep}$ (1925 ticks for PI-DMPC; 1923 ticks for QC-DMPC): For both schemes, this part represents the period from sending out the gate signals to the beginning of a new control interval.

Note that the total execution time including ADC conversion is 77 ticks for QC-DMPC, and 75 ticks for PI-DMPC. The calculation time is negligible compared to the whole sampling interval $T_s = 2000$ ticks. Therefore, the computation compensation is not necessary for either. Table I summarizes the timing and resource consuming issues of the two schemes.

V. Results and Analysis

A. Simulation Results

To verify the effectiveness of the proposed QC-DMPC scheme and also the dc-link voltage control comparison between the presented QC-DMPC and PI-DMPC schemes (for PI-DMPC, a conditional integration antiwindup PI strategy [26],

[1]The FPGA top-level clock is 40 MHz, and one 1tick $= \frac{1}{40\,\text{MHz}} = 25$ ns

[27] is used for a fair comparison), a simulative comparison in Matlab/Simulink environment is performed. The weighting parameters are obtained by using the equal-weighting method [see (29)] as: $\gamma_{i_l^\alpha}=1, \gamma_{i_l^\beta}=1, \gamma_{\text{CS}}^{i_l}=5000, \gamma_{P_n}^{\text{PI}}=1, \gamma_{Q_n}^{\text{PI}}=1, \gamma_{\text{CS}}^{S_n}=5000; \gamma_{P_n}^{\text{QC}}=1, \gamma_{Q_n}^{\text{QC}}=1, \gamma_{V_{\text{dc}}}^{\text{QC}}=\frac{V_{\text{dc}}}{S_n^{\max}}, \gamma_{\text{CS}}^{S_n}=5000.$ Note that, for a fair comparison, the parameters of the PI controller are tuned in a trial-and-error manner to reach a similar rising-time of T_r [$T_r \approx 0.22$ s, see Fig. 4(c) and (d)] as the QC-DMPC, and all the other conditions are set the same. The other parameters of the simulation are collected in Table II.

The simulation scenario is as follows: within the interval [0, 0.08]s, the load-side current reference has a frequency of 50 Hz and a magnitude of 10 A (peak). At $t = 0.03$ s, dc-link voltage reference steps up from 600 to 700 V (base value), whereas at $t = 0.08$ s, the current reference magnitude changes to 20 A. The reactive power changes from 0 to -3000 var at $t = 0.11$ s. The effectiveness of the proposed QC-DMPC scheme is illustrated in (b), (d), (f), (h), and (j) of Fig. 4. The two schemes demonstrate similar performance for the load-side current tracking [See Fig. 4(a) and (b)]. The power tracking performances during the steady state for both schemes are also identically good [see Fig. 4(e) and (f)]. However, the QC-DMPC scheme outperforms the PI-DMPC scheme in controlling the dc-link voltage, active power, and grid-side current during the transient state [see Fig. 4(c)–(j)]. For the PI controller, a typical second-order phenomenon is seen with noticeable over- and undershoot magnitudes [see the transient phases (around $t = 0.6$ s and $t = 0.8$ s) of Fig. 4(d) and (f)]. However, as expected, no over- or undershoot is observed for the QC-DMPC scheme. The load-side power estimation is an essential step for the proposed QC-DMPC scheme because the load-side power reflected at the dc-link part is required for calculating $I_n^*[k+1]$ [see (22)]. Simulation results in Fig. 5 confirm the effectiveness of the proposed load-side power estimation. The testing scenario is as follows: within the interval [0, 0.03]s, the load-side current reference has a frequency of 50 Hz and a magnitude of 10 A (peak). At $t = 0.3$ s, it changes from 50 to 150 Hz, then at $t = 0.06$ s the magnitude changes to 20 A (peak) [see Fig. 5(a)]. Clearly, the load-power estimation is working accurately during both magnitude and frequency changes [see Fig. 5(b)].

The robustness under parameter (load-side resistor) variations of the two schemes is also compared in the simulation. The results in Fig. 6 emphasize that PI-DMPC is less sensitive to parameter variation than QC-DMPC: for QC-DMPC, when changing the load-side resistor (to 150% and 50% of its measured value), noticeable dc-link voltage steady-state errors are seen [see Fig. 6(b)]; while for PI DMPC, neither transient nor steady-state performances are (evidently) affected by changing R_l [see Fig. 6(a)].

B. Experimental Results

Experimental verification of the proposed QC-DMPC scheme and its performance comparison with PI-DMPC are carried out on a self-constructed test bench (see Fig. 7). For the test bench, the only difference from the topology depicted in Fig. 1 is that a three-phase variac (F in Fig. 7) is added between the power line and the grid-side filter so as to reduce the grid-side phase voltage for safety concerns. The parameters in experiments are collected in Table II. Note that for all test scenarios the reactive power reference Q^* is set to be 0 var to obtain a unit power factor operation.

1) Experimental Verification of the Proposed QC-DMPC: Fig. 8 illustrates the steady-state and dynamic performances of the proposed QC-DMPC control scheme. The load-side current tracking performance during both steady-state and transient phases are with fast dynamics and small tracking errors [see Fig. 8(a)]. The dc-link control performances are shown in Fig. 8(b). Noticeably, the dc-link voltage is almost not affected during the load change [see (b) for $t \in [0.05, 0.06]$s]. Grid-side active and reactive power control performances are shown in Fig. 8(c). Especially, nice decoupling performance of using QC-DMPC is illustrated: At around $t = 0.052$ s, a step change happens to the active power due to the load-side current change, and the reactive power is almost not affected. The grid-side current and voltage in phase-a is illustrated by Fig. 8(d): A unit power factor and also a nice dynamic performance are achieved (See Fig. 8(d) at around $t = 0.052$ s, grid-side current immediately changes in accordance to the load change).

Fig. 9 illustrates the effects of N_s to the dc-link voltage control in QC-DMPC scheme: As N_s decreases, the dynamics, i.e., the rising time, for the dc-link change is getting shorter. This further confirms that the dynamics of the dc-link voltage is controllable by changing N_s.

2) Experimental Comparison of QC-DMPC and PI-DMPC: Note that a constant value of N_s is chosen ($N_s = 100$) for QC-DMPC scheme, and the PI controller parameters for PI-DMPC scheme are tuned in a trial-and-error manner to reach the same rising time [$T_r \approx 0.2$ s, see Fig. 10(a) and (b)] as the QC-DMPC scheme. Within the PI-DMPC scheme, a *conditional integration anti-windup* strategy as an industrial standard (see, e.g., [26], [27]) is used. A first-order low-pass filter is added to the dc-link voltage measurement for both controllers for a fair *grid current* performance comparison (Figs. 11 and 12). Furthermore, all the other operation conditions are set the same.

The performance comparison of the dc-link voltage control is shown in Fig. 10. The test scenario is as follows: at $t \approx 1.8$s the dc-link voltage reference is changed from 150 to 250 V; the load current is kept at 4 A. No overshoot occurs, but a fast dynamic (with $T_r \approx 0.2$ s) is achieved when using QC-DMPC [see Fig. 10(b)]; while a considerable overshoot showing a typical second-order phenomenon is seen when using PI-DMPC [see Fig. 10(a)]. Notably, for the PI-DMPC scheme, the power ripples also increase in comparison to the QC-DMPC scheme (see Fig. 10(c) and (d) for time interval of [2, 4]s).

Fig. 11 illustrates the dc-link control performance comparison in the presence of load disturbances. The test scenario is as follows: for the time range of [0, 0.48] s, the load-side current reference is set at a magnitude of 2 A, and at around $t = 0.48$ s it changes to 4 A [see Fig. 11(a) and (b)]; while for all $t \in$[0, 1] s, the dc-link voltage reference is set to be 150 V. The dc-link voltage is almost not affected for QC-DMPC when the load is changed [see Fig. 11(f)]; this is due to the dynamic power reference which is immediately generated accordingly

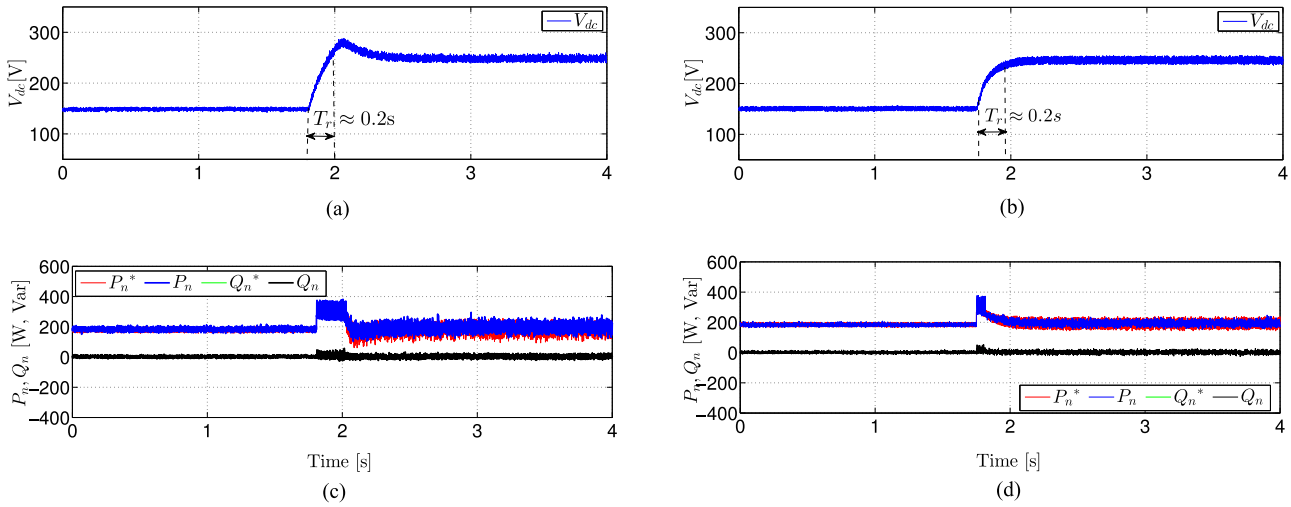


Fig. 10. Experimental results: dynamic performance comparison of PI-DMPC and QC-DMPC. (a) DC-link voltage with PI-DMPC. (b) DC-link voltage with QC-DMPC. (c) Grid-side power with PI-DMPC. (d) Grid-side power with QC-DMPC.

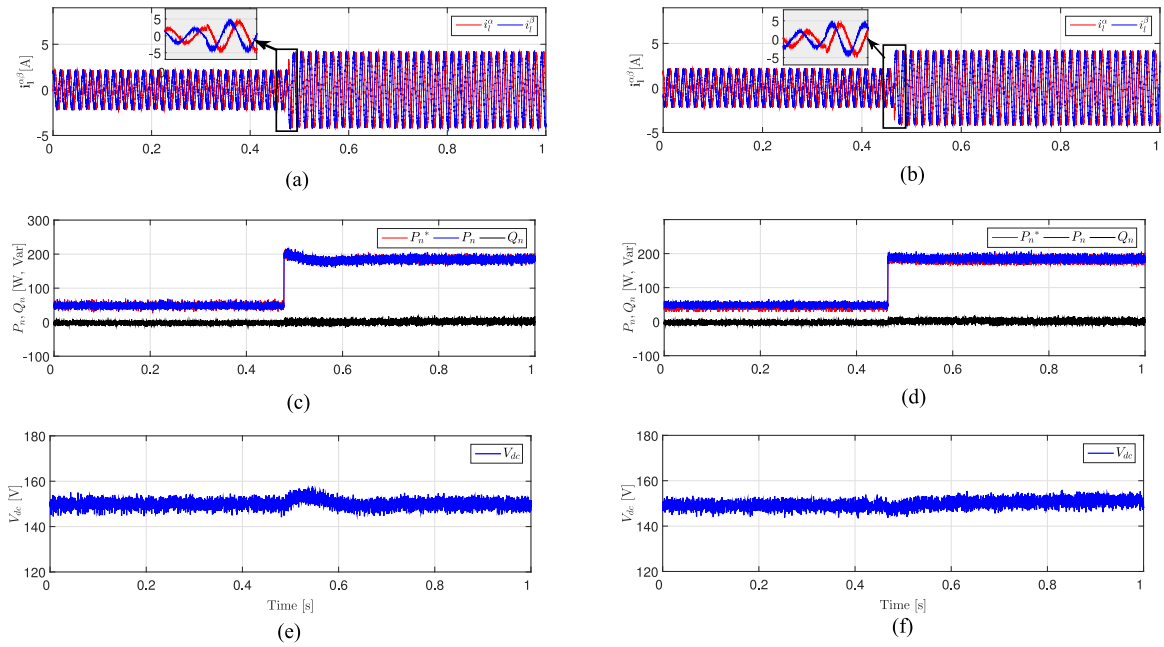


Fig. 11. Experimental results: dynamic performance comparison of PI-DMPC and QC-DMPC. (a) Load current with PI-DMPC. (b) Load current with QC-DMPC. (c) Grid-side power with PI-DMPC. (d) Grid-side power with QC-DMPC. (e) DC-link voltage with PI-DMPC. (f) DC-link voltage with QC-DMPC.

and tracked by the inner predictive control loop [see Fig. 11(d)]. However, a slight fluctuation occurs in the dc-link voltage and grid-side active power in the PI-DMPC scheme [see Fig. 11(e) and (c)] due to the slight mismatching of the load and grid-side power with using PI dc-link controller.

In Fig. 12(a) to (d), the grid-side current control comparison of PI-DMPC and QC-DMPC are given. The total harmonic distortions (THDs) of the grid-side current with QC-DMPC [3.59%, see Fig. 12(b) and (d)] outperforms PI-DMPC [4.02%, see Fig. 12(a) and (c)]. This is primarily due to the differences of the active power reference generation schemes involved. Therefore, in Fig. 12(e)–(h) the spectrum and THDs of the active power references for PI-DMPC and QC-DMPC are illustrated. The active power reference ripples in the QC-DMPC scheme are evidently smaller. The active power reference THDs for QC-DMPC is 4.10% and 4.68% for PI-DMPC [see Fig 12(h) and (g)].

3) Verification of the Robustness Under Parameters Variations: Experimental results shown in Fig. 13 illustrate the robustness of the dc-link voltage control to load parameter (load resistor R_l) variation for the two schemes. As expected, the PI-DMPC scheme outperforms the QC-DMPC scheme when the value of load-side resistor used in the controllers is changed to 150% or 50% of its measured value: QC-DMPC shows

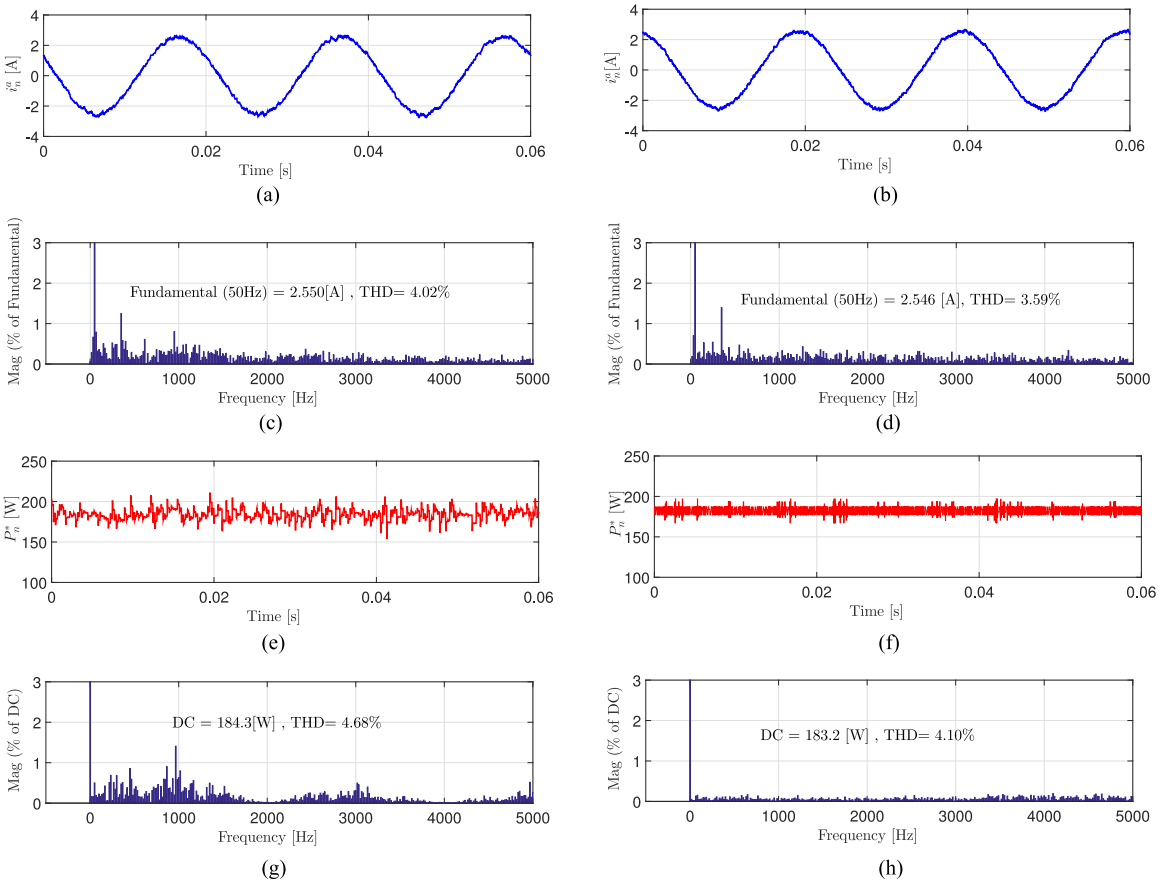


Fig. 12. Experimental results: THD comparison of PI-DMPC and QC-DMPC for grid-side current and active power reference. (a) Grid-side current with PI-DMPC. (b) Grid-side current with QC-DMPC. (c) Grid-side current spectrum and THDs with PI-DMPC. (d) Grid-side current spectrum and THDs with QC-DMPC. (e) Grid-side active power reference with PI-DMPC. (f) Grid-side active power reference with QC-DMPC. (g) Spectrum and THDs of the grid-side active power reference with PI-DMPC. (h) Spectrum and THDs of the grid-side active power reference with QC-DMPC.

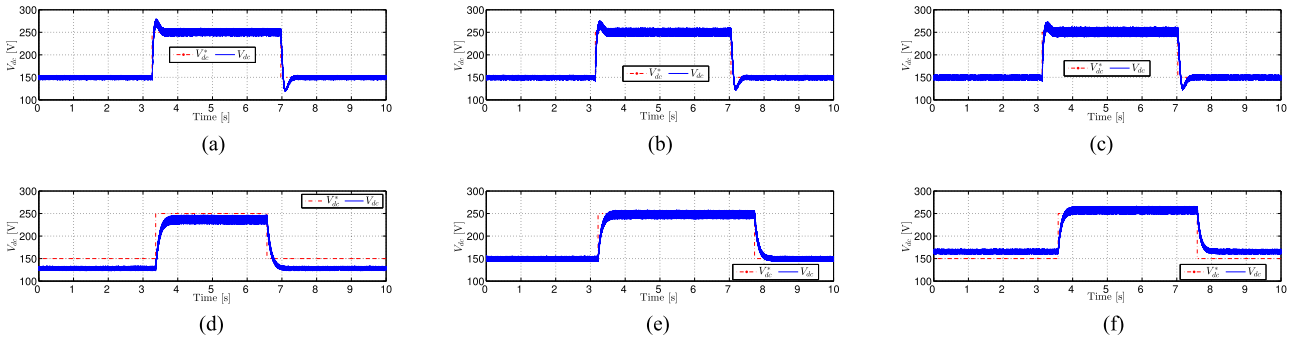


Fig. 13. Experimental results: Robustness to system parameter (load resistor R_l) variation. (a) DC-link voltage control PI-DMPC with $50\%R_l$. (b) DC-link voltage control PI-DMPC with R_l. (c) DC-link voltage control PI-DMPC with $150\%R_l$. (d) DC-link voltage control QC-DMPC with $50\%R_l$. (e) DC-link voltage control QC-DMPC with R_l. (f) DC-link voltage control QC-DMPC with $150\%R_l$.

noticeable constant steady-state errors [see Fig. 13(d) and (f)], while the steady-state performance of PI-DMPC scheme is almost not affected [see Fig. 13(a) and (c)].

Discussion of the dc-link voltage steady-state tracking errors. For QC-DMPC scheme, generally speaking, two sources may lead to dc-link voltage tracking errors in steady state: 1) modeling errors, especially the system parameter variations (like the load resistor parameter variation as is illustrated in this study); 2) actual efficiency of the power converter. While developing the dynamic reference an ideal efficiency (i.e., 100% power converter efficiency) is assumed. If in practice, the power converter efficiency is lower than 100%, evident dc-link voltage tracking errors can be observed. Intuitively, adding a term of integration (or in practice a low-pass filter) over the dc-link voltage tracking

errors to the generated reference can be a method to conquer this. Due to the length and the focus of this paper, the authors will study improved QC-DMPC schemes in the near future.

VI. Conclusion

This study has proposed a QC-DMPC scheme for voltage source back-to-back power converters. With the proposed control scheme, the dc-link voltage is directly controlled by the grid-side predictive controller using a dynamic reference generation concept, and the load-side power is estimated and fed forward to the predictive controller. With the proposed scheme, the dc-link voltage control shows good performance without any PI controller. Also, a comparison between the proposed QC-DMPC scheme and the conventional PI-DMPC scheme is investigated through *both* simulation *and* experimental results. The results confirm that the QC-DMPC outperforms the PI-DMPC scheme with accurate system parameters but with a slightly higher FPGA resource cost; however, the PI-DMPC scheme is more robust against parameter variation.

Future work will focus on eliminating the steady-state errors of the QC-DMPC scheme, and its application to back-to-back converter-based permanent-magnet synchronous generator wind turbine systems.

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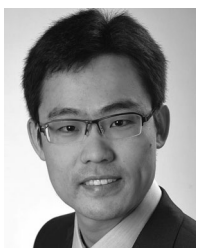

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