The Design and Data-Throughput Performance of Readout Module Based on ZYNQ SoC

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***Abstract*— ZYNQ has gradually become a flexible and suitable architecture with field-programmable gate arrays and dual-high-performance advanced RISC machine Cortex-A9 processors in applications of data acquisition and readout systems in the field of nuclear electronics. The high data rate and high-efficient data-throughput performance between the programmable logic (PL) and processing system (PS) is essential in a readout module based on ZYNQ. In this paper, four typical readout electronics system architectures are introduced, and the details of hardware and software design of the new-generation compact readout module RAIN1000Z2 based on ZYNQ XC7Z020–CLG400 are illustrated. Then, the data-throughput performance tests between the PL and PS are designed and implemented. The highest performance readout mode can reach more than 2000 MB/s data-throughput in different high-performance port combination modes. In conclusion, recommendation of combination mode is given for different data-throughput applications' requirements in readout applications based on the ZYNQ-based readout module.**

***Index Terms*— Data-throughput performance, readout module, ZYNQ.**

I. Introduction

NUCLEAR electronics have made rapid progress in the past 10 years along with the large strides of consumer and communication electronics. Many new generation electronic components such as high-performance field-programmable gate arrays (FPGAs), analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and operational amplifiers are broadly used in the data acquisition of modern nuclear electronics.

Readout electronics are an essential part of the data-acquisition chains in the electronics of many nuclear and physics experiments, such as plasma physics and nuclear fusion [1], particle physics, and high-energy physics [2], [3].

The main tasks of readout electronics include interfacing with multichannel ADCs (more than 100 MSPS), DACs, high-speed ADCs (more than 1000 MSPS) and DACs, buffering data, triggering and data transmission to the PC or server. They will be described in the following.

In order to be interfaced with ADCs, readout electronics are developed from single FPGAs, such as Spartan-6 FPGA and 7-series FPGA, into ZYNQ series, which is composed of programmable logic (PL) cells and a processing system (PS). Both the speed and volume of logic cells have been improved greatly. ZYNQ is a new all-programmable and system-on-chip (SoC) architecture of a 7-series 28-nm FPGA with dual-core high-performance advanced RISC machine (ARM) Cortex-A9 processors from Xilinx. It combines high-volume PL for real-time applications and high-speed data processing with ARM processors for high-level operating systems such as embedded Linux with TCP/IP stack and user applications. At the same time, for data buffering, the double data rate (DDR) SDRAM is often used to interface with an FPGA or ARM [4].

Variable physical interfaces, such as USB 2.0, USB 3.0, CAN, and Ethernet and fiber interfaces can be used to exchange data with the data center. In large distributed networks, the Ethernet interface has been widely used, such as in the China Dark Matter Experiment (CDEX) which is located in the China Jinping Underground Laboratory (CJPL) [2], Large High Air Altitude Shower Observatory [3], Jiangmen Underground Neutrino Observatory [5], dark matter experiment with liquid argon pulse-shape discrimination [6], and the Compact Muon Solenoid experiment [7]. The Ethernet interface has mature interface drivers and programming modes for most operating systems. Ethernet line speed has increased from 10/100 MB/s to 100 GB/s.

This paper is organized as follows. Section II presents four typical readout electronics' structures in order to introduce the readout module based on ZYNQ later.

Sections III–VI, respectively, introduce the hardware design and challenges of readout module RAIN1000Z1 and RAIN1000Z2, and the development flow of ZYNQ. They are significant preparations for experiments of data-throughput between PL and PS.

Section VII presents and compares the five data-throughput methods based on ZYNQ in detail. It also explains how the bandwidth of DDR SDRAM influences the data-throughput performance. The date rate (also use the bus rate) and the utilization of bus are defined to indicate the data-throughput performance. And finally, Section VIII concludes the data-throughput testing and results, and proposes the future works.

II. Evolution of Readout Electronics Structures

In recent years, architectures of readout electronics have migrated from the traditional VME architecture to many new types, especially for readout with the high-speed ADCs, where the sample speed is typically 100 MSPS to several GSPS. The low voltage differential signaling (LVDS) data rate

Manuscript received March 2, 2018; accepted March 26, 2018. Date of publication March 29, 2018; date of current version May 16, 2018.

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Digital Object Identifier 10.1109/TNS.2018.2820706

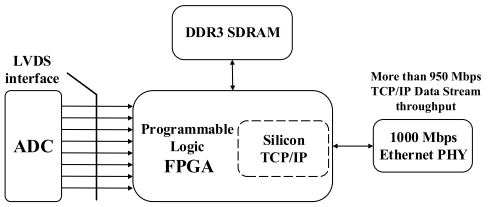

Fig. 1. Readout electronics system architecture with a single FPGA and "silicon" TCP/IP stack developed based on HDL.

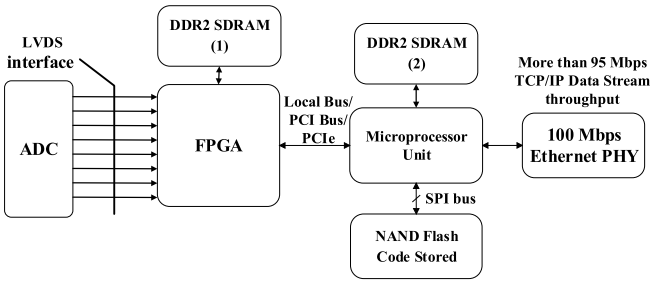

Fig. 2. Readout electronics system architecture with an FPGA and MPU. The TCP/IP stack is based on embedded Linux.

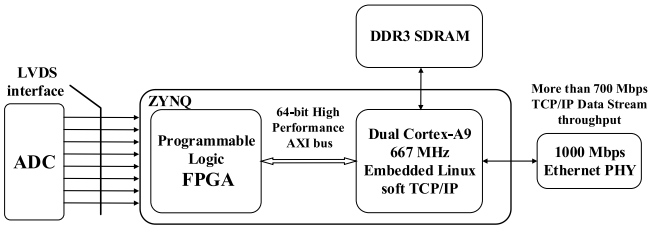

Fig. 3. Readout electronics system architecture with a single ZYNQ SoC and TCP/IP stack based on embedded Linux. The DDR3 SDRAM connected to the ARM processor is used for the high-throughput data buffer.

depends on the ADC sampling rate and bit resolution. Four readout electronics systems are summarized in Figs. 1–4. For convenience, only the interface to ADCs will be discussed. The differences among these architectures are in the way how to buffer the data from the ADCs and how to transmit the data using the Ethernet interface.

In Fig. 1, the data from external ADCs are buffered in the external DDR3 SDRAM, which is directly controlled by the FPGA, and then sent to the Ethernet interface by a hardware description language (HDL)-based TCP/IP stack, such as the SiTCP [8] or some home-made UDP stack developed for dedicated applications, where the number of sockets is limited.

Within the other architectures depicted in Figs. 2–4, the software TCP/IP stack with embedded Linux is used. Although the typical HDL-based TCP/IP stack's data rate is higher than that of the software TCP/IP stack in embedded Linux, the embedded Linux solution is more convenient than the silicon TCP/IP solution due to the flexible and easy way to develop and maintain.

Before the release of ZYNQ SoC with FPGA and ARM processors in a single chip, the architecture of the traditional readout system was similar to that shown in Fig. 2. This architecture uses a single FPGA, such as a Spatran-6 family

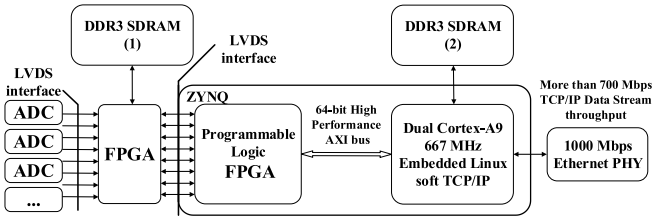

Fig. 4. Readout electronics system architecture with dual chips. The standalone FPGA is used for high-density I/O, and connected to multiple ADCs, the ZYNQ is used for readout. External FPGA is used because ZYNQ's PL does not have enough I/O pins, and more bandwidth can be realized with the DDR SDRAM connected to external FPGA.

FPGA, to receive the 1000 MSPS ADC data stream through LVDS or LVCMOS signals. The DDR2 SDRAM is used as a data buffer, running at a clock rate of approximately 266 MHz.

Some staple interfaces are used as bridges between the FPGA and microprocessor unit (MPU) (such as the Power PC-based 400-MHz MPC5125 from Freescale). The local bus is typically a 66-MHz asynchronous bus, with 32-bit data width [9], which is shared with other peripherals such as flash memory. The PCI bus is typically a 33- or 66-MHz synchronous bus with 32-bit data width and direct memory access (DMA) can be used [10]. The typical bandwidth of these two traditional bridges is approximately 100–250 MB/s. (Bandwidth is bus speed multiply with data width.)

Some architectures use PCI express as the bridge between the FPGA and MPU [11], but it is limited by the unique serial transceivers used for data links, most low-end FPGA or MPU products do not have a PCI Express interface.

The MPU integrates high-speed interfaces such as the Ethernet interface and some slow control interfaces [12]. This type of readout subsystem requires one independent FPGA and one MPU, with their separate associated power supplies and other chips, and has the shortcomings of larger printed circuit board (PCB) area and higher power consumption. The readout electronics architectures based on ZYNQ in Figs. 3 and 4 will be introduced in the Sections III and IV.

III. Previous RAIN1000Z1 Hardware Design

Since early of 2014, the RAIN1000Z1 readout module with a Gigabit Ethernet interface has been developed [13]. It is based on ZYNQ SoC. Readout electronics systems embedded with the RAIN1000Z1 readout modules have been developed for nuclear and particle experiments [14], [15].

Within the RAIN1000Z1 module, embedded Linux runs on the dual ARM processors and the real-time processing logic including the central direct memory access (CDMA) controller, buffer, FIFO, and LVDS interface are embedded and run on the corresponding logic resources in the FPGA in a single chip. Based on embedded Linux, the programs based on the TCP/IP socket and the relevant device drivers [16] are developed for data transport with the Ethernet interface, and some slow-control software are also implemented, such as EPICS [17].

Most of the modern high speed, high-performance ADC chips (typically 100 MSPS 14-bit ADC or 1000 MSPS 12-bit ADC) use the serial or parallel LVDS interface to output the converted digital data to the associated external FPGA.

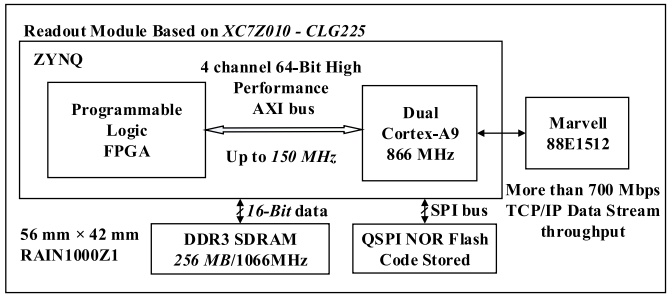

Fig. 5. Previous RAIN1000Z1 readout module system architecture.

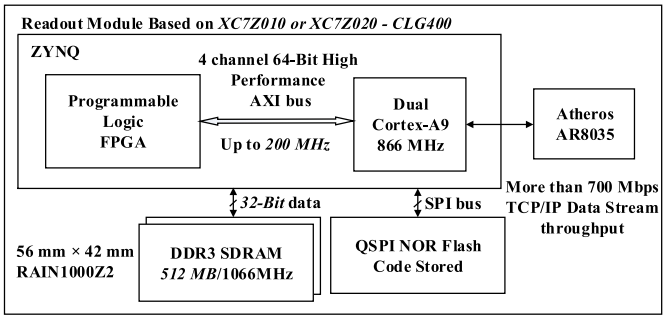

Fig. 6. RAIN1000Z2 readout module system architecture.

In the previous design, the AD9253 is a 14-bit 100 MSPS ADC. It uses two data lanes; the data rate for each data lane is 800 MHz in the singe data rate (SDR) mode or 400 MHz in the DDR mode [18]. The ADC12D1000 is a 12-bit 1000 MSPS ADC and the nondemuxed parallel LVDS 1:1 output is 1000 MHz in the SDR mode or 500 MHz in the DDR mode [19].

All of these ADCs can be interfaced to the RAIN1000Z1 module directly. The readout system architecture is similar to that shown in Fig. 3, where the DDR SDRAM is connected to the ARM processor directly and used for high-throughput data buffer.

For readout systems that need additional LVDS signals to interface with multiple-ADC chips, a separate larger footprint, higher volume logic resource FPGA is used for the main logic hub and the RAIN1000Z1 module is only used for readout. An example [20] is the XC7K325T with FFG900 footprint in the data acquisition system for the high-purity germanium detector of CDEX in CJPL. The readout system architecture is similar to that shown in Fig. 4.

Fig. 5 shows the architecture of the previous generation RAIN1000Z1 readout module. It is an independent module without ADC.

Due to the ZYNQ XC7Z010 chip in the CLG225 footprint, there are several disadvantages in the RAIN1000Z1 readout module as follows.

One is the limited number of LVDS pairs. Although the footprint of the XC7Z010 chip (13 mm × 13 mm package size) is quite small and suitable for the 56 mm × 42 mm readout module size, there is a limitation in the pin numbers of the CLG225 package. The input and output (I/O) pins includes only 27 LVDS pairs or 54 single-LVCMOS pins. This is adequate for single or dual 14-bit 100-MHz ADCs, but it is insufficient for higher sample speed ADCs, such as ADC12D1000, which requires a parallel LVDS data interface and about 50 LVDS pairs are needed.

The second disadvantage is the low-bandwidth interface with the DDR3 SDRAM. The XC7Z010 chip of RAIN1000Z1 has a 16-bit data-bus-width DDR3 SDRAM interface. The memory chip MT41J128M16 is used as the external DDR3 SDRAM. The single-external memory chip is favorable for a compact module design, but the 16-bit data-bus-width limits the throughput when transferring the data from the external ADCs to the DDR3 SDRAM with DMA. The details and comparisons will be introduced later.

TABLE I
DESIGN COMPARISON OF RAIN1000Z1 AND RAIN1000Z2

Comparison item	RAIN1000Z1	RAIN1000Z2
ZYNQ chip	XC7Z010-CLG225	XC7Z020-CLG400
LVDS interface	27 pairs	60 pairs
DDR data width	16-Bit	32-Bit
DDR theoretical bandwidth	2033 MB/s	4066 MB/s
I/O bank power supply	Fixed	Flexible

Other disadvantages include the flexibility of I/O banks' power supply. In the design of the RAIN1000Z1 module, the VCC I/O ports for all banks are connected to the same power rail. In many applications, different power rails are needed for different I/O banks to meet the voltage level requirements of different interfaces.

IV. RAIN1000Z2 HARDWARE DESIGN

The RAIN1000Z2 readout module has been developed for more complex applications of readout systems that require more I/O pins and compact physical size. The main chip is XC7Z010 or XC7Z020 in the CLG400 footprint; these two chips are footprint compatible. Chip's footprint is 17 mm × 17 mm, which is slightly larger than the previous size of XC7Z010 in the CLG225 footprint.

Fig. 6 depicts the architecture of the RAIN1000Z2 readout module. It is an independent module without ADC.

The DDR3 SDRAM interface has been upgraded to a 32-bit data bus width and two MT41J128M16 chips (16-bit DDR3 SDRAM in each chip) are used. Table I compares the key features of RAIN1000Z2 with the previous RAIN1000Z1. The theoretical bandwidth is calculated with multiply the data bus width and data rate of the DDR interface (typically 533 MHz in DDR). The details will be illustrated later.

A. Board-to-Board Connectors

Four connectors are selected and used for the readout module. Each connector has dual rows and 60 pins. It is high-density, fine-contact-pitch, surface-mounted and board-to-board connectors from MezzoStak series connectors [21].

The MezzoStak connector can be mated to itself, so the same connectors are used in the readout module and base board. This feature can reduce the component-engineering costs. The MezzoStak series connector supports high-speed

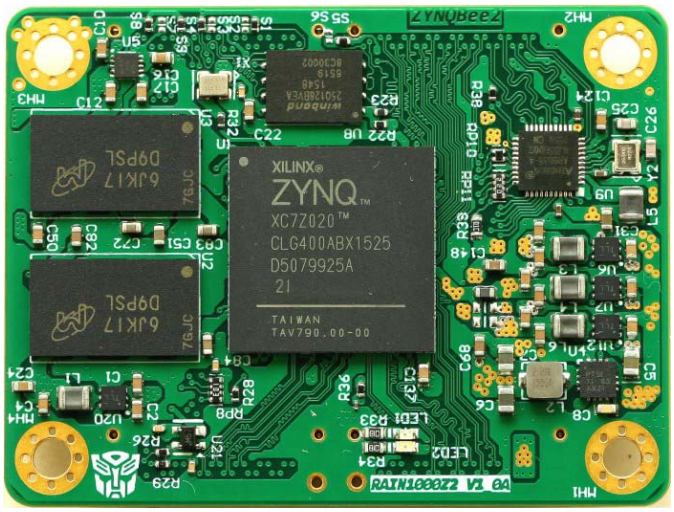

Fig. 7. Top view of the RAIN1000Z2 readout module.

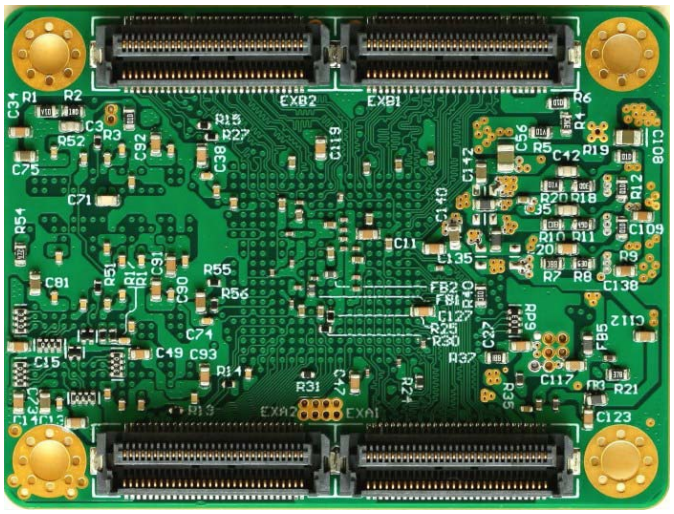

Fig. 8. Bottom view of the RAIN1000Z2 readout module with four MezzoStak 60-pin 0.5-mm-fine-pitch dual-row connectors. There are four 3.2-mm assembly holes in the corners, which are connected to the ground.

differential signal standards, such as the PCI Express Gen2, whose maximum bandwidth can reach 5 GB/s.

With four MezzoStak 60-pin connectors, a total of 240 pins can be deployed for power, Ethernet, LVDS I/O, XADC, and the debugging interface. Fig. 7 shows the top view of the RAIN1000Z2 module, and Fig. 8 shows the bottom. The four MezzoStak connectors can be found in Fig. 8. For comparison, the top view of the previous RAIN1000Z1 module is shown in Fig. 9.

B. PCB Layout

The RAIN1000Z2 has been kept of the same size with the RAIN1000Z1 though the RAIN1000Z2 become more densely packed. For flexibility in the I/O power supply, more dc/dc power converters are used.

C. Ethernet PHY and Power Supply

The AR8035 Gigabit Ethernet PHY chip is used for the new design because of its smaller PCB footprint. The copper interface for unscreened twisted-pair cables is provided and the fiber interface is removed.

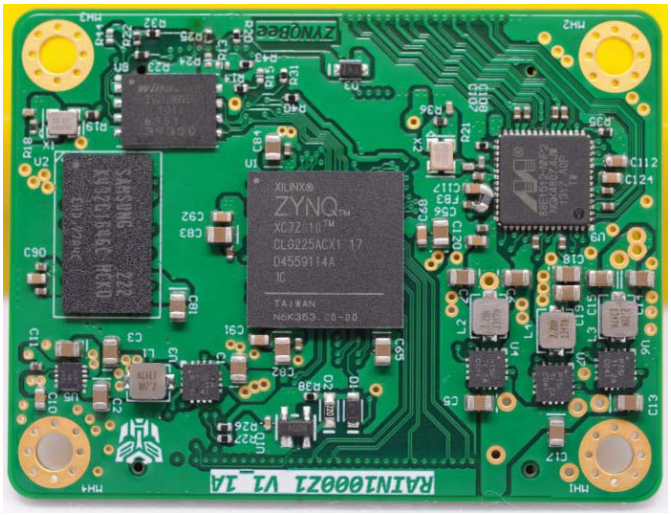

Fig. 9. Top view of the previous RAIN1000Z1 readout module [13].

The TPS62130RGT, NCP1529MUTBG, and TPS51206DSQ are used as dc/dc power converters to generate different power rails. Their input voltages are from the 5-V dc power supply via the board-to-board connectors. The TPS62130RGT and the IHLP1212 power inductor are used to generate the 1-V/3-A core power for the ZYNQ SoC. The NCP1529MUTBG and LQM2HPN4R7MG0 are used to generate 3.3-V/1-A, 2.5-V/1-A, and 1.8-V/1-A power for I/O banks, LVDS, and auxiliary supply, respectively. The TPS51206DSQ (generate 0.75 V) is used as the dedicated DDR3 SDRAM terminal source/sink voltage regulator.

D. SPI Flash and SD Card

The N25Q128F8 Quad SPI NOR serial flash memory from micrometer is used to store the FPGA bit stream, boot loader, Linux kernel, file system, and user application code. An additional Micro-SD Card interface and socket can be supplied within the base board, as the required signals are present in the board-to-board connectors. An electro static discharge protection circuit and voltage-level translation circuit can be added for the card socket when it is used for long-distance or hot-plug operation.

V. Hardware Design Challenges

Signal integrity (SI) is the key issue in high-speed hardware designs [22]. The design of the RAIN1000Z2 readout module faces many challenges, which are mostly derived from the 1066-MHz DDR3 SDRAM interface and the small module size.

In the small physical size, the ZYNQ chip and two DDR3 SDRAM chips must be deployed, along with some associated power chips and other components. However, blind VIAs in the PCB layout design are not desirable because of the expensive setup and fabrication costs.

Simultaneously, with the fly-by topology, the high-speed 1066-MHz memory interface of DDR3 SDRAM should not only ensure the impedance control at 40 Ω and length matching of the trace on the PCB but also consider and compensate for the flight time in the silicon package.

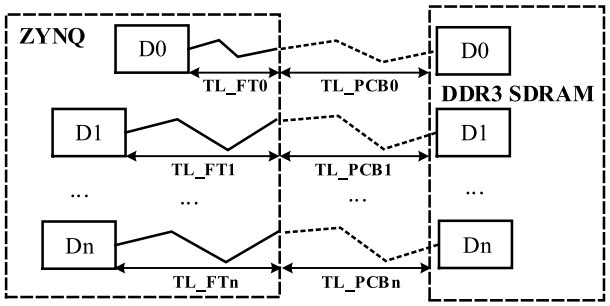

Fig. 10. Trace length-match structure of the data signals.

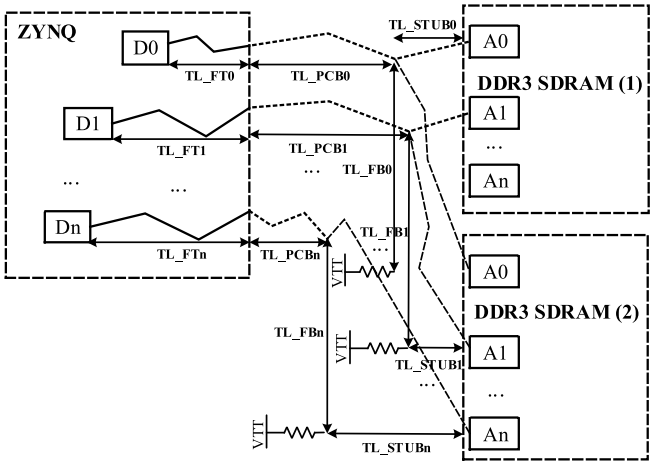

Fig. 11. Trace length-match structure for the address and control signals in the fly-by topology of the DDR3 SDRAM.

A. Data Signals of the DDR3 SDRAM Layout

Fig. 10 depicts the data signal's trace length-match structure. The flight time or trace length in the silicon package is TL_FT, and the trace length in the PCB layout is TL_PCB. The length matching for the data signals between FPGA and DDR3 SDRAM should include both. Equation (1) shows the data signal length-matching rules. The discrepancies between the DQ signals in the same group (DQ0 to DQ7, DQ8 to DQ15, DQ16 to DQ23, DQ24 to DQ31, and their corresponding DQS and DM signals, in the four independent groups) should be controlled to within ±5 ps or ±40 mils (FR4 PCB materials). According to the design guide [23] from Xilinx, the CLK_P/CLK_N signal has to be delayed relative to the DQS_P/DQS_N signal by at least 150 ps or 1200 mils

$$\text{TL\_FT0}+\text{TL\_PCB0}=\text{TL\_FTn}+\text{TL}_{\text{PCBn}},\quad \text{for } n=1,2,\ldots. \tag{1}$$

B. Address and Control Signals of the DDR3 SDRAM Layout

The fly-by topology is used for the address and control signals of the DDR3 SDRAM. Fig. 11 indicates the length matching structure for address and control signals. The trace length between the two DDR3 SDRAMs in the fly-by topology is TL_FB. The stub trace length from the address/control signals to the terminal resistors is TL_STUB. The following

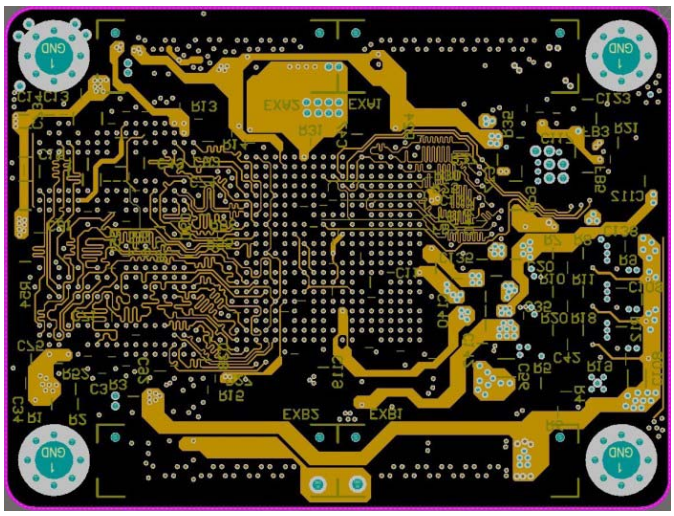

Fig. 12. Layout of the RAIN1000Z2 PCB design. The left-middle area shows the PCB trace tuning for the length matching.

equation shows the length match rules for address and control signals:

$$\begin{gathered}\text{TL\_FT0}+\text{TL\_PCB0}=\text{TL\_FTn}+\text{TL\_PCBn},\quad \text{for } n=1,2,\ldots\\ \text{TL\_FB0}=\text{TL\_FBn},\quad \text{for } n=1,2,\ldots\\ \text{TL\_STUB0}=\text{TL\_STUBn},\quad \text{for } n=1,2,\ldots.\end{gathered} \tag{2}$$

The deviations of the address and control signals from the CLK signal need to be controlled within ±8 ps or ±64 mil. In addition, the length of the signal between two adjacent DDR3 SDRAMs should be controlled from 350 to 750 mils.

C. Termination

Terminations for the address and control signals are needed and should be stubbed to a 0.75-V terminal regulator through 40-Ω resistors.

Fig. 12 shows the data signals and address/control signals on one middle PCB layer. The length tuning (the twists and turns of PCB traces) can be observed. The tuning rules are calculated and correspond to (1) and (2).

D. Signal Integrity of Other Signals

In the PCB design of the RAIN1000Z2, the SI must be considered. It includes not only the DDR3 SDRAM interface but also the Quad-SPI interface, the RGMII PHY interface, and every LVDS pair routed to the high-speed board-to-board connectors. In addition, impedance and length matching must be ensured.

E. Thermal Design

The thermal design had to be considered in the design of the RAIN1000Z2 module and the heat is produced mostly by the ZYNQ chip. Due to the compact size of the readout module, a custom heat-sink cap was designed for the module. Fig. 13 shows the heat sink, where there is a cap for the ZYNQ chip and it is fastened with the four assembly holes in the corners of the readout module. The metal studs (the red

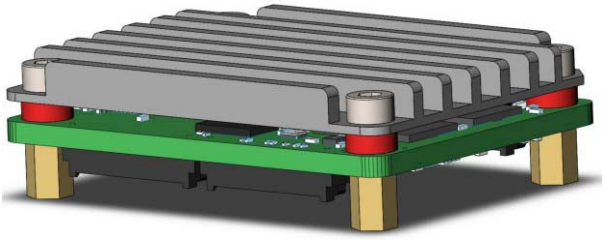

Fig. 13. Dedicated heat sink for the RAIN1000Z2 thermal control in the conditions with no airflow.

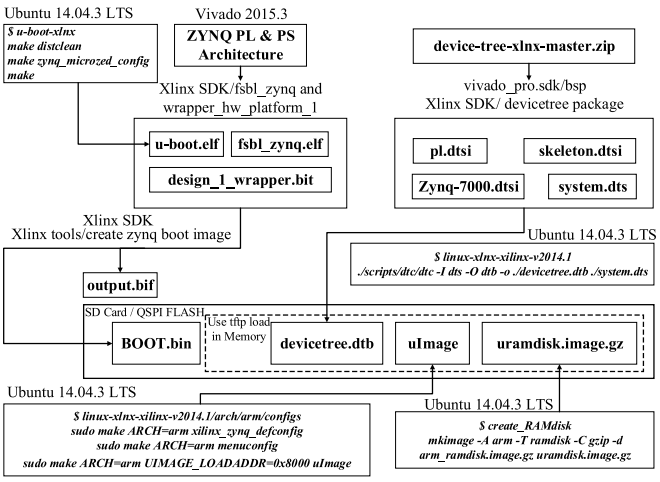

Fig. 14. File preparations and development flow with ZYNQ.

ones in Fig. 13) under the heat sink also have the effect of heat conduction. With the heat-sink cap assembled, the ZYNQ chip is cooled down from 73 °C to 53 °C. The temperature is measured with the XADC integrated in the ZYNQ chip, and a dedicated user application is running in embedded Linux with the frame-supported industrial I/O devices [24].

The stacked height of the dual MezzoStak board-to-board connector is 7 mm (with the base-board connector and readout module). The height of the heat sink is approximately 5 mm, and the capability of heat dissipation is sufficient for most applications with the RAIN1000Z2 module. For heavy power loads, additional fan should be used.

VI. Software and Firmware Development

The development for the RAIN1000Z2 readout module based on ZYNQ includes two sections. One is the program design, which is developed in a high-level language such as C, C++, and Python. It runs in embedded Linux on the ARM processor. The other section is the firmware design, which is developed by the HDL for the FPGA.

Fig. 14 outlines the file preparations and development flow with ZYNQ. The Vivado 2015.3 integrated development environment from Xilinx is used for HDL development. The Ubuntu 14.04.3 LTS with the cross ARM GCC is used for program development based on embedded Linux. Several key commands after symbol "$" are presented to generate u-boot.elf, devicetree.dtb, uImage, and uramdisk.image.gz. The Xilinx software development kit 2015.3 is used to establish BOOT.bin and suppo*rt*packages (such as devicetree).

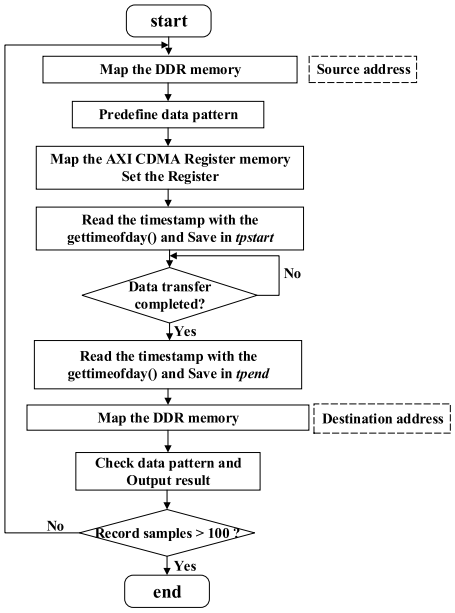

Fig. 15. Detailed test flow of a single HP port. The function gettimeofday() is used to obtain the current time and the function mmap() is used to map the memory to the file.

SD Card and QSPI Flash can be used as storage media. The BOOT.bin is mainly used to boot FPGA and embedded Linux.

To test the data throughput between PL and PS, the /dev/mem device and mmap function in embedded Linux (version Linux-3.13.0-Xilinx) are used. Although dedicated device drivers can be developed for accessing the physical memory in embedded Linux, the /dev/mem device with the mmap function is the most direct, easy, and flexible way to access the physical memory.

With the mmap function, the /dev/mem device provides the ability to access system's physical memory, including the memory space of the external DDR3 SDRAM, dual-port BRAM in the PL space, and the registers of IP cores.

Fig. 15 illustrates the flow of the test application for performance testing.

The test application's steps are as follows.

1) Initialize the dual-port BRAM through the AXI4 bus with hexadecimal data pattern "5A" per byte. The BRAM will act as the source in CDMA transport.
2) Clear the corresponding memory space in the external DDR3 SDRAM, which will act as a destination in CDMA transport.
3) Initialize the CDMA registers. Configure the CDMA in simple mode, and set the source address and the destination address.
4) Write the BTT register of CDMA to start the transfer of CDMA. Follow this operation, read the timestamp with the gettimeofday() function in microseconds resolution, and save it in the tpstart variable. No other operation should be allowed between the BTT register operation and the gettimeofday() function call.
5) Poll the status register of CDMA and wait for DMA to finish. When it is finished, read the timestamp with the gettimeofday() function and save it in the tpend variable.

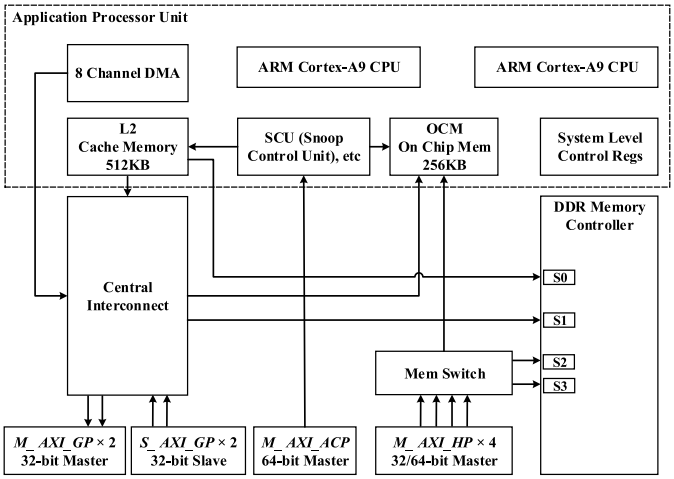

Fig. 16. Block diagram of PL and PS connections in ZYNQ.

6) Read from the destination address and compare with the data pattern.
7) Calculate the time used with tpend and tpstart. Test does not end until 100 samples are recorded.

VII. Performance Testing and Results

The theoretical bus rate (in megabyte per seconds) is calculated by (3), where freq (inmegahertz) is the frequency of bus clock and width (in bits) is the width of bus. The utilization of bus is calculated by the following equation:

$$\text{Theoretical Bus Rate} = \text{freq} \times \frac{\text{width}}{8} \times \left(\frac{1000}{1024}\right)^2 \quad (3)$$

$$\text{Utilization of Bus} = \frac{\text{Tested Bus Rate}}{\text{Theoretical Bus Rate}} \times 100\%. \quad (4)$$

Fig. 16 outlines the typical interconnection buses and their connections with the DDR memory controller. There are three kinds of data-exchange ports between PS and PL, and a total of nine AXIs (Advanced eXtensible Interfaces) are provided in ZYNQ SoC, i.e., four 32-bit general-purpose (GP) ports for general usage, four 32-/64-bit high-performance ports (HP-ports) for high-bandwidth data exchange and a 64-bit accelerator coherency port (ACP).

HP ports and the ACP ports are used to access the external DDR memory in cooperation with the CPU and hardware accelerator [25]. Some factors of their performance data are discussed in [26]. Generally, the GP ports can be used for register configuration and slow data exchange.

The four high-speed, high-performance data paths between the PS and PL are named HP0 to HP3, support up to 64-bit, 150-MHz operation frequency (the typical frequency, which is decided by the silicon speed version and timing constraint result) and can reach up to 1144 MB/s bandwidth for one HP port theoretically.

In the following test modes (from Mode A to Mode E), the GP master port is always used to readback BRAM data, initialize BRAM and configure the associated CDMA registers when necessary. Different combinations of GP ports and HP ports have been deployed. Five different test mores are implemented for performance tests between PL and PS.

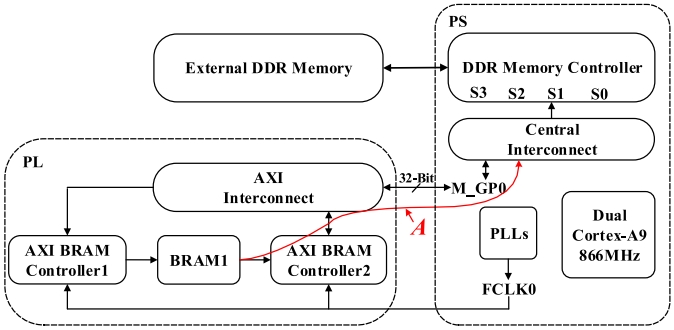

Fig. 17. Block diagram of the deployment of a single GP port. The line pointed by A means the direction of data flow from PL to PS.

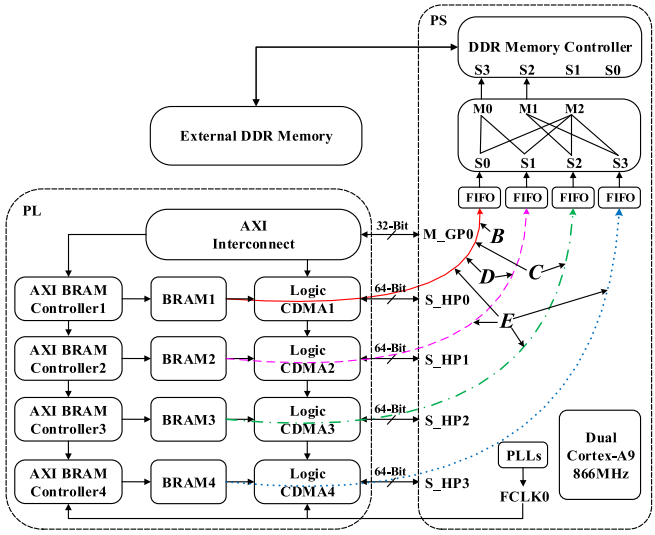

Fig. 18. Block diagram comparing Mode E with Modes B, C, and D. The lines pointed by B, C, D, and E mean the direction of data flow from PL to PS.

Fig. 17 outlines the block diagram for Mode A, and Fig. 18 depicts the test Mode B to Mode E. The details of every mode will be discussed later.

In the previous RAIN1000Z1 readout module, the 16-bit, 1066-MHz DDR3 SDRAM's theoretical data bus bandwidth is about 2033 MB/s for read and write operations separately. The data throughput was limited by RAIN1000Z1's 16-bit data bus width with the external DDR3 SDRAM. In practical applications, the typical essential raw data bandwidth of DDR3 SDRAM is approximately 80% of the theoretical bandwidth [27], so the actual bandwidth of DDR3 SDRAM is about 1626 MB/s. This is because, in actual applications, not only the inconsistency between ARM and DDR3 SDRAM but also the embedded Linux operating system also requires some percentages of the read/write bandwidth.

However, in the previous RAIN1000Z1, in Mode B (use a single HP port for data exchange), the maximum of the actual bandwidth can attach about 808 MB/s, which is about a half of the actual bandwidth of DDR3 SDRAM.

Within the new RAIN1000Z2 readout module, the DDR3 SDRAM's data bus widths is doubled to 32-bit, the theoretical bandwidth is increased to 4066 MB/s for read/write

operation separately, and the essential bandwidth is approximately 3253 MB/s. The maximum of the actual bandwidth is upgraded from 808 to 1087 MB/s.

The details of the test mode, software flow and results will be discussed later. In the following test, 100 samples are measured for every test mode. Every tested bus rate and its standard deviation are calculated by (5)

The tested bus rate is presented as tested bus rate standard deviation. The utilization of bus has the same data process and presentation with the tested bus rate.

In embedded Linux, command top is used to obtain the CPU usage. The average CPU usage is about 21% in Mode A and 11% in Mode B to Mode E

$$\text{Tested Bus Rate} = \frac{\sum_{i=1}^{100} \text{sample}(i)}{100}$$

$$\text{Standard Deviation} = \sqrt{\frac{\sum_{i=1}^{100} [\text{Tested Bus Rate} - \text{sample}(i)]^2}{100}}. \quad (5)$$

A. Mode A, Use a Single GP Port for Data Exchange

Mode A is the simplest mode for gathering data from an external ADC or other data source (The I/O bandwidths are similar, so only the input bandwidth is discussed in the following test.) Fig. 17 outlines the block diagram for Mode A.

Two AXI_BRAM_Controller IP cores are used to access the dual-port BRAM. One is used for data-throughput performance test and the other is used to initialize the dual-port BRAM with hexadecimal data pattern "5A" per byte. With the data pattern, process of postdata verification can be performed. Both AXI_BRAM_Controller cores should be assigned with the proper addresses in address editor within Vivado. The test application reads from and writes to the corresponding address to complete data pattern initialization and throughput performance test with the/dev/mem device and mmap function in embedded Linux.

FCLK0 is the clock generated from the PS and fed to the PL logic as main clock source. It can be controlled and trimmed in embedded Linux with the xdevcfg device node and the corresponding drivers, which allow user-space FCLK speed controls in real time. The range of FCLK clock speed is 50 to 250 MHz. A typical series of test frequencies is 50, 100, 125, 142.8, and 166.7 MHz. (Due to the 33.33-MHz PS clock and the PLL limitation, a 142.8 MHz was the actual clock speed when we set it to 150 and 166.7 MHz was the actual clock speed when we set it to 180 MHz.)

The Mode A test results are shown in Table II for different frequencies of FCLK0. In Mode A, the RAIN1000Z1 readout module has the same performance with the RAIN1000Z2.

The GP ports are not intended for data throughput with high data rate. In the illustration for Mode A, no CDMA is used due to low participation of the ARM processor with embedded Linux. The data bandwidth is also influenced by the other AXI bus operations. However, Mode A is not complicated to implement and it does not require the configuration of many complex IP cores or software development. Therefore, it should be the first choice for data-throughput with lower data rate applications.

TABLE II
TEST RESULTS IN MODE A FOR THE RAIN1000Z2 MODULE

FCLK0 (MHz)	Data Rate (MB/s)	Single GP port theoretical Bus Rate (MB/s)	Utilization of Bus (%)
50	172.0 ± 0.5	190.7	90.2 ± 0.2
100	335.0 ± 1.5	381.5	87.8 ± 0.4
125	414.2 ± 2.4	476.8	87.7 ± 0.5
142.9	468.5 ± 3.1	545.1	86.0 ± 0.6
166.7	540.1 ± 4.2	635.9	84.8 ± 0.7

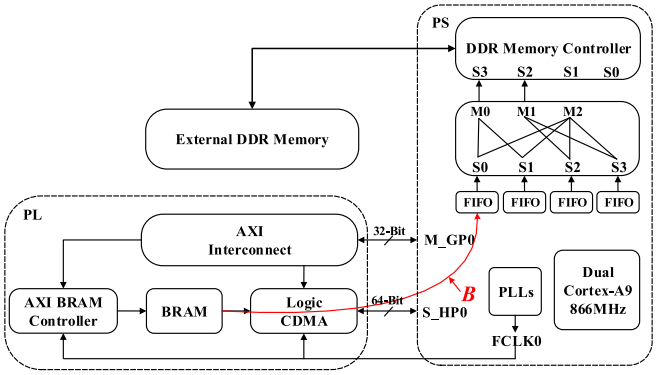

Fig. 19. Block diagram of the deployment of a single HP port. The line pointed by B means the direction of data flow from PL to PS.

B. Mode B, Use a Single HP Port for Data Exchange

For data-throughput with higher data rate applications, HP ports should be used with CDMA function to exchange data between the PS and PL. The HP ports in 32- or 64-bit configurations can be used. In the following discussion, only 64-bit configurations are considered. Fig. 19 shows the block diagram for Mode B.

In Fig. 19, the left AXI_BRAM_Controller IP core is used to initialize the dual-port BRAM with a predefined data pattern for final data verification. The right CDMA controller will transfer the preinitialized data from BRAM through HP0, memory interconnect, the DDR memory controller to external DDR3 SDRAM and then to the ARM processor. The registers of the CDMA controller can be read or written through GP ports with some slow controls.

For comparison, the previous RAIN1000Z1 readout module and the new RAIN1000Z2 module are both tested in Mode B. Table III shows the test results for Mode B with the RAIN1000Z1 module, which has the 16-bit DDR3 SDRAM interface.

Due to the limitation of 16-bit DDR3 SDRAM interface in the RAIN1000Z1 module, it is found that the data rate for Mode B increased in direct proportion to the increments of the FCLK0 clock speed and became flat at approximately 800 MB/s with 125-MHz FCLK0 clock rate. The reason is that the maximum essential bandwidth of the 16-bit DDR3 SDRAM is 1626 MB/s. About 50% of bandwidth can be used in single HP port mode (because we perform write and read together).

TABLE III
TEST RESULTS IN MODE B OF THE RAIN1000Z1 MODULE

FCLK0 (MHz)	Data Rate (MB/s)	Single HP port theoretical Bus Rate (MB/s)	Utilization of Bus (%)
50	346.5 ± 3.4	381.5	90.8 ± 0.9
100	664.9 ± 2.6	762.9	86.8 ± 0.3
125	800.1 ± 4.8	953.7	83.9 ± 0.5
142.9	808 ± 5.0	1090.2	74.1 ± 0.5

TABLE IV
TEST RESULTS IN MODE B OF THE RAIN1000Z2 MODULE

FCLK0 (MHz)	Data Rate (MB/s)	Single HP port theoretical Bus Rate (MB/s)	Utilization of Bus (%)
50	359.2 ± 2.9	381.5	94.2 ± 0.8
100	689.2 ± 15.7	762.9	90.3 ± 2.1
125	848.4 ± 25.2	953.7	89.0 ± 2.6
142.9	947.7 ± 21.6	1090.2	87.0 ± 2.0
166.7	1087.7 ± 26.3	1271.8	85.5 ± 2.1

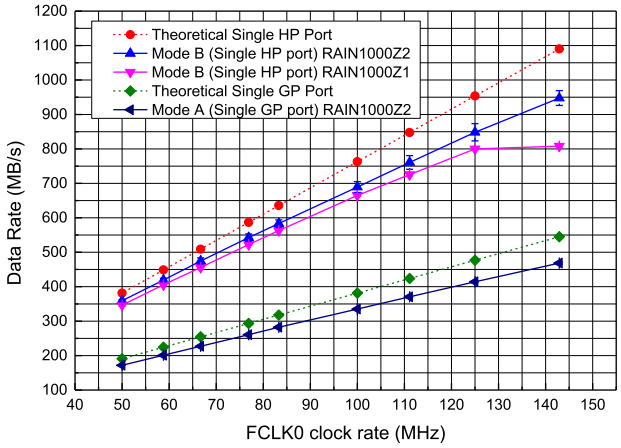

Fig. 20. Comparison of the test results in single test mode for the RAIN1000Z1 and RAIN1000Z2 modules. The limitation of the throughput for the 16-bit DDR3 SDRAM data bus and the plateau of the data rate for the RAIN1000Z1 at 100-MHz FCLK0 clock rate are shown.

Table IV shows the test results in Mode B for the RAIN1000Z2 module, which has the 32-bit DDR3 SDRAM interface.

The data-throughput performances for RAIN1000Z1 and RAIN1000Z2 in Mode A and Mode B are compared in Fig. 20. It is observed that Mode B with the HP port and CDMA controller has an improvement over Mode A with the GP port in terms of data rate. Besides, with the improvement from the previous 16- to the 32-bit DDR3 SDRAM data bus, it is observed that the limitation of data throughput from the DDR3 SDRAM is no longer playing a leading role. The data rate increases in proportion to the FCLK0 clock speed, and the bottleneck is inexistent. The utilization of bus can reach more than 85% of the theoretical bus bandwidth of a single HP port.

C. Mode C, Use Combined Dual HP Ports HP0 With HP2

With the demand for data throughput with higher data rate in readout applications such as the multigigahertz ADCs used for pulse-shape digitalization, it is instinctive to use more HP ports to implement multichannel data exchange between the PL and PS with external DDR3 SDRAM.

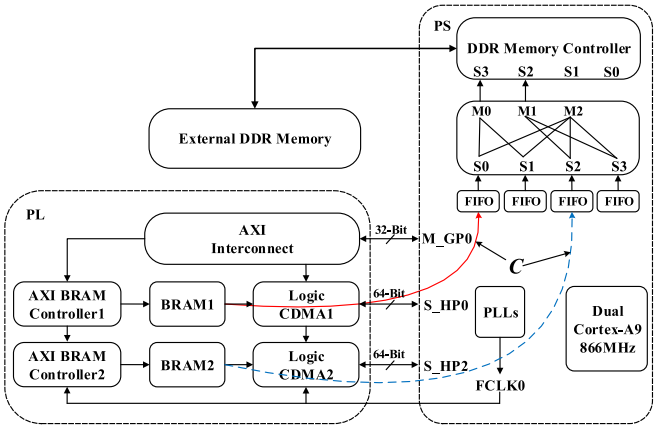

Fig. 21. Block diagram of the deployment of combined dual HP Ports HP0 and HP2. The lines pointed by C means the direction of data flow from PL to PS.

Two combination methods of dual HP ports (HP0 with HP2 and HP0 with HP1) are used in Mode C and Mode D. The other combination methods of dual ports have the similar data throughput performance. For example, the throughput performance of HP1 with HP3 is equal to that of HP0 with HP2. The reason is illustrated in the following.

Fig. 21 shows the block diagram for Mode C (combining dual HP ports HP0 and HP2). The top right of Fig. 21 shows the internal architecture of the four HP ports. In the dual-channel combination mode, the HP0 with HP2 groups and the HP0 with HP1 groups are compared. The internal HP ports are connected to the memory interconnect and the mux to the memory controller.

HP0 and HP1 are connected to the same *S*3 port in the DDR memory controller, and HP2 and HP3 are connected to the same *S*2 port. When HP0 and HP1 are combined with dual channel mode, competition, and arbitration will occur and the data bandwidth will be nonfluent when the switch bus is busy. With the combination of HP0 with HP2, separate mux gates *S*3 and *S*2 are used, the bandwidth will be used efficiently.

The test results for Mode C are shown in Table V.

D. Mode D, Use Combined Dual-HP Ports HP0 and HP1

We can switch from Mode C to Mode D (combined dual HP ports HP0 and HP1) by replacing HP2 with HP1 in Fig. 20. The test results for Mode D are shown in Table VI.

In Mode C, the combination of HP0 and HP2 doubles the data rate approximately, compared with Mode B (single HP port), which is very useful for data-throughput with higher utilization of bus applications. When Mode D (combination of HP0 and HP1) is used, the utilization of bus is lower than 85% when FCLK0 is more than 142.9 MHz.

E. Mode E, Use Combined Quad HP Ports HP0 to HP3

The theoretical highest performance solution is the quad ports combined mode, which is called Mode E. All the four

TABLE V
TEST RESULTS IN MODE C WITH THE RAIN1000Z2 MODULE

FCLK0 (MHz)	Data Rate (MB/s)	(HP0+HP2) ports theoretical Bus Rate (MB/s)	Utilization of Bus (%)
50	719.8 ± 5.8	762.9	94.3 ± 0.8
100	1385.0 ± 18.3	1525.9	90.8 ± 1.2
142.9	1911.5 ± 35.8	2180.5	87.7 ± 1.6
166.7	2203.3 ± 57.4	2543.6	86.6 ± 2.3

TABLE VI
TEST RESULTS IN MODE D WITH THE RAIN1000Z2 MODULE

FCLK0 (MHz)	Data Rate (MB/s)	(HP0+HP1) ports theoretical Bus Rate (MB/s)	Utilization of Bus (%)
50	707.8 ± 5.6	762.9	92.8 ± 0.7
100	1350.0 ± 17.9	1525.9	88.5 ± 1.2
142.9	1842 ± 66.3	2180.5	84.6 ± 3.0
166.7	1874.0 ± 67.2	2543.6	73.7 ± 2.6

TABLE VII
TEST RESULTS IN MODE E WITH THE RAIN1000Z2 MODULE

FCLK0 (MHz)	Data Rate (MB/s)	Quad HP ports combined theoretical Bus Rate (MB/s)	Utilization of Bus (%)
50	1423.1 ± 4.3	1525.9	93.3 ± 0.3
76.9	2066.4 ± 34.0	2346.8	88.0 ± 1.4
100	2103.5 ± 36.8	3051.8	69.0 ± 1.2
142.9	2111.8 ± 22.4	4361.0	48.4 ± 0.5
166.7	2132.8 ± 18.8	5087.3	41.9 ± 0.4

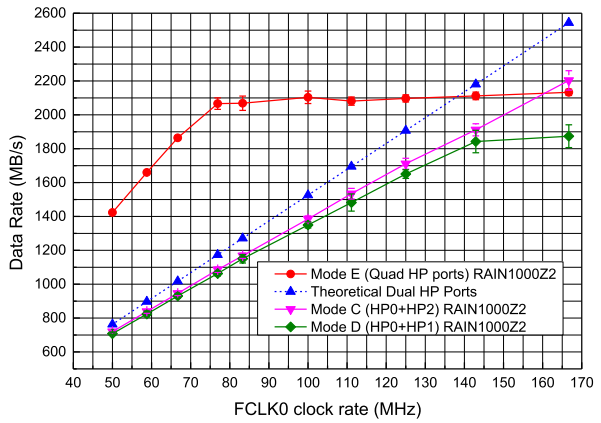

Fig. 22. Comparison of the test results using combined HP ports for the RAIN1000Z2 module.

HP ports are used for data exchange. The block diagram is shown in Fig. 18. The test results are shown in Table VII.

The results of Mode C to Mode E are compared and depicted in Fig. 22. The maximum data rate is limited by the memory interconnect bandwidth, which is 64-bit, 355 MHz, or 2840 MB/s. This is because the memory interconnect is the bridge between DDR Memory Controller and the associated HP logics. In Mode E, refer to Table VII and Fig. 22, the utilization of bus is lower than 85% when FCLK0 is about more than 80 MHz. Although the design of the PL is more complex, the data rate can reach approximately 2066 MB/s when the clock speed is as low as 76.9 MHz. This is useful for some specific applications that require relatively slow clock speeds and lower power consumption.

Mode C holds the maximum of the utilization of bus among Mode C, Mode D, and Mode E. In Mode C, the data rate is proportional to the FCLK0 speed. For readout applications, higher clock speed leads to higher data rate and higher power consumption.

VIII. CONCLUSION AND FUTURE WORK

A. Conclusion

The new RAIN1000Z2 readout module based on the ZYNQ XC7Z020 in a CLG400 footprint has more LVDS interfaces and a 32-bit DDR3 SDRAM interface. It has 60 LVDS pairs, which can support the interface of more or higher rate ADCs and DACs.

In addition, the 32-bit data width of the DDR3 SDRAM interface provides improvement in BRAM-to-DRAM data throughput and has no limitation up to 166.7-MHz FCLK0 clock rate. The data rate can reach about 1087 MB/s in Mode B (single HP port) and about 2203 MB/s in Mode C (combined dual HP ports).

In applications of readout electronics, which require higher data rate (for example, of more than 2000 MB/s) and deploy two combined HP channels, more than 10% improvement in data-throughput can be realized through Mode C relative to Mode D. This performance is higher than the theoretical bandwidth of PCI Express Gen2 x4 Lanes, which is 2000 MB/s (The typical actual efficiency of PCI Express Gen2 x4 Lanes performance is 85%–95%, due to the performance of the CPU and motherboard.) Refer Fig. 22, the dual-HP combined mode can reach the bandwidth performance of PCI Express Gen2 x4 Lanes at the clock speed of approximately 150 MHz. Moreover, not only the logic architecture but also the software and hardware development, is convenient to implement.

The most powerful mode is Mode E, with combined quad HP ports. It can provide more than 2000 MB/s data rate at a relatively low clock speed of approximately 75 MHz.

For applications that the data rate is lower than 500 MB/s, Mode A (the BRAM with a single GP port) is the simplest solution for readout.

B. Future Work

In the future, the new readout module based on the ZYNQ UltraScale family of FPGAs from Xilinx will be designed. Meanwhile, similar data-throughout performance tests will be processed.

Besides, power consumption of the readout module based on Xilinx ZYNQ is worthy of study. There are many factors that influence the power consumption, including module devices, interfacing with LVDS lines and so on.

A study on dynamic tuning of clock based on data rate is in processing. Compression technology can be used for input data so that DDR3 SDRAM can operate at lower data rate to

achieve lower power consumption. The DDR3 SDRAM and ZYNQ can be configured at different clock frequencies so that the firmware can meet requirements of high-instantaneous data rate while maintaining a relative low power consumption.

ACKNOWLEDGMENT

The authors would like to thank Prof. Y. Liu and Z. Deng, for support and discussions over the years in the Nuclear Electronics Laboratory, Department of Engineering Physics (DEP), Tsinghua University, Beijing, China. They would also like to thank the master hands and patient help of Y. Xue, W. Xue, and J. Zhang, who are technical engineers at the electrical workshop of DEP.

REFERENCES

[1] C. Yang, W. Zheng, M. Zhang, T. Yuan, G. Zhuang, and Y. Pan, "A real-time data acquisition and processing framework based on FlexRIO FPGA and ITER fast plant system controller," *IEEE Trans. Nucl. Sci.*, vol. 63, no. 3, pp. 1715–1719, Jun. 2016.

[2] K.-J. Kang *et al.*, "Introduction to the CDEX experiment," *Frontiers Phys.*, vol. 8, no. 4, pp. 412–437, Aug. 2013.

[3] L. Zhao *et al.*, "Design of the readout electronics prototype for LHAASO WCDA," in *Proc. IEEE-NPSS Real Time Conf. (RT)*, Jun. 2016, pp. 1–3.

[4] B. Wang, J. Du, X. Bi, and X. Tian, "High bandwidth memory interface design based on DDR3 SDRAM and FPGA," in *Proc. Int. SoC Design Conf. (ISOCC)*, Nov. 2015, pp. 253–254.

[5] Y. E. Mei and Z. Han, "Framework upgrade of the detector control system for JUNO," in *Proc. IEEE-NPSS Real Time Conf. (RT)*, Jun. 2016, pp. 1–3.

[6] F. Retiere *et al.*, "DEAP trigger and readout electronics," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2012, pp. 1802–1805.

[7] J.-M. André *et al.*, "Performance of the new DAQ system of the CMS experiment for run-2," in *Proc. IEEE-NPSS Real Time Conf. (RT)*, Jun. 2016, pp. 1–4.

[8] Y. Takubo *et al.*, "Development of SiTCP based DAQ system of double-sided silicon strip super-module," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 699, pp. 116–119, Jan. 2013.

[9] *PCI Local Bus Specification Revision 3.0*, Xilinx, Inc., San Jose, CA, USA, 2004. [Online]. Available: https://www.xilinx.com/Attachment/PCI_SPEV_V3_0.pdf

[10] B. K. Fawcett, "Designing PCI bus interfaces with programmable logic," in *Proc. 8th Annu. IEEE Int. Appl. Spec. Integr. Circuits Conf.*, Sep. 1995, pp. 321–324.

[11] H. Kavianipour, S. Muschter, and C. Bohm, "High performance FPGA-based DMA interface for PCIe," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 2, pp. 745–749, Apr. 2014.

[12] R. Szabó and A. Gontean, "Commanding a robotic arm on serial interface using Linux operating system running on FPGA," in *Proc. 12th IEEE Int. Symp. Electron. Telecommun. (ISETC)*, Oct. 2016, pp. 231–234.

[13] T. Xue, W. Pan, G. Gong, M. Zeng, H. Gong, and J. Li, "Design of Giga bit Ethernet readout module based on ZYNQ for HPGe," in *Proc. 19th IEEE-NPSS Real Time Conf. (RT)*, May 2014, pp. 1–4.

[14] T. Xue, M. Zeng, G. Gong, and J. Li, "8-channel 14-bit 125MHz FADC electronics with 1G Ethernet readout based on ZYNQ for HPGe detector," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Nov. 2014, pp. 1–2.

[15] T. Xue, G. Gong, and J. Li, "Readout system with 2-channel 8-bit 1GHz FADC based on RAIN1000Z1 ZYNQ module for crystal detector," in *Proc. IEEE-NPSS Real Time Conf. (RT)*, Jun. 2016, pp. 1–3.

[16] Xilinx, Inc. (Mar. 5, 2016). *Linux Drivers*. [Online]. Available: http://www.wiki.xilinx.com/Linux%20Drivers

[17] P. Pręd ki *et al.*, "EPICS-based visualisation and control in DAQ systems," in *Proc. 18th Int. Conf. Mixed Design Integr. Circuits Syst. (MIXDES)*, Jun. 2011, pp. 180–183.

[18] Analog Device, Inc. (2015). *Quad, 14-Bit, 80 MSPS/105 MSPS/125 MSPS Serial LVDS 1.8 V analog-to-digital converter*. [Online]. Available: http://www.analog.com/media/en/technical-documentation/data-sheets/AD9253.pdf.

[19] Texas Instruments, Inc. (2015). *ADC12D1/times00 12-Bit, 2.0/3.2 GSPS ultra high-speed ADC*. [Online]. Available: http://www.ti.com/lit/ds/symlink/adc12d1000.pdf

[20] T. Xue, G. Gong, and J. Li, "Combo FADC readout system with 8-channel 14-Bit 100MHz FADC and 2-channel 12-Bit 2GHz FADC for HPGe detector," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2015, pp. 1–2.

[21] Amphenol ICC, Inc. (2010). *MezzoStak 0.5 BTB Connector System*. [Online]. Available: https://cdn.amphenol-icc.com/media/wysiwyg/files/documentation/gs-12-577.pdf.

[22] E. Bogatin. *Signal and Power Integrity—Simplified*. Boston, MA, USA: Pearson Edu., Inc., 2009, pp. 81–90.

[23] Xilinx, Inc. (2016). *Zynq-7000 All Programmable SoC PCB Design Guide*. [Online]. Available: https://www.xilinx.com/support/documentation/user_guides/ug933-Zynq-7000-PCB.pdf

[24] D. Kirschberger, H. Flatt, and J. Jasperneite, "An architectural approach for reconfigurable industrial I/O devices," in *Proc. Int. Conf. ReConFigurable Comput. FPGAs (ReConFig)*, Dec. 2014, pp. 1–6.

[25] V. Sklyarov, I. Skliarova, J. Silva, and A. Sudnitson, "Analysis and comparison of attainable hardware acceleration in all programmable systems-on-chip," in *Proc. Euromicro Conf. Digit. Syst. Design (DSD)*, Aug. 2015, pp. 345–352.

[26] J. Silva, V. Sklyarov, and I. Skliarova, "Comparison of on-chip communications in Zynq-7000 all programmable systems-on-chip," *IEEE Embedded Syst. Lett.*, vol. 7, no. 1, pp. 31–34, Mar. 2015.

[27] Xilinx, Inc. (2015). *Xilinx MIG 7 Series DDR2 and DDR3 Performance Estimation Guide*. [Online]. Available: https://www.xilinx.com/Attachment/Xilinx_Answer_63234_MIG_Performance_Estimation_Guide.pdf