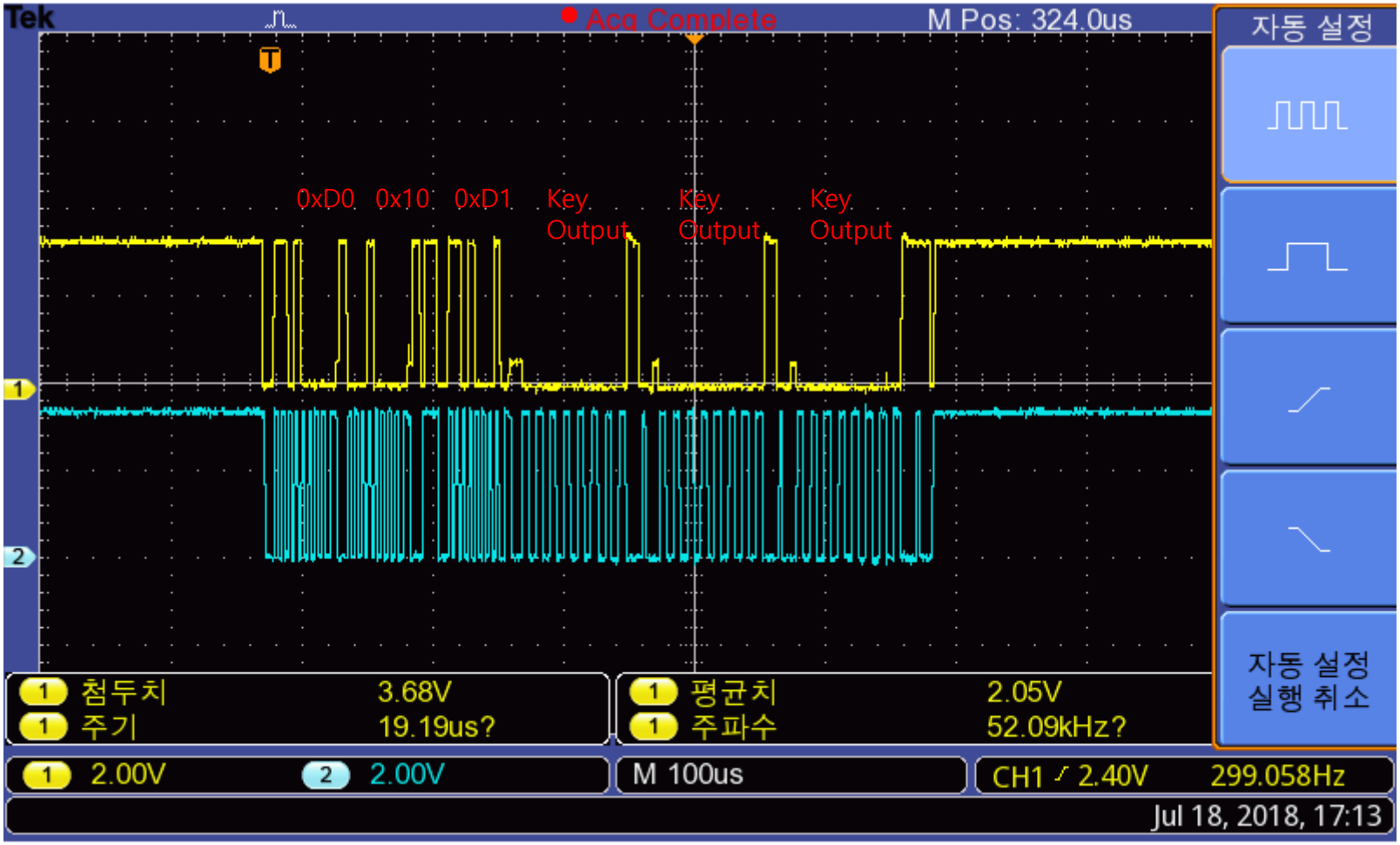
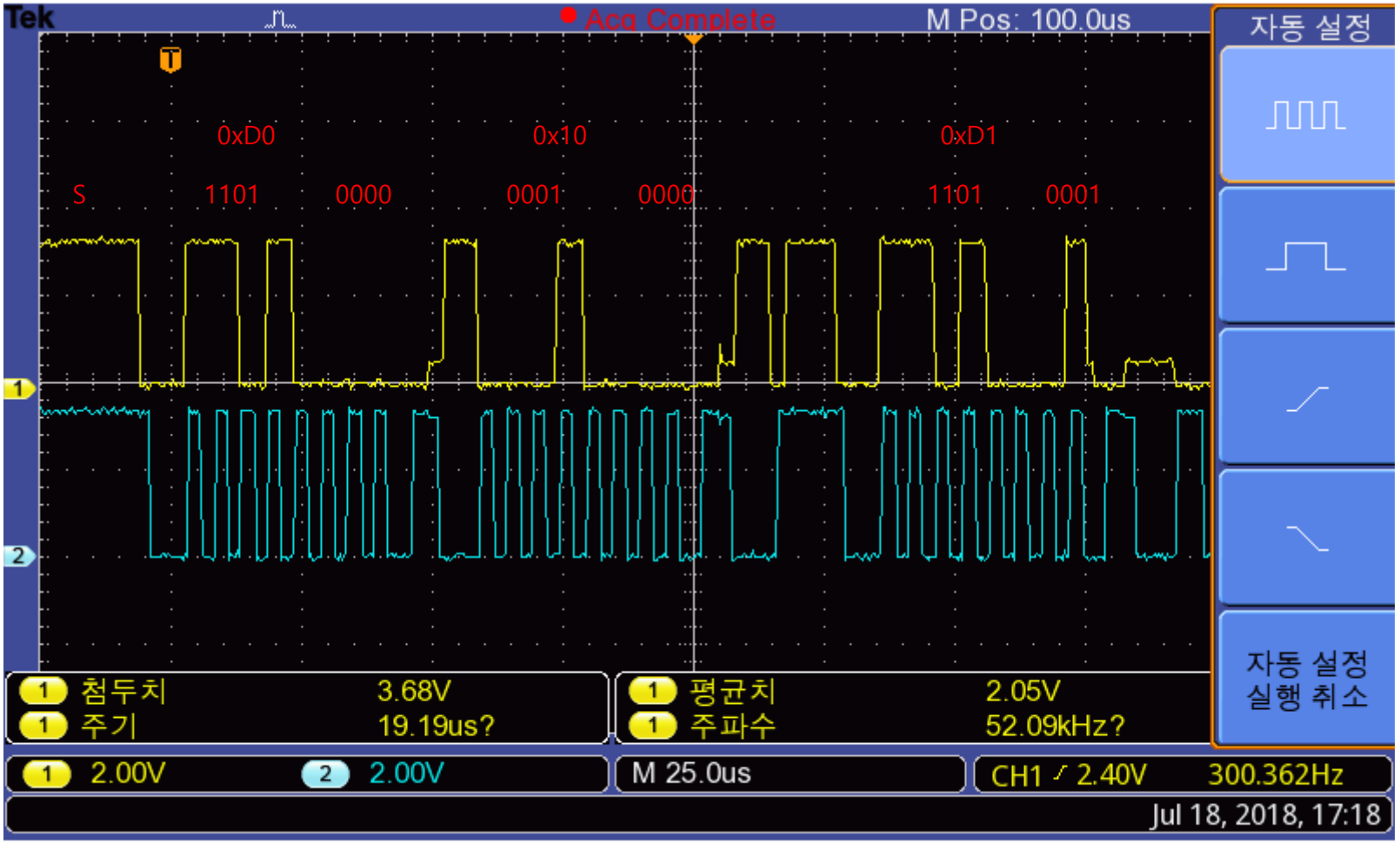
* TSM12 I2C 통신 파형

* TSM12 Chip Address 0xD0 (8bit)인 경우
* TSM12 Register 0x10h ~ 0x12h 번지의 3byte Data를 연속으로 read 하는 경우의 파형



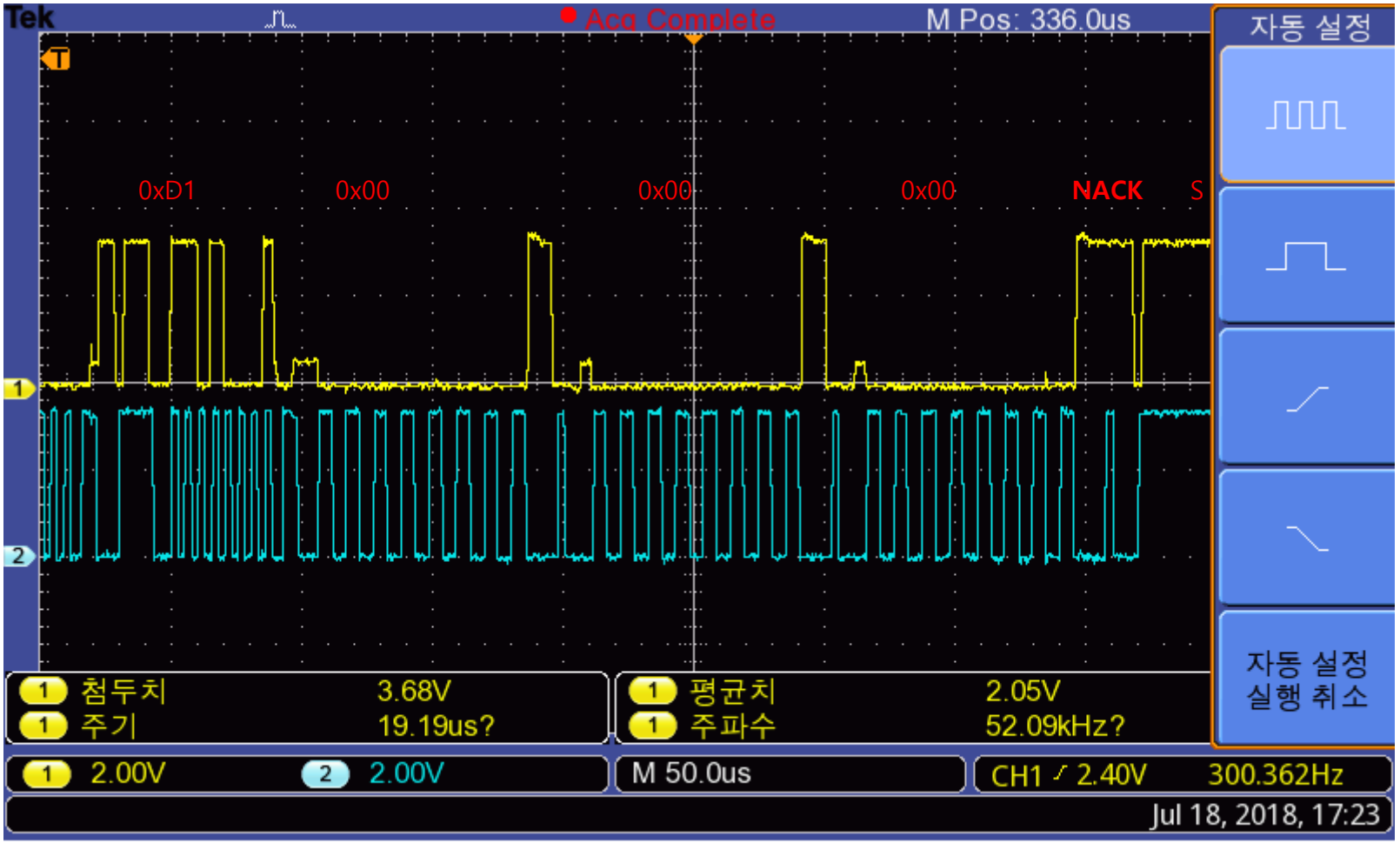
* TSM12 I2C 통신 파형

* TSM12 Chip Address 0xD0 (8bit)인 경우
* TSM12 Register 0x10h ~ 0x12h 번지의 3byte Data를 연속으로 read 하는 경우의 파형



* TSM12 I2C 통신 파형 (Touch Key 출력 부분)

* TSM12 Chip Address 0xD0 (8bit)인 경우
* TSM12 Register 0x10h ~ 0x12h 번지의 3byte Data를 연속으로 read 하는 경우의 파형



* TSM12 I2C 통신 파형 (Touch Key 출력 부분)

8.2.7 Output Register

Type: R

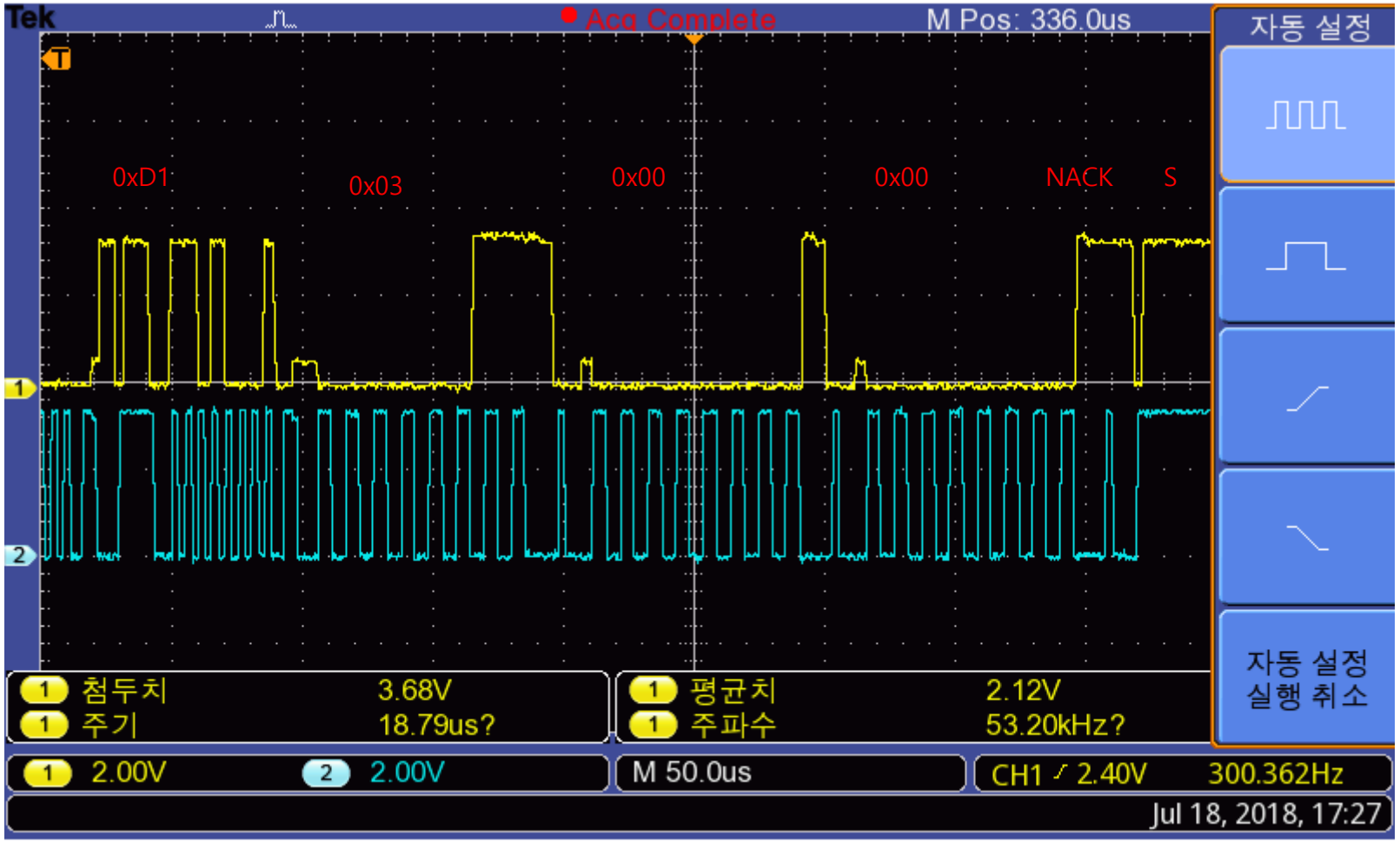
Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	output1	OUT4[1:0]		OUT3[1:0]		OUT2[1:0]		OUT1[1:0]	
11h	output2	OUT8[1:0]		OUT7[1:0]		OUT6[1:0]		OUT5[1:0]	
12h	output3	OUT12[1:0]		OUT11[1:0]		OUT10[1:0]		OUT9[1:0]	

Description

The each channel output of TSM12 is compressed with 2 bits. It has 3 level output information that is low, middle and high.

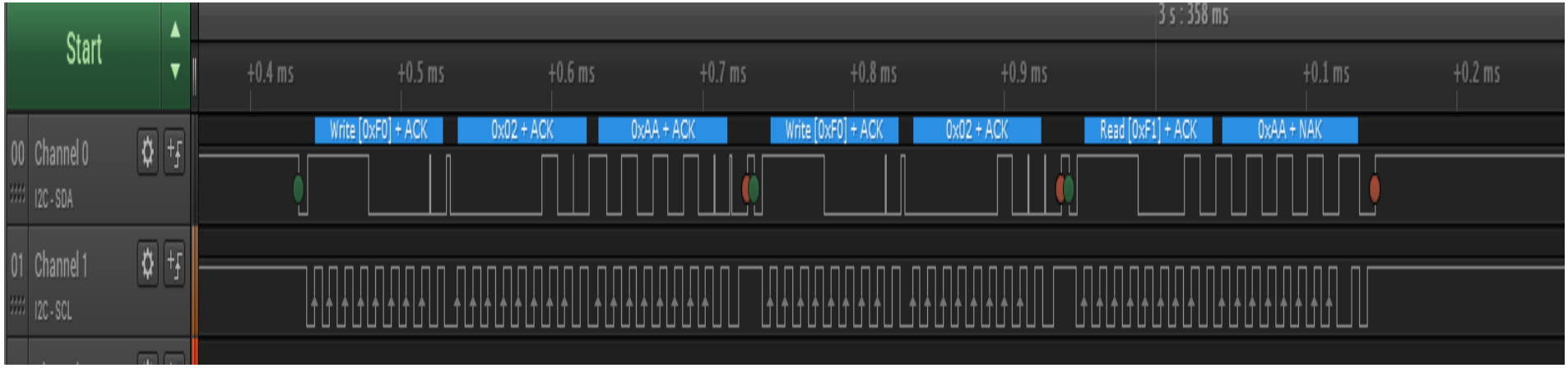
Bit name	Reset value	Function
OUT1[1:0] ~ OUT12[1:0]	00	Output of channels 00: No output 01: low output 10: middle output 11: high output

•ch1번 Key를 터치 하는 경우 0x03 Key Data 출력
(0x00, 0x01, 0x02, 0x03 출력 발생)



* TSM12 I2C 통신 파형 (Touch Key 출력 부분)

* TSM12 Chip Address 0xF0 (8bit)인 경우
* TSM12 Register 0x02h 번지에 0xAA 값을 write 하고, 다시 read 하는 경우의 파형



* TSM12 I2C 통신 파형 (Touch Key 출력 부분)

8.2.7 Output Register

Type: R

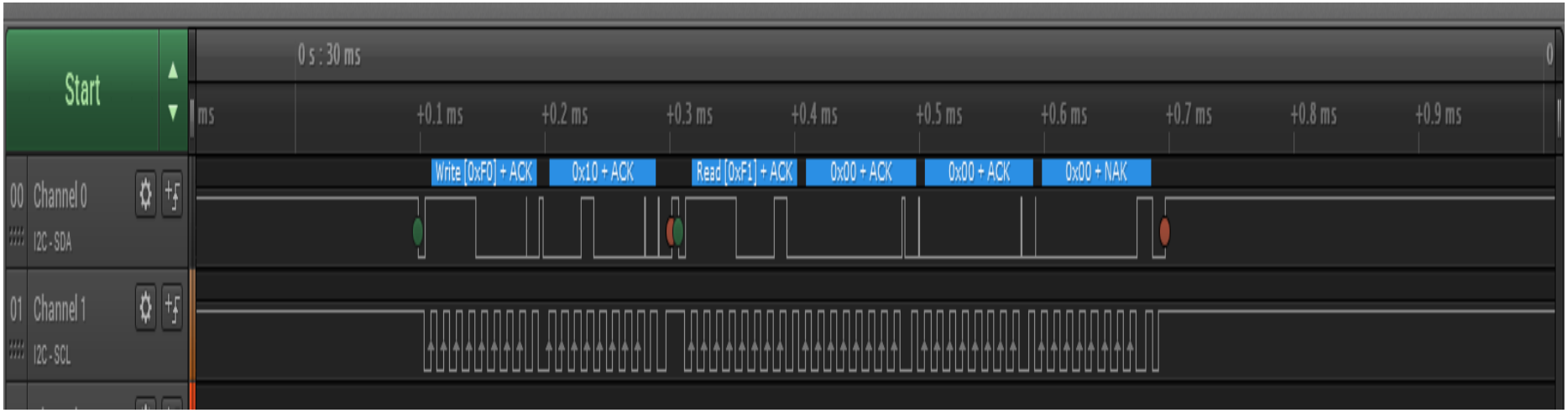
Address	Register Name	Bit7 Bit6	Bit5 Bit4	Bit3 Bit2	Bit1 Bit0
10h	output1	OUT4[1:0]	OUT3[1:0]	OUT2[1:0]	OUT1[1:0]
11h	output2	OUT8[1:0]	OUT7[1:0]	OUT6[1:0]	OUT5[1:0]
12h	output3	OUT12[1:0]	OUT11[1:0]	OUT10[1:0]	OUT9[1:0]

Description

The each channel output of TSM12 is compressed with 2 bits. It has 3 level output information that is low, middle and high.

Bit name	Reset value	Function
OUT1[1:0] ~ OUT12[1:0]	00	Output of channels 00: No output 01: low output 10: middle output 11: high output

* TSM12 Chip Address 0xF0 (8bit)인 경우
* TSM12 Register 0x10h ~ 0x12h 번지의 3byte Data를 연속으로 read 하는 경우의 파형



* TSM12 I2C 통신 파형 (Touch Key 출력 부분)

8.2.7 Output Register

Type: R

Address	Register Name	Bit7 Bit6	Bit5 Bit4	Bit3 Bit2	Bit1 Bit0
10h	output1	OUT4[1:0]	OUT3[1:0]	OUT2[1:0]	OUT1[1:0]
11h	output2	OUT8[1:0]	OUT7[1:0]	OUT6[1:0]	OUT5[1:0]
12h	output3	OUT12[1:0]	OUT11[1:0]	OUT10[1:0]	OUT9[1:0]

Description

The each channel output of TSM12 is compressed with 2 bits. It has 3 level output information that is low, middle and high.

Bit name	Reset value	Function
OUT1[1:0] ~ OUT12[1:0]	00	Output of channels 00: No output 01: low output 10: middle output 11: high output

* TSM12 Chip Address 0xF0 (8bit)인 경우

* TSM12 Register 0x10h ~ 0x12h 번지의 3byte Data를 연속으로 read 하는 경우의 파형