

Test result

1. Freuquency and LUTs cost

For 1024bit bus width, the timing slack is shown in Fig 1. LUTs cost is shown in Fig 2. For all the bus width, results is shown in Table 1.

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing ×			
Design Timing Summary			
General Information			
Timer Settings			
Design Timing Summary			
Clock Summary (5)			
Check Timing (1)			
Intra-Clock Paths			
Inter-Clock Paths			
Other Path Groups			
User Ignored Paths			
Unconstrained Paths			
Setup			
Worst Negative Slack (WNS): 0.226 ns			
Total Negative Slack (TNS): 0.000 ns			
Number of Failing Endpoints: 0			
Total Number of Endpoints: 19251			
Hold			
Worst Hold Slack (WHS): 0.033 ns			
Total Hold Slack (THS): 0.000 ns			
Number of Failing Endpoints: 0			
Total Number of Endpoints: 19203			
Pulse Width			
Worst Pulse Width Slack (WPWS): 0.000 ns			
Total Pulse Width Negative Slack (TPWS): 0.000 ns			
Number of Failing Endpoints: 0			
Total Number of Endpoints: 14604			
All user specified timing constraints are met.			

Fig 1. timing slack

Name	Slice LUTs (433200)	Slice Registers (866400)	Slice (108300)	LUT as Logic (433200)	LUT as Memory (174200)	LUT Flip Flop Pairs (433200)	Block RAM Tile (1470)	Bonded (85)
freq_test_top	8915	14355	3141	8706	209	7068	2.5	
dbg_hub (dbg_hub_CV)	428	709	200	404	24	274	0	
u_clk_wiz_0 (clk_wiz_0)	0	0	0	0	0	0	0	
u_data_source (data_...)	1039	1034	643	1039	0	1032	0	
u_ftag_axi_0 (ftag_axi_...)	590	1388	297	414	176	419	2.5	
u_resault (resault)	72	316	63	72	0	50	0	
u_test_top (test_top)	6790	10908	2567	6781	9	5275	0	
u_axi_hwicap_0 (ax_...)	186	688	146	186	0	99	0	
u_go_back_top (go_...)	6603	10220	2420	6594	9	5176	0	
u_go_back_pip_...	1775	1219	542	1775	0	539	0	
u_lut_pipe_top_...	4821	8962	1886	4820	1	4628	0	

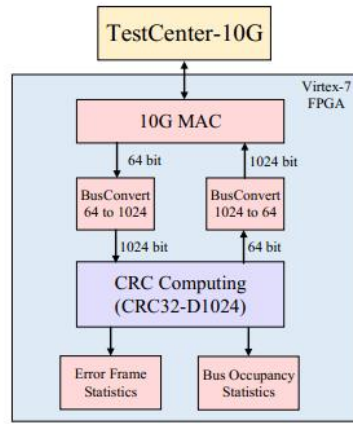
Fig 2. LUTs cost

Table 1 Results for all the bus width

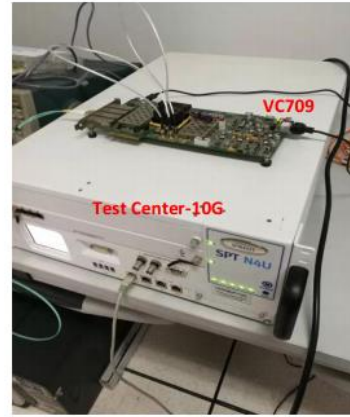
Bus Width	Fmax	LUTs	FFs	Timing Slack	Throughput
64	577.03	1488	1873	0.267	36.9
128	558.66	2042	2591	0.21	75.3
256	565.93	2910	3921	0.233	144.6
512	558.97	4265	6309	0.211	285.7
1024	563.7	6790	10908	0.226	577.2
2048	550.36	11706	20035	0.183	1126.4

4096	510.99	21110	37684	0.043	2088.9
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2. Board-level project



(a) System architecture.



(b) VC709 and TestCenter.

Fig 3 Board-level system architecture

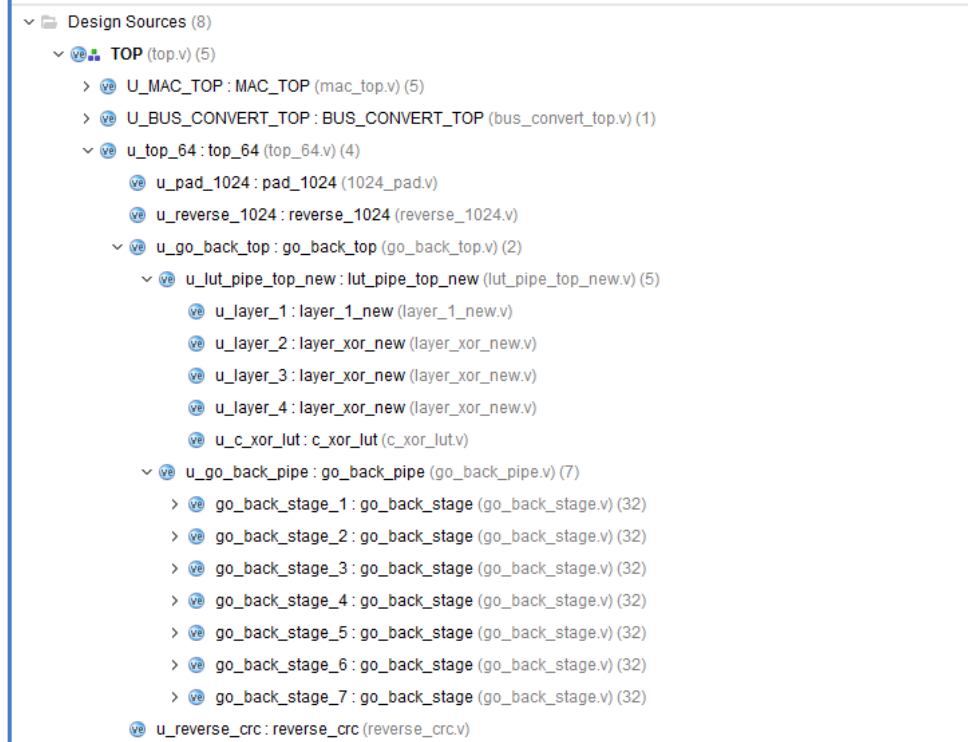


Fig 4 project file structure

3. Board-level test result

Table 2 Board-level test result

Frame length	64	128	256	512	1024	1518	random
L2 frames rate (Gbps)	7.62	8.65	9.28	9.62	9.81	9.86	9.75
Bus occupancy ratio	2.976%	1.689%	1.812%	1.879%	1.915%	1.943%	2.053%
Bandwidth consumed	15.24	8.65	9.28	9.62	9.81	9.95	10.51
Bus efficiency	50.00%	100.00%	100.00%	100.00%	100.00%	99.10%	92.77%
Frames (send)	124572593	93055550	30603445	29321297	8215975	6781626	32007145
Error frames (send)	24914448	18611110	6120689	5864243	1643193	1825363	6401425
Error frames checked	24914448	18611110	6120689	5864243	1643193	1825363	6401425