No	Month Task	Task	Description	Nov				Dec				Jan				Feb				Mar				April				May				June				July			
				1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
1	**build workflow, get familiar to the Env**	Linux Dev Env and board	get Nexys-Vedio board and build development enviroment of the project on linux																																				
		Risc-V Vivado Project	build risc-v vivado project and finish basic simulation				☆																																
2	**build Risc-V core and testify the communication between cores**	Risc-V core	build risc-v core and dowload it to the FPGA board																																				
		CAN controller core	build the CAN controller core form opencore																																				
		bare-metal program and test	build the bare-metal program of risc-v, basic BSP program to drive gpio like switches and leds and																																				
		CAN transceiver core	to make it possible to communicate on the board without a physical CAN transceiver, we need to																																				
		testify comm	verify the communication between two cores with CAN bus IP and its driver code										☆																											
3	**build 4-core risc-v 32 project and Wrap the can cantroller to a AXI mode to speed it up**	build 4-core prj	build 4-core risc-v block design and adjust the structure of the project																																				
		wrap CAN controller	wrap the CAN controller to AXI mode in order to speed up the control process																																				
		Interim Report(Jan 26)	Finish the Interim report and determine the structure of the project												☆																								
4	**build Ethernet Comm to PC and get fimiliar to the DNN ip core**	build Ethernet node and interface	build the Ethernet node on the board to send command and monitor the risc-v cores																																				
		build basic python script	build the python script on PC to operate the risc-v core, make it possible to download software and																																				
		build DNN core	get familiar and build the DNN core on the FPGA																																				
5	**error Injection and DNN detection data preparation**	inject errors to the CAN bus	inject errors like Dos, Replay, Spoofting to the CAN net with the software on PC																		☆																		
		data gathering	gather the data of CAN bus for training the DNN model and for pre-processing																																				
		DNN core utilization	utilize the DNN core to detect the attack on the CAN bus, build the basic framework																																				
6	**build benchmark of the DNN model**	build benchmark of the DNN model	build benchmark of the DNN model																																				
		Milestone Progress Report(April 24)	Milestone Progress Report																								☆												
7	**progress Presentation**	Progress Presentation(May 17)	Progress Presentation																												☆								
8	**Written Dissertation**	Dissertation(1st version)	Written Dissertation(1st version)																																☆				
9	**Written Dissertation**	Dissertation(final version)(July 12)	Written Dissertation(final version)																																		☆		