



**Trinity College Dublin**  
Coláiste na Tríonóide, Baile Átha Cliath  
The University of Dublin

# Hardware-In-The-Loop Emulator For In-Vehicle Controller Area Networks

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# Background & Project goals

## Problem Recap

### ■ Background



Hackers Remotely Kill a Jeep on the Highway (2015 USA)

### ■ Project goals

In this project, we will build a **hardware in the loop runtime for vehicular ECUs** using a RISC-V / Microblaze softcore processor as the compute core for each ECU. We will integrate the **ability to inject errors (like DoS, replay and spoofing) into the emulation framework** with multiple ECUs spread across one or more FPGA development boards.

Increased  
Network  
Complexity



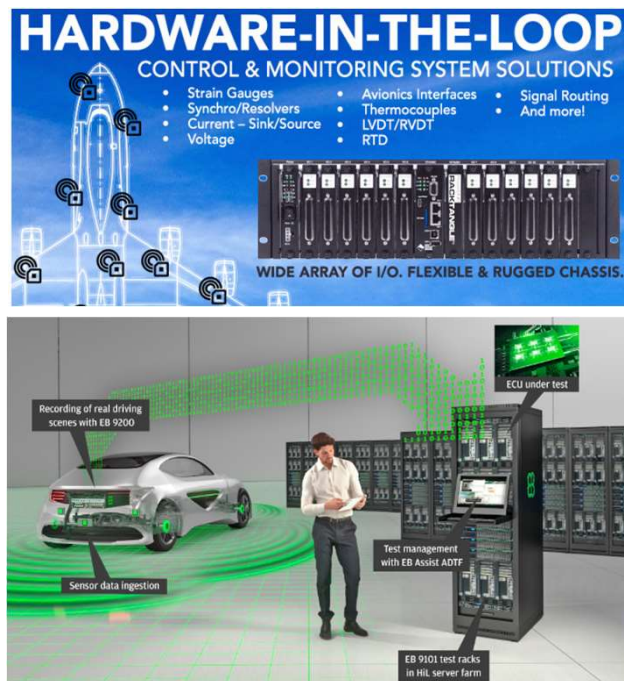
Increased  
Cyber Security  
Risk

A hardware-in-the-loop emulator  
for vehicle bus attack simulation & prevention

Hacker exposed the security vulnerabilities in automobiles by hacking into cars remotely, controlling the cars' various controls from the radio volume to the brakes on Wednesday, July 1, 2015 in Ladue

# Previous work & Novelty

## Previous work - HWIL



**Hardware-in-the-loop simulation** was first used in the **1960s** in the **aerospace field**, it was used to test flight control systems, and now it is also widely used in the automotive field.[1]

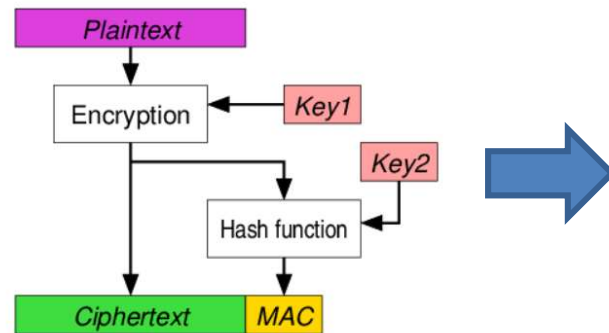
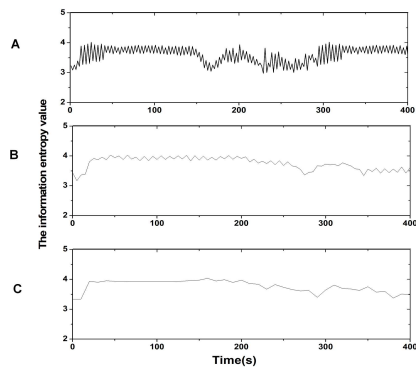
The applications in the **automotive field**, HIL provides a virtual vehicle for **system-level verification**.

Virtual ECU technology is a hot topic

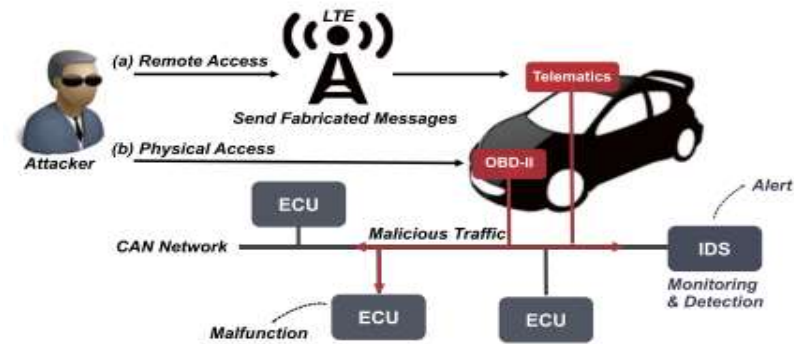
[1] S Raman, N Sivashankar, W Milam, W Stuart, and S Nabi. Design and implementation of hil simulators for powertrain control system software development. In Proceedings of the 1999 American Control Conference (Cat. No. 99CH36251), volume 1, pages 709–713. IEEE, 1999

# Previous work & Novelty

## Previous work – attack detection



### Traditional Detection & Encryption



### IDS & DNN detection

Neural networks have greatly improved attack detection performance,

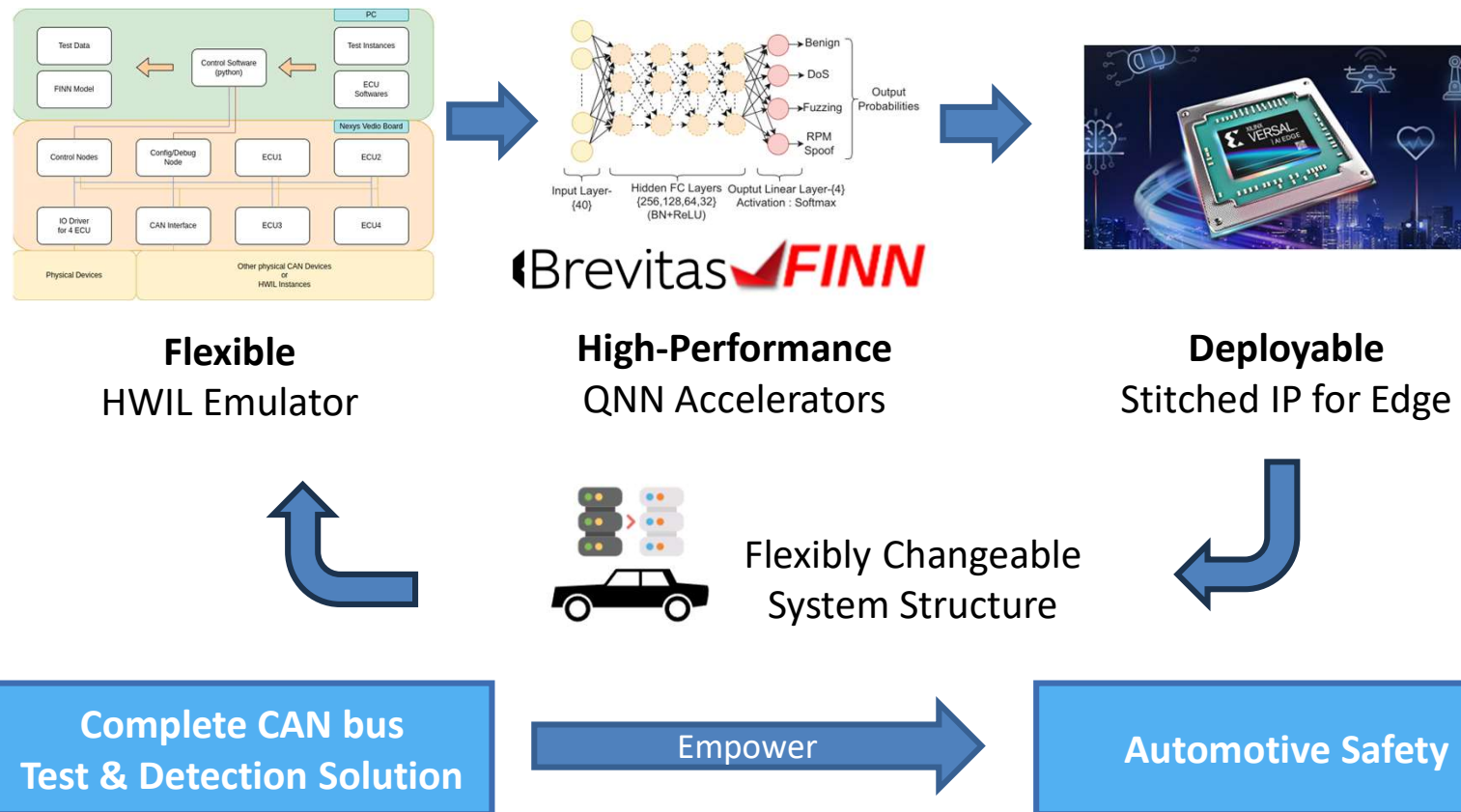
But how to deal with **flexible system (Topo change -> Feature change)**

Agile attack simulation & model building toolchain  
to be developed

Method	Precision (%)		Recall (%)		F1-Score (%)	
	Known	New	Known	New	Known	New
OCSVM	35.43	10.83	71.15	35.12	47.30	16.55
IF	43.58	15.62	73.42	31.56	54.69	20.90
OTIDS	<b>99.82</b>	70.81	71.68	42.01	83.44	52.73
RNN+Heuristics	98.69	70.25	<b>99.49</b>	50.53	<b>99.09</b>	58.78
<b>CANTransfer</b>	94.93	<b>87.97</b>	95.57	<b>88.97</b>	95.25	<b>88.47</b>
Gain	-4.89	<b>17.16</b>	-3.92	<b>38.44</b>	-3.84	<b>26.69</b>

# Progress Review

## Project Structure



# Progress Review

## Milestone Review

### Gantt Chart

				Nov				Dec				Jan				Feb				Mar				April				May				June				July			
No	Month Task	Task	Description	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	
1	build workflow, get familiar to the Env	Linux Dev Env and board	get Nexys-Veddo board and build development environment of the project on linux																																				
		Risc-V Vivado Project	build risc-v vivado project and finish basic simulation																																				
2	build Risc-V core and testify the communication between cores	Risc-V core	build risc-v core and dowload it to the FPGA board																																				
		CAN controller core	build the CAN controller core form opencore																																				
		bare-metal program and test	build the bare-metal program of risc-v, basic BSP program to drive gpio like switches and leds and to make it possible to communicate on the board without a physical CAN transceiver, we need to																																				
		CAN transceiver core	verify the communication between two cores with CAN bus IP and its driver code																																				
		testify comm																																					
3	build 4-core risc-v and microblaze project and Wrap the can controller to a AXI mode to speed it up	build 4-core prj	build 4-core risc-v block design and adjust the structure of the project																																				
		wrap CAN controller	wrap the CAN controller to AXI mode in order to speed up the control process																																				
		Interim Report(Jan 26)	Finish the Interim report and determine the structure of the project																																				
4	build Comm to PC and get familiar to the DNN ip core	build Ethernet node and interface	build the Ethernet node on the board to send command and monitor the risc-v cores																																				
		build basic python script	build the python script on PC to operate the risc-v core, make it possible to download software and																																				
		build DNN core	get familiar and build the DNN core on the FPGA																																				
5	error Injection and DNN detection data preparation	inject errors to the CAN bus	inject errors like Dos, Replay, Spoofing to the CAN net with the software on PC																																				
		data gathering	gather the data of CAN bus for training the DNN model and for pre-processing																																				
		DNN core utilization	utilize the DNN core to detect the attack on the CAN bus, build the basic framework																																				
6	build benchmark of the DNN model	build benchmark of the DNN model	build benchmark of the DNN model																																				
		Milestone Progress Report(April 24)	Milestone Progress Report																																				
7	deploy the core on the FPGA progress Presentation	Progress Presentation(May 17)	Progress Presentation																																				
8	Written Dissertation	Dissertation(1st version)	Written Dissertation(1st version)																																				
9	Written Dissertation	Dissertation(final version)(July 12)	Written Dissertation(final version)																																				

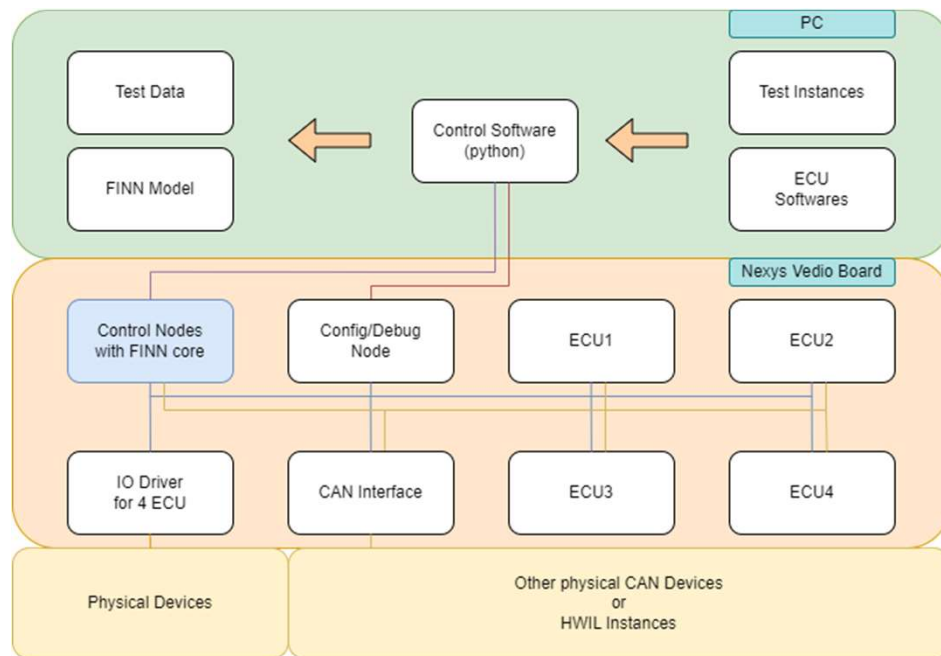
### Main goals

- Virtual ECU cores & Control logic
- Virtual CAN bus network
- Attack Injections
- Attack detection model
- Hardware Accelerators
- Benchmarking



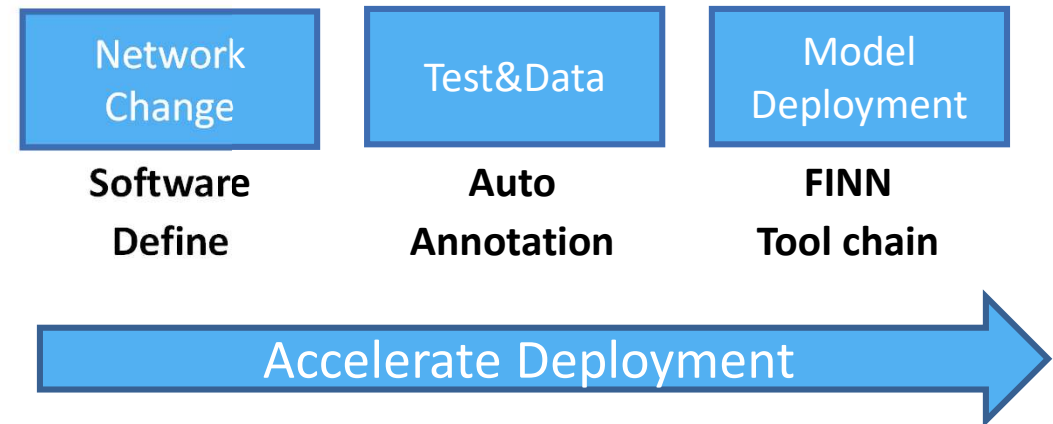
# Progress Review

## HWIL Emulator - Structure



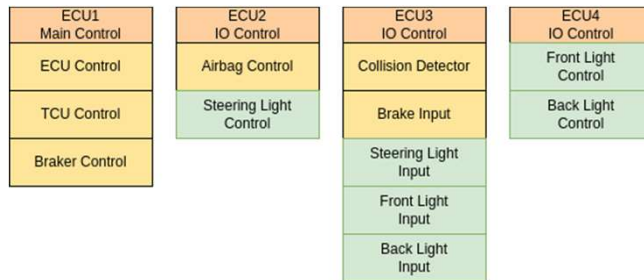
**HWIL Emulator Structure**

- Flexible nodes(type, scale)
- Physical device access
- Automatic testing
- Complete tool chain



# Progress Review

## Virtual ECUs



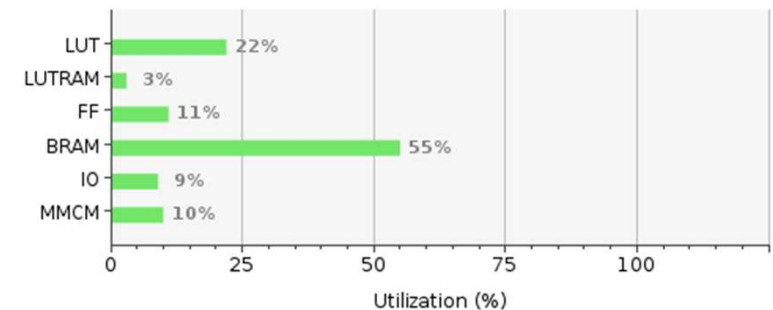
Simulating CAN bus topology



Hardware Implementation Platform



Soft MCU Core: AMD Microblaze

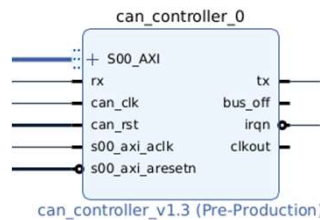


Effective Resource Utilization - Scalable



# Progress Review

## Virtual CAN BUS network

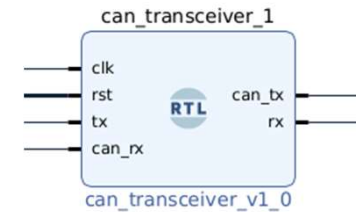


**AXI CAN controller IP core**

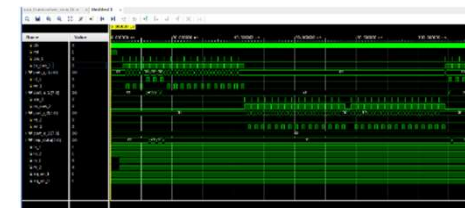
```

245 void can_init(uint32_t can_addr);
246 void can_set_pin(uint32_t can_addr, uint8_t pin, uint8_t value);
247 void can_set_data(uint32_t can_addr, uint8_t value);
248 uint8_t can_read_data(uint32_t can_addr);
249 void write_register(uint32_t can_addr, uint8_t reg_addr, uint8_t reg_data);
250 uint8_t read_register(uint32_t can_addr, uint8_t reg_addr);
251 void can_txd(uint32_t can_addr);
252 void can_rxd(uint32_t can_addr);
253 void can_txd_frame(struct can_data_frame *frame);
254 struct can_data_frame initialize_can_data_frame(addr1, addr2, addr3, can_addr);
255 void can_rxd_frame(struct can_data_frame *frame);
    
```

**Standard driver**



**CAN transceiver IP core**

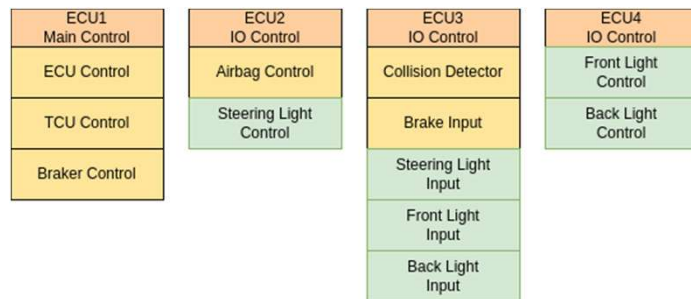


**IP core timing simulation**

# Progress Review

## Virtual ECU control logic

### Virtual communication protocol



	A	B	C	D	E	F	G	H	I	J	K
1				7	6	5	4	3	2	1	0
2	0	0	0	CAN mode =1 extend	Data Type =0 data						
3	1		1								
4	2		2								
5	3	1	3								
6	4		4								
7	5	2	5								
8	6		6								
9	7	3	7								
10	8	4	8								
11	9		9								
12	10		10								
13	11	5	11								
14	12	6	12								

Build up 4 ECUs with different logic for the test.  
All ECUs: Generate Life signal to indicate that they are alive.  
periodically send status messages to report their status.

**ECU1:** Control Engines, transmission unit and brake unit.

**ECU2:** Control Airbags and Steering Lights.

**ECU3:** Physical IO inputs, receive the signal from the sensors like Collision detector, brake detector, Lights control switches

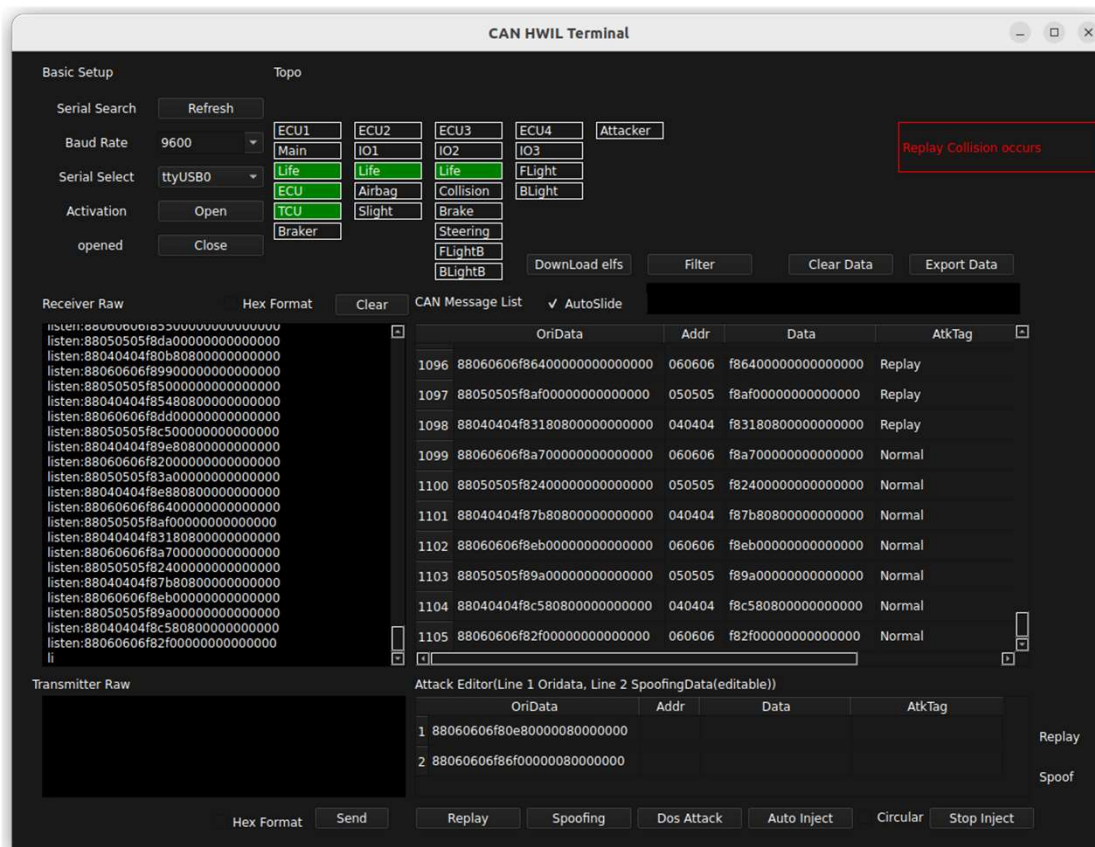
**ECU4:** Control Front light and back light of the car.

All the ECUs communicate with CAN bus.

**Building a virtual communication protocol And build ECU collaborative applications**

# Progress Review

## ECU Attack Test Platform



Status Monitor



ECU Program



Auto Injection



Labeled Data Export

No	Type	Msg
1	Dos	88000000f800000000000000
2	Spoofing	88040404f81580880400800030
3	Replay	88040404f81580880000000000
4	Dos	88000000f800000000000000
5	Dos	88000000f800000000000000
6	Dos	88000000f800000000000000
7	Spoofing	88040404f81580880400800030

Attack Sequence

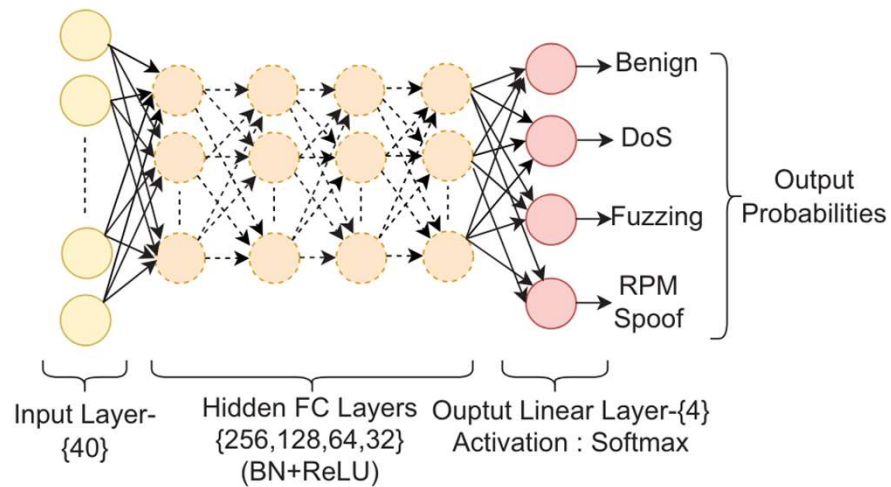
239	237,0505,8,21,00,00,00,00,00,00,Normal
240	238,0606,8,85,00,00,00,00,00,00,Normal
241	239,0404,8,af,00,00,00,00,00,00,Dos
242	240,0505,8,96,00,00,00,00,00,00,Dos
243	241,0606,8,c9,00,00,00,00,00,00,Dos
244	242,0404,8,f9,00,00,00,00,00,00,Dos
245	243,0505,8,0b,00,00,00,00,00,00,Dos

Labeled data for training

# Progress Review

## Model and performance

Successive  
CAN Message  
(ID + Payload)



**Mature**  
**Flexible & Deployable & High-performance**  
**CAN bus Attack detection model [1]**

Attack	Model	Precision	Recall	F1	FNR
DoS	GIDS [30]	-	99.9	-	-
	DCNN [13]	100	99.89	99.95	0.13
	MLIDS [36]	99.9	100	99.9	-
	G-IDCS [28]	99.81	98.86	99.33	-
	TAN-IDS [29]	100	100	100	-
	HyDL-IDS [33]	100	100	100	0
	NovelADS [32]	99.97	99.91	99.94	-
	TCAN-IDS [31]	100	99.97	99.98	-
	iForest [35]	-	-	-	-
Fuzzing	GRU [34]	99.93	99.91	99.92	-
	CQMLP-IDS	99.92	99.88	99.90	0.11
	GIDS [30]	-	98.7	-	-
	DCNN [13]	99.95	99.65	99.80	0.5
	MLIDS [36]	99.9	99.9	99.9	-
	G-IDCS [28]	99.71	99	99.35	-
	TAN-IDS [29]	99.99	99.99	99.99	-
	HyDL-IDS [33]	99.98	99.88	99.93	-
	NovelADS [32]	99.99	100	100	-
RPM-Spoof	TCAN-IDS [31]	99.96	99.89	99.22	-
	iForest [35]	95.07	99.93	97.44	-
	GRU [34]	99.32	99.13	99.22	-
	CQMLP-IDS	99.93	99.69	99.81	0.27
	GIDS [30]	-	99.6	-	-
	DCNN [13]	99.99	99.94	99.96	0.05
	MLIDS [36]	100	100	100	-
	G-IDCS [28]	99.85	98.69	99.27	-
	TAN-IDS [29]	99.99	99.93	99.96	-
RPM-Spoof	HyDL-IDS [33]	100	100	100	0
	NovelADS [32]	99.9	99.9	99.9	-
	TCAN-IDS [31]	99.9	99.9	99.9	-
	iForest [35]	98.9	100	99.4	-
	CQMLP-IDS	99.96	100	99.98	0

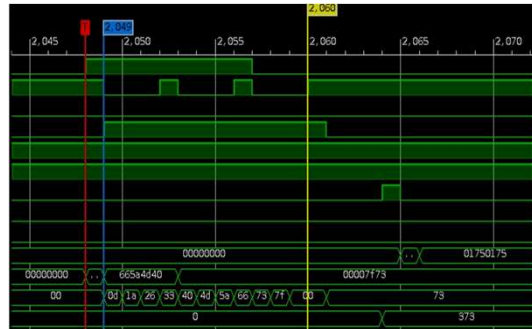
[1] Shashwat Khandelwal and Shanker Shreejith. Exploring highly quantised neural networks for intrusion detection in automotive can. In 2023 33rd International Conference on Field-Programmable Logic and Applications (FPL), pages 235–241. IEEE, 2023

# Progress Review

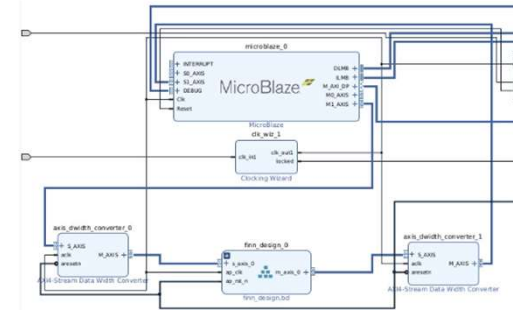
## Model integration and testing



### FINN Flow for light-weight platforms



Model data ILA capture



### Microblaze calls FINN IP via AXI-Stream

```

100: # in_X = np.zeros((1,10), dtype=np.float32)
    in_X = np.array([0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.], dtype=np.float32)
    # in_X = np.zeros((1,10), dtype=np.float32)
    # in_X = np.array([0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.], dtype=np.float32)
    # in_X = np.zeros((1,10), dtype=np.float32)
    in_X = in_X.reshape((1,10))

    input_dict = {}
    input_dict["global_in"] = in_X

    output_dict_fpl_23 = exe.execute_omni(fpl_model, input_dict, return_full_exec_context=True)
    print(output_dict_fpl_23)
    fpl_23_out = np.array(output_dict_fpl_23.get("global_out"))
    print(fpl_23_out)

    ('global_in': array([[0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.], dtype=float32], 'global_out': array([[0.61278073]], dtype=float32),
    'Add_0_param': array([-0.99550817], dtype=float32), 'Mul_0_out': array([[0.98834889]], dtype=float32), 'MatMul_0_param': array([[
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# Progress Review

## JLR Testing Tech Week - Share Fair



**Participate in Jaguar Land Rover testing technology sharing fair and demonstrated the project**



# Progress Review

## Milestone modification

- **Original plan:** Using **Risc-V rocket** soft core simulation ECU
- **Plan after the change:** Using **Microblaze** as ECU soft core
- **Reason for change:** Microblaze is more suitable for Xilinx ecosystem, which is **convenient for debugging and driver coding**. Microblaze is gradually beginning to support **Risc-V** instruction set.
- **Original plan:** Adopt the standard FINN integrated flow integrated attack detection core
- **Plan after the change:** Slightly behind schedule with custom build flows that can target both lightweight and traditional FPGAs
- **Reason for change:** Makes the project more **versatile**, but the custom workflow is slightly more complicated than the standard integration process

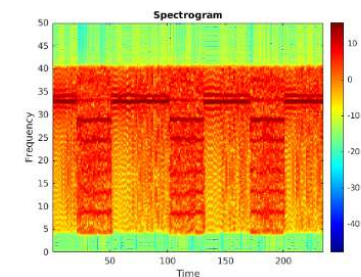
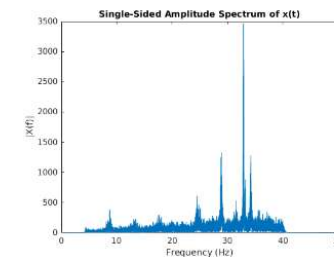
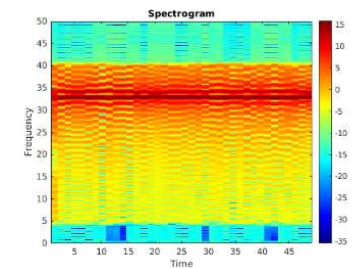
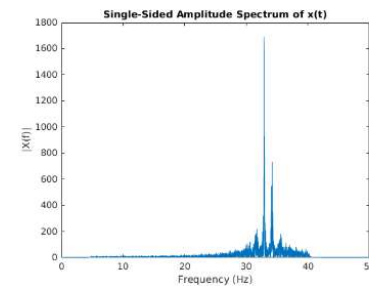
Functions such as automated attack injection, data export, and attack detection IP core hardware deployment were not originally planned, but were added for engineering integrity and usability.

# Plan for the rest of the project

## Next step

- Performance optimization
- Resource utilization optimization
- Ablation experiment
- Quantization effect
- Acceleration test

Model benchmarking and optimizing



Testing and comparison of other methods  
(like using STFT with DNN for attack detection)

Of course, there is also thesis writing, refer to the previous Gantt chart plan



**Trinity College Dublin**  
Coláiste na Tríonóide, Baile Átha Cliath  
The University of Dublin

# Thank You

**Changhong Li**  
**Supervisor: Shreejith Shanker**

Date 23/05/2024

