FSM Design Review

FSM Design

- Simple example in class to demonstrate design strategy and coding styles
- Example: Traffic Light Controller
  - Sequence "**Green** – **Amber** – **Red** – **Green** – **Amber** …"
  - Duration of each light is on should vary

Design Process

- Decide inputs and outputs
  - Input: use counter to control state transitions
  - Output: must control lights and state duration
- Decide states, control of state transitions and outputs
  - Moore or Mealy?
  - Document in state graph or ASM

Draw your own state graph now!

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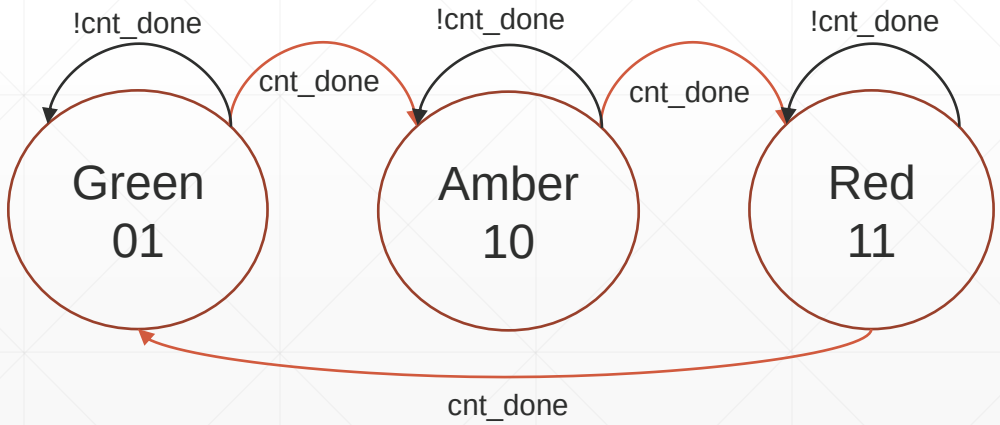
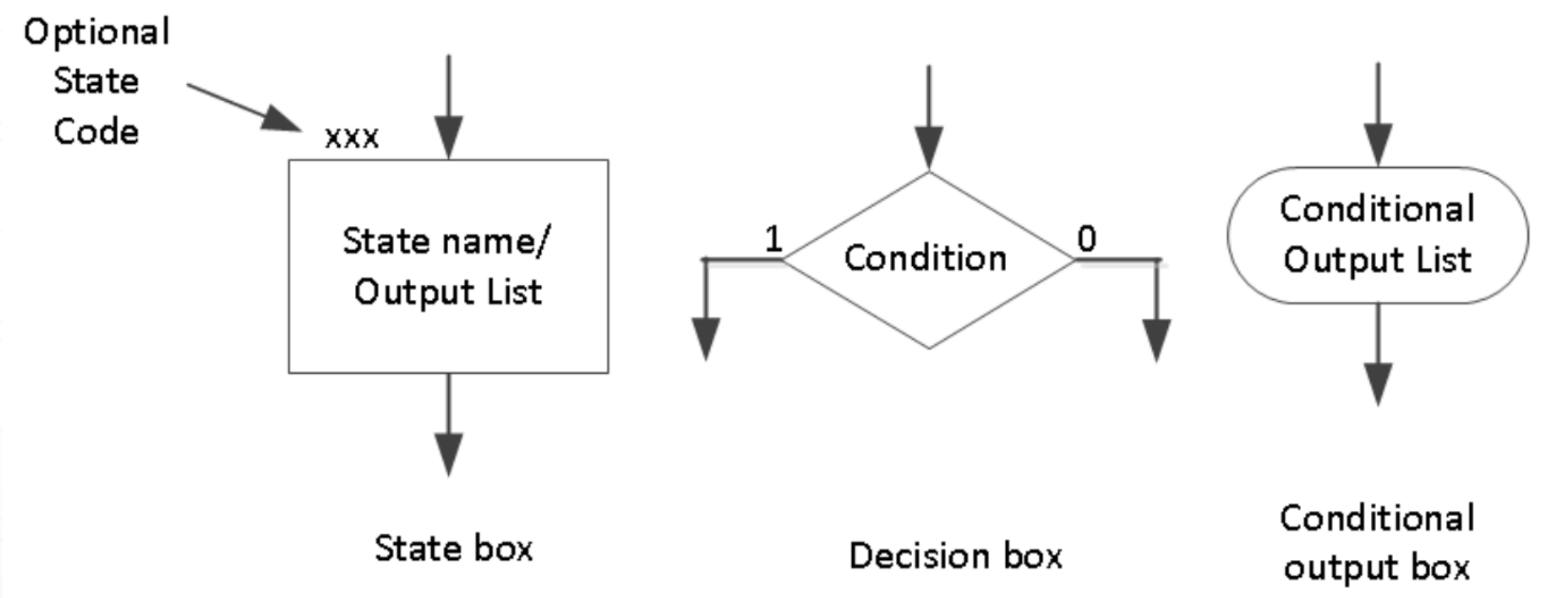
Moore State Graph:

Input:
- cnt_done (Flag from counter block to move state)

Outputs:
- current_state (01 = green, 10 = Amber, 11 = Red)



Algorithmic State Machine (ASM)



https://www.xilinx.com/support/documentation/university/Vivado-Teaching/HDL-Design/2015x/VHDL/docs-pdf/lab11.pdf
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In-Class Demo:
FSM Example Code and Basic Testbench

- Coding style – can choose to separate next state logic and output definitions
- Registering outputs
  - Why is this a good general coding practice?