

## Lab4 Report

### • A brief description of the filter you created in Vivado HLS

We firstly create a function named `sobel_accel` which has the `AXI_STREAM` input and output arg. The `sobel.cpp` includes `sobel.h` which contains some libraries like HLS video and some parameter definition.

In the function, we use HLS data-flow and implement these:

1. Transefer the video to matrix;
2. Convert the color from source matrix to gray matrix.
3. Utilize Gaussian Blur with a windows size 3x3.
4. Copy the matrix to 2 matrix.
5. Utilize Sobel function which is include in HLS library to finish the filtering in x and y dimension.
6. Convert the scale and take absolute value of x and y value
7. Add the result of sobel in x direction an in y direction with same weight to get the final result
8. Transfer the gray image back to BGR image
9. Transfer the result to AXI format and send it to the output stream.

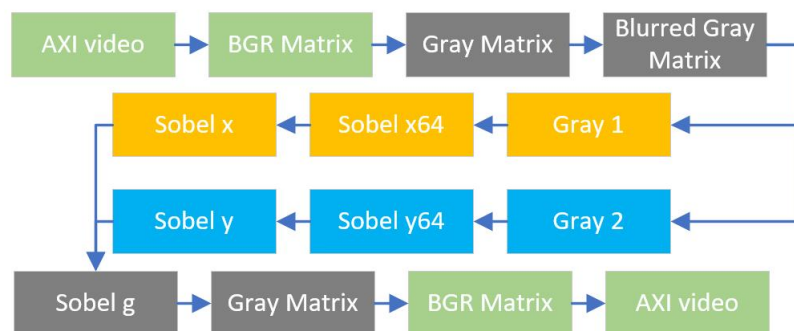


Figure 1. Flow chart of the filter

### • Screenshots of your overlay and describe the role of each IP

The Screenshots of my overlay is shown as below.

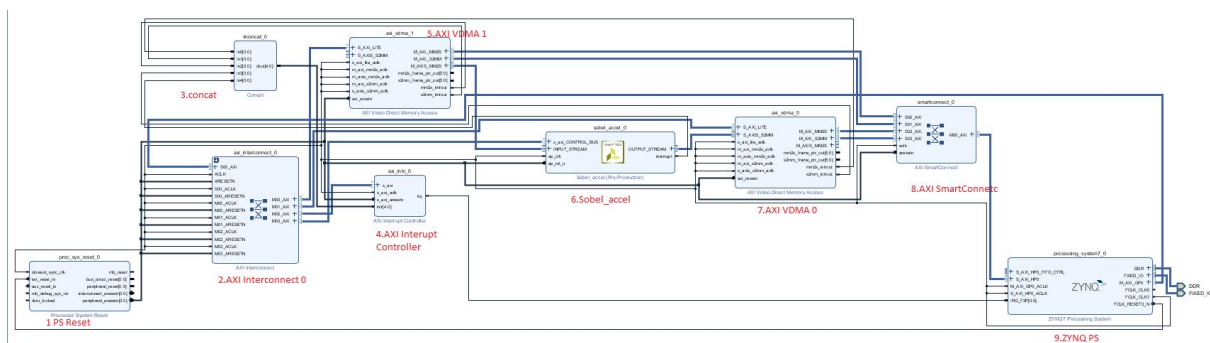


Figure 2. Screenshot of my overlay

### 1. PS Reset

The IP to reset Processer System.

### 2. AXI Interconnect 0

Connect the interface of PS and PL to transfer data.

The AXI Interconnect IP connects one or more AXI memory-mapped master devices to one or more AXI memory mapped slave devices.

### 3. Concat

Convert the interrupt signal of each part to a [4:0] signal in order to feed AXI interrupt controller.

Concatenates up to 32 ports into a single port.

### 4. AXI Interrupt Controller

Generate an interrupt request from the PL to PS.

The Logical CORE IP AXI Interrupt Controller (AXI INTC) core concentrates multiple interrupt inputs from peripheral devices to a single interrupt output to the system processor.

### 5. AXI VDMA1

Transfer input picture data from processing system (python script) to sobel acc core.

### 6. Sobel Acc

The IP core we generated to finish the sobel operation.

### 7. AXI VDMA 0

Transfer output picture data from sobel acc core to processing system (python script).

### 8. AXI Smart Connect

The AXI Smart Connect IP connects one or more AXI memory-mapped master devices to one or more AXI memory-mapped slave devices

### 9. ZYNQ PS

ZYNQ Processing system which carries the operating system running python script.

#### • Include the image you used before and after processing

The Images I used for the processing and after processing are shown as below.



**Figure 3. Image before and after processing**