UNIVERSITY OF DUBLIN

TRINITY COLLEGE

FACULTY OF ENGINEERING, MATHEMATICS & SCIENCE

SCHOOL OF ENGINEERING

Electronic & Electrical Engineering

Senior Sophister
Engineering
Annual Examinations

Hilary Term, 2015

INTEGRATED SYSTEMS DESIGN (4C1)

Date: 5th January 2015 **Venue: Luce Upper** **Time: 9.30 – 11.30**

Assistant Professor Naomi Harte

Answer FOUR questions in total.
Question 1 is COMPULSORY.
Answer any THREE of the remaining questions.

All questions carry equal marks

Permitted Materials:

Calculator
Drawing Instruments
Graph Paper

Q.1

(a) Convert -0.244140625 to an appropriate 8-bit representation, stating the representation used and highlighting any rounding or truncation used.

(b) An 8-bit and 10-bit number are multiplied. Assuming no sign bit in either number, what is the maximum bit width of the result?

(c) What is the primary difference between Verilog tasks **$monitor** and **$display** ?

(d) How does the ADC impact filter performance in a digital system?

(e) If memory is described as *volatile*, what does this mean?

(f) What is the advantage of distributed arithmetic for multipliers on FPGAs?

(g) Outline briefly the difference between distributed RAM and block RAM.

(h) What 3 functions are LUTs typically used to realise in FPGA based hardware?

(i) If flexibility is the major design constraint, which is more suitable: Soft IP or Hard IP? Explain briefly.

(j) What potential synthesis issue can you see with this snippet of Verilog code?

```
always @ *
 begin
 if (sel == 1)
  f = a;
 end
```

[25 marks]

Q.2

(a) The plots in Figure Q2 (A), (B), (C) and (D) (overleaf) show the magnitude responses of four FIR lowpass filters. One of the filters is not quantised. This filter was designed with a sampling rate of 20kHz, and passband and stopband frequencies of 2000Hz and 2350Hz respectively. The original 120 filter coefficients were quantised in different ways to obtain the remaining three filters.

By inspecting the magnitude responses of these 4 filters:

i. Identify which of the filters is not quantised.

ii. Of the remaining filters, match the filters to the following levels of coefficient quantisation in terms of LSB: 2^{-16}, 2^{-10}, 2^{-6}

iii. If the filter has been designed to remove a 2.5kHz tone from a speech waveform, discuss the impact of different levels of quantisation on system performance.

Justify your answers with explicit reference to properties of the magnitude responses of the filters.

[15 marks]

(b) Based on your experience of designing a similar filter for 4C1, and the magnitude responses shown here in Figure Q2:

i. What level of quantisation do you think would yield a useful filter for this case? Why?

ii. What interaction would you expect to see in terms of increased filter length versus using an increased number of bits in the coefficients? Explain.

[10 marks]

(Q2 continued overleaf.....)

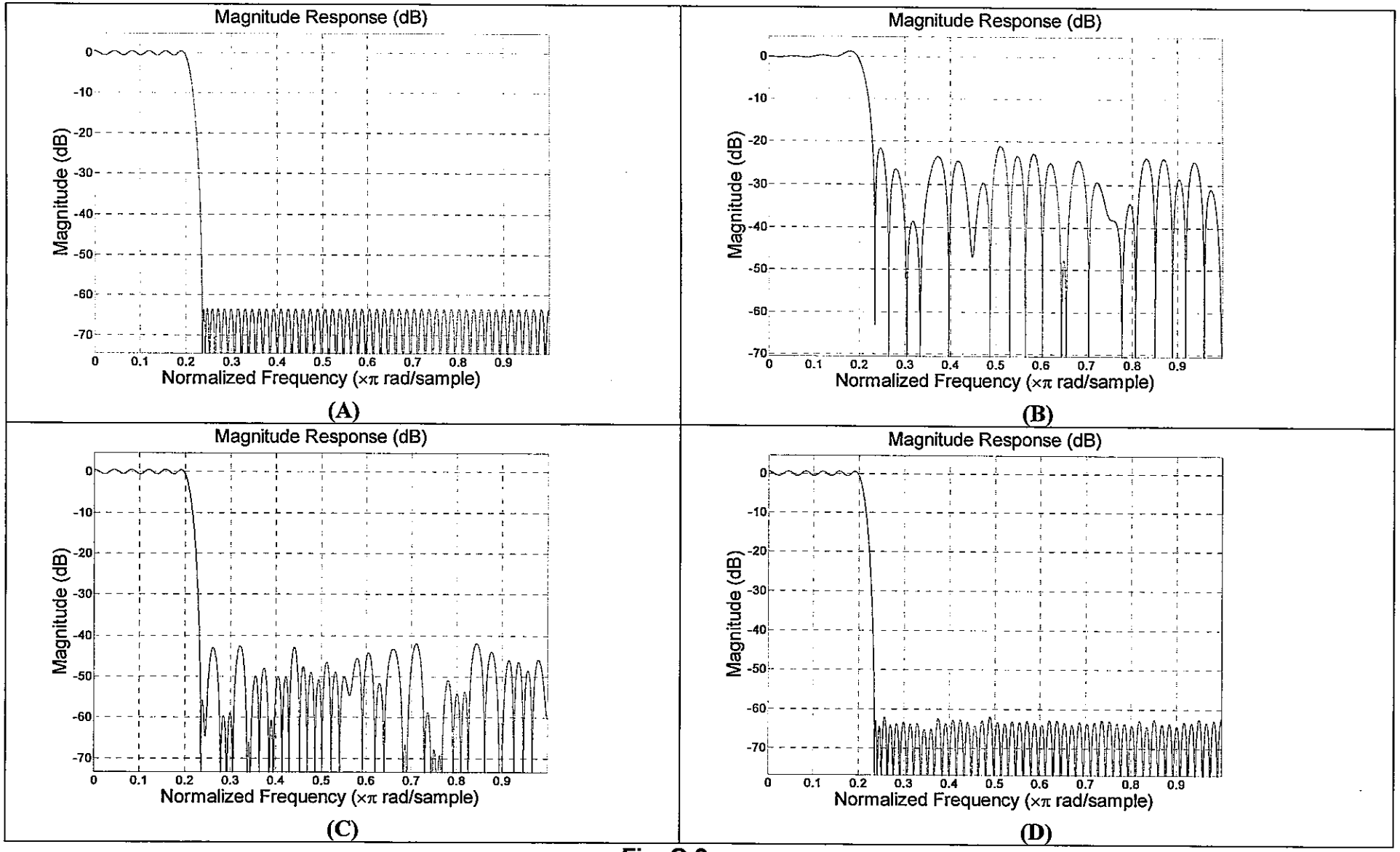
Magnitude Response (dB)
Magnitude (dB)
Normalized Frequency (×π rad/sample)
(A)
Magnitude Response (dB)
Magnitude (dB)
Normalized Frequency (×π rad/sample)
(B)
Magnitude Response (dB)
Magnitude (dB)
Normalized Frequency (×π rad/sample)
(C)
Magnitude Response (dB)
Magnitude (dB)
Normalized Frequency (×π rad/sample)
(D)

Fig. Q.2

Q.3

(a) Can the following algorithms exploit a distributed arithmetic approach:

i. Discrete Fourier Transform (DFT)?

ii. An adaptive FIR filter?

Explain your answer briefly with reference to the fundamental assumption underlying distributed arithmetic.

[9 marks]

(b) Compare memory requirements for the following 16X16 bit multiplier architectures on an FPGA:

i. Basic LUT multiplier

ii. Basic LUT multiplier using partial products

iii. LUT based multiplier using distributed arithmetic

Clearly show how you have calculated the memory requirements, using diagrams as appropriate to illustrate your answer.

[16 marks]

Q.4

(a) Using Figure Q4 as a reference, explain what is meant by the ***design gap*** in the IC Design industry, and how it has come about.

Explain how the design gap has been a driver for the IP Cores market.

[14 marks]

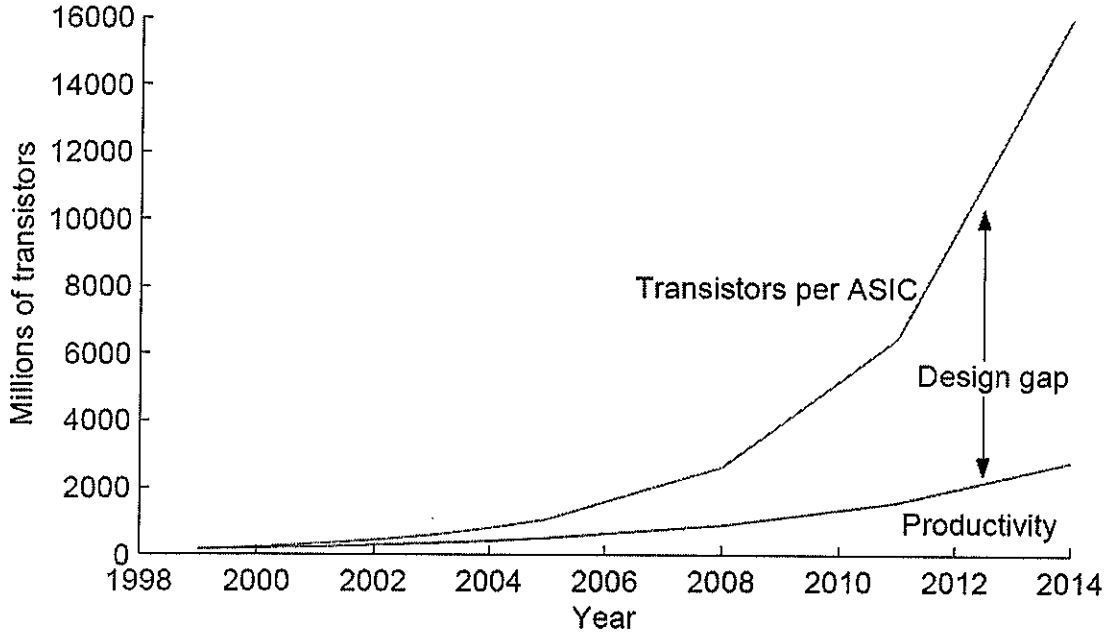

Figure Q4

(b) With reference to your assigned reading from 4C1, do you believe that IP Cooperation in the way ahead for IP Vendors?

Justify your answer briefly with reference to a specific example.

[11 marks]

Q.5

(a) Consider that the following initial block is used in a testbench to manage file output and testbench monitoring.

```
initial
begin
  // setup output file
  log_file=$fopen("eqlog.txt");
  if (!log_file)
    $display("Cannot open log file");
  console_file = 32'h0000_0001;
  out_file = log_file | console_file;

  // assume other testbench activity here

  // stop simulation
  $fclose(log_file);
  $stop;
end
```

Explain the difference in behaviour of the following two lines of code used later in the testbench. Assume that **value1** is an appropriately declared variable within the testbench.

```
$fmonitor(out_file, "%10d    %b", $time, value1);
$fmonitor(log_file, "%10d    %b", $time, value1);
```

[10 marks]

(b) The two major elements in a VGA controller circuit are the synchronisation circuit and the pixel generation circuit.

i. What is the role of the synchronisation circuit?

ii. Briefly describe how bit mapped, tile mapped and object mapped pixel generation circuits differ and comment on the memory requirements of each scheme.

Identify situations where you might use each of the pixel generation schemes if you were designing a simple video game. **[15 marks]**