Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
Ollscoil Átha Cliath | The University of Dublin

FACULTY OF ENGINEERING, MATHEMATICS & SCIENCE

SCHOOL OF ENGINEERING

Electronic & Electrical Engineering

Engineering **Hilary Term, 2016**

Senior Sophister

Annual Examinations

Integrated Systems Design

6th January 2016 **Exam Hall** **09.30 – 11.30**

Associate Professor Naomi Harte

Instructions to Candidates:

Answer FOUR questions in total.

Question 1 is COMPULSORY.

Answer any THREE of the remaining questions.

All questions carry equal marks

Materials permitted for this examination:

Calculator

Q.1 All elements carry equal marks in this question

(a) A 6-bit and a 4-bit number are multiplied. The LSB of both numbers is 2^{-2}. Assuming no sign bit in either number, what is the maximum bit width of the result?

(b) What is the advantage of distributed arithmetic for multipliers on FPGAs?

(c) Outline briefly the difference between distributed RAM and block RAM.

(d) What 3 functions are LUTs typically used to realise in FPGA based hardware?

(e) What is the primary difference between Verilog tasks **$monitor** and **$display** ?

(f) How does the quantisation of partial products from the MAC operation impact filter performance in a digital system?

(g) If memory is described as *volatile*, what does this mean?

(h) What is the purpose of non-blocking statements in a clocked **always** block for register updates?

(i) If flexibility is the major design constraint, which is more suitable: Soft IP or Hard IP? Explain briefly.

(j) What is the role of the synchronisation circuit in a VGA controller?

[25 marks]

Q.2

(a) Describe, with the aid of suitable diagrams the significant differences between a **Linear Phase FIR** filter and a **Transversal FIR filter**.

[10 marks]

(b) Let x_i represent a vector, of length *N*, of M-bit two's complement numbers where $|x_i| < 1$

Let a_i represent the elements of a vector of *N* constant coefficients.

$$y = \sum_{i=0}^{N-1} a_i x_i$$

Derive an expression for a distributed arithmetic version of y in the equation.

[15 marks]

Q.3

A filter is required to remove a 2kHz tone from a speech waveform with a sampling rate of 20kHz. As a systems designer, you made a decision to use a lowpass filter which filters out all frequencies just below and beyond the tone. The final filter will be implemented in hardware and must use finite precision. You need to maximise the quality of the speech with the minimum area requirement.

The plots in Figure Q3 (A), (B), (C) and (D) (overleaf) show the magnitude responses of four prototype FIR lowpass filters under evaluation. Filter (A) and (B) were designed using the least-squares method with a passband frequency up to 1900Hz and a stopband frequency of 2100Hz. Filter A was constrained to have 100 coefficients. Filter B was constrained to have 50 coefficients. The coefficients are not quantised in both cases. Filter (C) is a version of (A) with the coefficients quantised with an LSB of 2^{-7}. Filter (D) is a version of (B) with the coefficients quantised with an LSB of 2^{-15}.

(a) By inspecting the magnitude responses of these 4 filters, and considering your design constraint and the impact of quantisation on filter performance:
Which filter do you propose to use?
Justify your answers with explicit reference to properties of the magnitude responses of the filters.

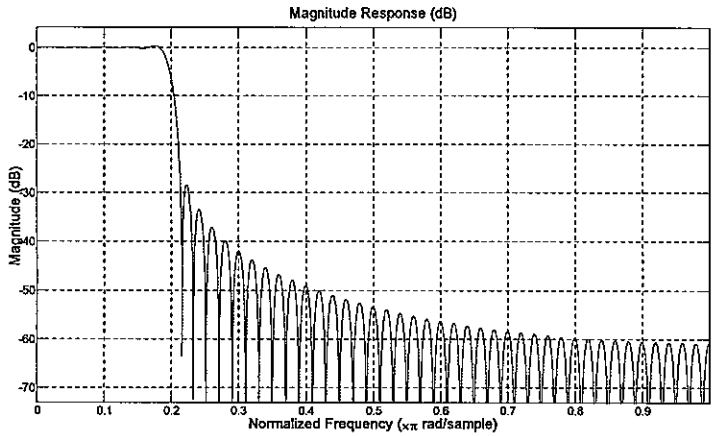
[20 marks]

(b) Based on your experience of designing a similar filter for 4C1, and the magnitude responses shown here in Figure Q3:

i. Will the filtered speech be of high quality if filtered with (A) or (B)? Explain, including reference to the properties of speech.

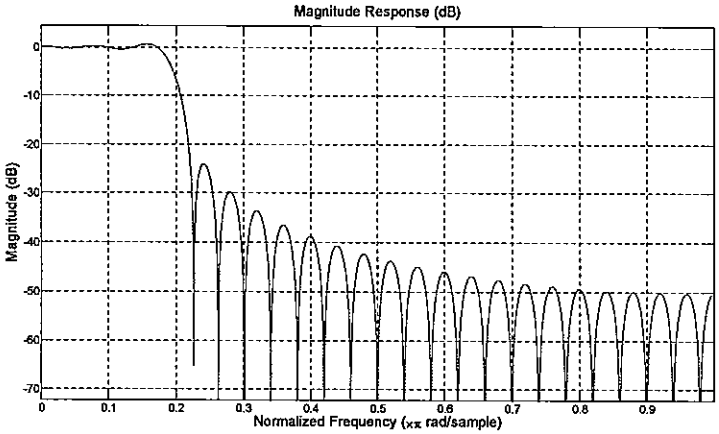
[5 marks]

(Q3 continued overleaf.....)



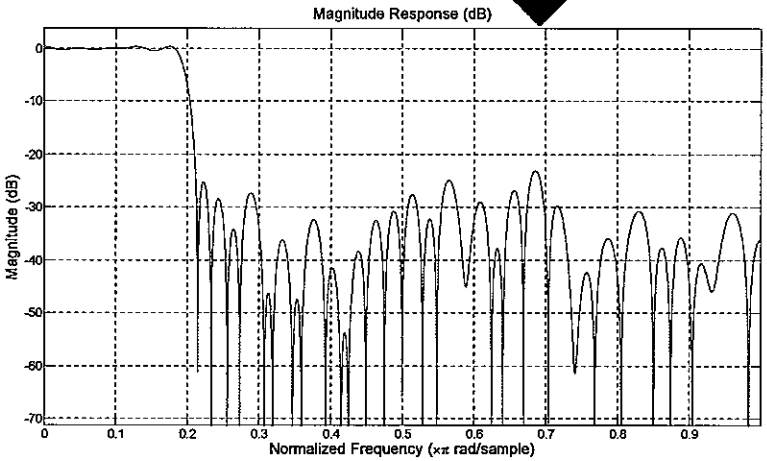
(A)

quantise

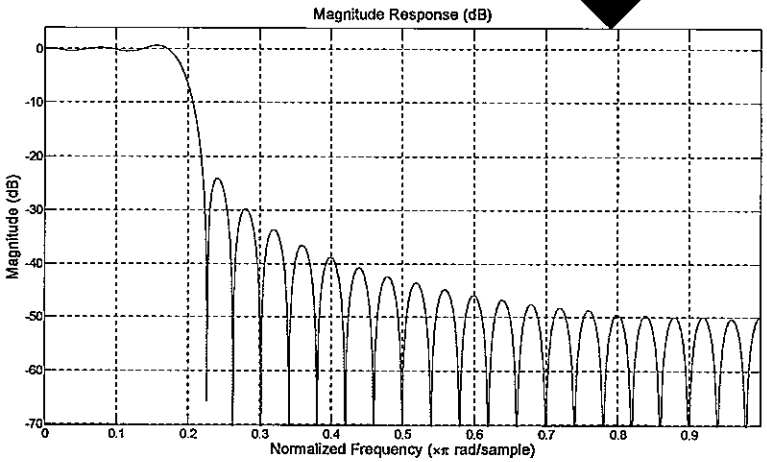


(B)

quantise



(C)



(D)

Fig. Q.3

Q.4

(a) Can the following algorithms exploit a distributed arithmetic approach:

i. Discrete Cosine Transform (DCT)?

ii. An adaptive FIR filter?

Explain your answer briefly with reference to the fundamental assumption underlying distributed arithmetic.

[10 marks]

(b) The diagram in Figure Q4 below shows a partial product implementation for the logic required to perform the multiplication of two 8-bit numbers, A and B.

Explain how the multiplier works, including how the bit-shift operations as shown achieve the desired outcome.

Calculate the memory requirements for this multiplier and compare to the use of a basic LUT multiplier for the same multiplication.

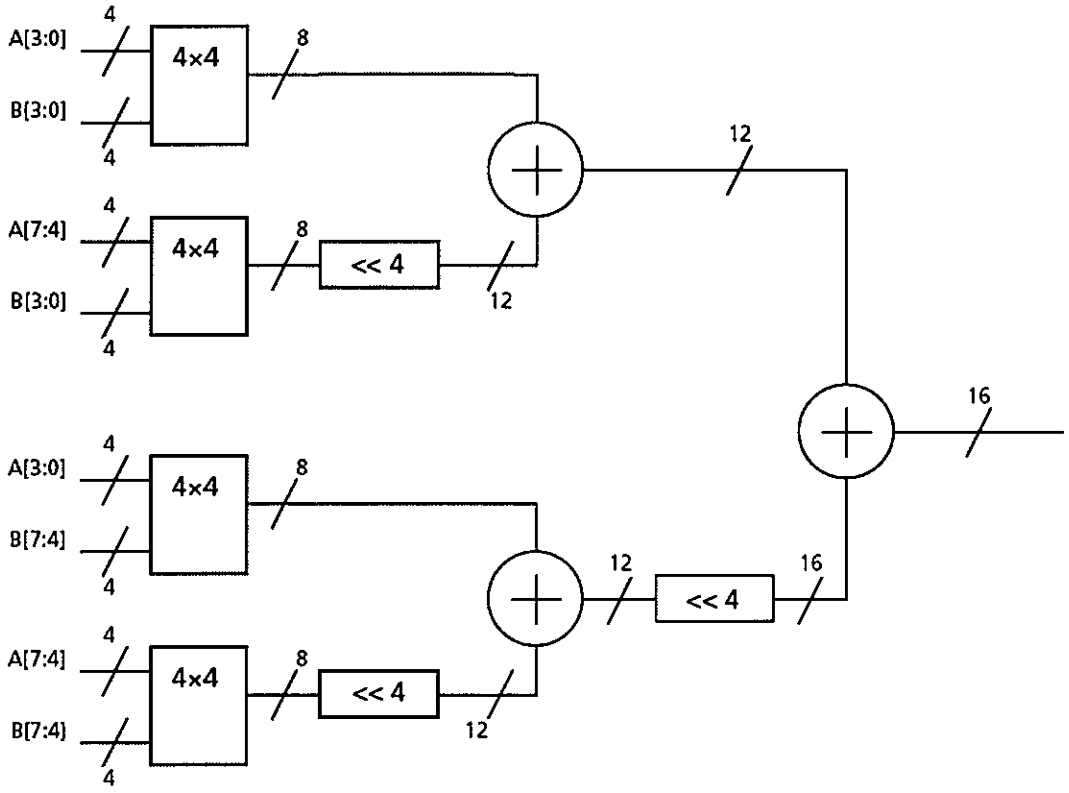


Fig. Q.4

[15 marks]

Q.5

(a) You have been asked to troubleshoot a hardware design. An engineer has tried to implement a design using the Xilinx design tools but no bit file was generated. The following report was given after synthesis:

Logic Utilization	Used	Available	Utilization
Registers	15,541	33,280	46%
LUTs	20,954	33,280	62%
Occupied Slices	13,171	16,640	79%
Multipliers	21	20	105%
BRAMs	15	20	75%

What is the problem with the engineer's design?

Suggest an approach to solve this problem.

This hardware passes all tests in behavioural simulations but does not build. Why does the behavioural simulation not find this error?

[NOTE: You are not required to write Verilog code for this circuit]

[10 marks]

(b) With reference to your assigned reading from 4C1, do you believe Moore's Law is dead?

Justify your answer with direct reference to trends in the semiconductor industry.

[15 marks]