UNIVERSITY OF DUBLIN

TRINITY COLLEGE

FACULTY OF ENGINEERING, MATHEMATICS & SCIENCE

SCHOOL OF ENGINEERING

Electronic & Electrical Engineering

Senior Sophister
Engineering
Annual Examinations

Trinity Term, 2014

INTEGRATED SYSTEMS DESIGN (4C1)

Date: 13th May 2014 **Venue: SPORTS CENTRE** **Time: 14.00 – 16.00**

Dr. Séamas McGettrick

Answer question ONE and ANY THREE of the remaining questions

All questions carry equal marks

Permitted Materials:

Calculator
Drawing Instruments

Q.1 All parts carry equal marks.

(a) What is meant by the term Saturation in the context of fixed point arithmetic?

(b) Calculate the result of the following multiplication between two twos complement fixed point binary numbers:
010.110 * 0.100

(c) What does the term non volatile memory mean? Is the memory on an FPGA non-volatile? Explain your answer.

(d) Name three ways Look-up Table resources can be used on an FPGA.

(e) There are two different types of slices on the Spartan 3 FPGA, slice M and sliceL. Why is this the case?

(f) What is an IP core?

(g) How does the ADC impact performance of filters in a digital system?

(h) What is contained in the annual ITRS report?

(i) Outline briefly the difference between distributed and block RAM

(j) List three advantages of automated testbenches.

[25 marks]

Q.2

(a) Describe, with the aid of suitable diagrams the difference between a **Linear Phase FIR filter** and a **Transversal FIR filter.**

Comment on how increasing quantisation of the coefficients of a FIR filter affects the filter's performance. Use suitable sketches to illustrate your answer.

[13 marks]

(b) The two major elements of a VGA controller are the synchronisation circuit and the pixel generation circuit.
What is the role of the synchronisation circuit?

Briefly describe how **bit mapped**, **tile mapped** and **object mapped** pixel generation circuits differ and comment on the memory requirements of each scheme.

Explain when you might use each of pixel generation schemes if you were designing a simple video game.

[12 marks]

Q.3

(a) What is Distributed arithmetic? To what kind of algorithms can it be applied? Identify one major advantage of Distributed Arithmetic on FPGAs

[5 marks]

(b) The hardware in Fig. Q3 shows a logical view of a distributed arithmetic Multiply Accumulate (MAC) unit.

Redraw the circuit in Fig Q3 replacing all unnecessary hardware with a single ROM.
Calculate the contents of the ROM in terms of K_0,K_1, K_2 and K_3.

[10 marks]

(c) Explain, with the aid of a diagram what is meant by Basic LUT multiplier using partial products.
Calculate the memory requirements of a 16x16 Basic LUT multiplier and compare it to that of a Basic LUT multiplier with partial products.

Highlight one disadvantage of the Basic LUT multiplier using partial products when compared with the Basic LUT multiplier.

[10 marks]

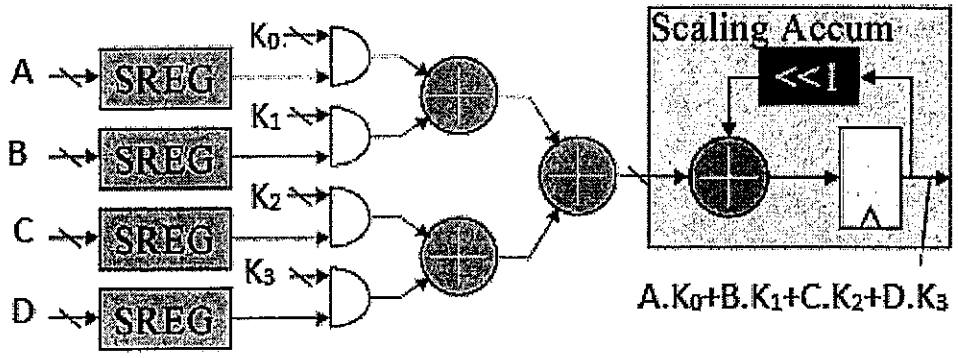

Fig. Q.3

Q.4

(a) You have been asked to troubleshoot a hardware design shown in Fig. Q4. The engineer has tried to implement the design using the Xilinx design tools with a target clock speed of 100 MHz. A bit file was generated but the design does not work correctly on the board. The engineer used IP cores for the memory and multipliers. The IP cores have registered outputs and are fully pipelined.

The following report was given after place and route:

Logic Type	Used	Available	Utilization
Registers	15,541	33,280	46%
LUT	32,280	33,280	97%
Occupied Slices	16,640	16,640	100%
Multipliers	0	20	0%
BRAMS	0	20	0%
Max achievable clock rate: 90 MHz			

i. This hardware passes all tests in behavioural simulations and builds with warnings but without errors. What is the problem with the engineer's design?
ii. Suggest an approach to fix this problem.
iii. Why do the ISE tools not fail to implement on this type of error?

[12 marks]

(b) Define what is meant by **latency** and **throughput** in the context of hardware design.

[5 marks]

(c) Describe with aid of diagrams what is meant by **pipelining a circuit** in the context of hardware design.
How does pipelining a design affect the latency and throughput of the circuit?

[8 marks]

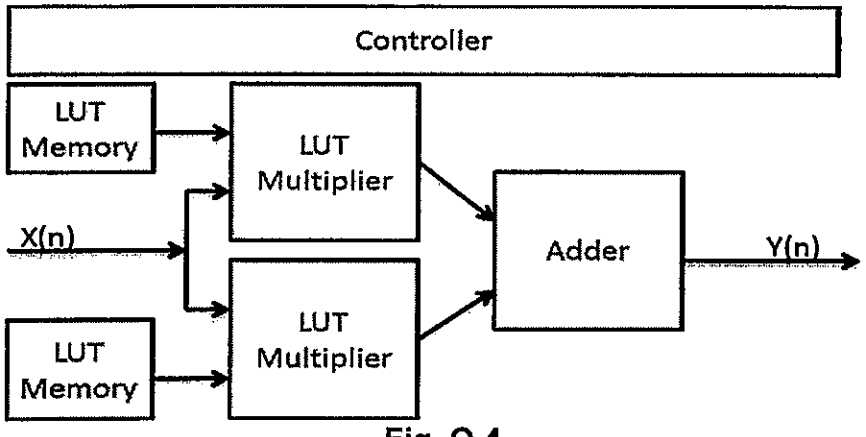

Fig. Q.4

Q.5

(a) The response of a particular Infinite Impulse Response (IIR) filter is given by:

$$y(n) = \sum_{i=0}^{3} b_i x(n-i) - \sum_{j=1}^{3} a_j x(n-j)$$

Sketch a circuit that can implement this equation using the following components:

- 5 Multipliers
- 4 Adders
- 4 Registers

Assuming that the adder and the multiplier components have a delay of 3ns and that the wires have a negligible delay, what is the minimum clock period that you could use with this design?

[12 marks]

(b) List **five** design considerations/tradeoffs a system designer might take into account when designing an integrated system.

Explain how these considerations might affect the designer's choice to use Intellectual Property (IP) cores and the type of IP cores used in the system.

[13 marks]