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EE5M01-1

FACULTY OF SCIENCE, TECHNOLOGY, ENGINEERING AND MATHEMATICS

SCHOOL OF ENGINEERING

Electronic and Electrical Engineering

Engineering **Semester 1, 2022**

MAI/MSc

Integrated Systems Design

14/12/2022 **RDS-SIMMONSCOURT** **14:00–16:00**

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Instructions to candidates:

Answer all questions.

Acronyms used in this paper:

ASIC	Application Specific Integrated Circuits
FPGA	Field Programmable Gate Arrays
FSM	Finite State Machine
LUT	Look-Up Table
IP	Intellectual Property

All symbols have usual meanings

Q.1 **[Total: 25 marks]**

(a) In each of the following scenarios, state whether the value assigned to d is **signed** or **unsigned**. Give reason(s) for your answer. Also determine the BINARY value of d.

```
reg signed [2:0] a;
reg        [2:0] b;
reg signed [3:0] c;
reg signed [5:0] d;

assign a = 3'd3;
assign b = 3'd4;
assign c = -4'sd1;
```

i) d = a + c;

ii) d = $signed(b) + c[0];

iii) d = $signed(b) * a;

[9 marks]

(b) A verification engineer is designing a testbench for Verilog code. They wish to enable a counter for N clock cycles before disabling the counter again.

Write a Verilog task that will take N as a variable input, set an enable signal high, wait N clock cycles and then set an enable signal low after the falling edge of the clock. You may assume that both clk and cnt_enable are variables declared outside the task but available inside the scope of the task.

[10 marks]

(c) Referring back to part b, explain why we use a **task** and not a **function** in this circumstance. **[2 marks]**

(d) The verification engineer now wishes to edit the test to make it self-checking. Give two reasons for doing this. **[4 marks]**

Q.2 **[Total: 25 marks]**

A controller processes sensor data and requires the detection of 5 consecutive 0s or 1s pattern on a serial input. This is to be controlled by a Finite State Machine. You are given the following information:

i) Your FSM has 3 inputs:

   (a) **clk:** clock signal.

   (b) **reset:** active-high, synchronous reset signal.

   (c) **serial_in:** 1-bit serial data which is considered valid at every clock cycle.

ii) Your FSM has 1 output:

   (a) **data_out[1:0]:** 2-bit signal indicates that the sequence has been detected. This should stay high until the next clock cycle.

iii) The outputs should behave as follows:

   (a) In the event of a sequence of four consecutive 1's your state machine should output 10.

   (b) In the event of a sequence of four consecutive 0's the state machine should output 01.

   (c) At all other times the output should be 00.

iv) Valid sequences may overlap.

(a) Provide a state diagram that defines the state transition logic and outputs. **[10 marks]**

(b) Define a test plan for your design, giving a brief outline of each testcase that you would use to verify your design. **[10 marks]**

(c) Provide a brief justification of your design choices (e.g. number of states/ bits used to represent them, type of state machine). **[5 marks]**

Q.3 **[Total: 25 marks]**

(a) A digital filter design for a specific application has the following impulse response:

$$y(n) = ax(n) + bx(n-2) + cx(n-3)$$

i) Explain, with the help of diagrams, a simple and pipelined implementation of the filter.

ii) Determine the maximum operating frequency of the simple and pipelined models. Given: An adder incurs 10 ps of delay and a multipler incurs 25 ps of delay.

iii) Determine the latency and throughput of the simple and pipelined models, assuming the same delays as above. Comment on the latency and throughput results.

iv) Provide an expression for output y_{pp} the output of the pipelined system.

[18 marks]

(b) After an optimisation, the coefficients of the digital filter are found to be as follows:

$$a = 16, b = 32, c = 2$$

Explain how you would implement this filter and comment on the hardware costs/energy benefits of this approach. **[7 marks]**

Q.4 **[Total: 25 marks]**

(a) A high definition image processing pipeline uses AXI streaming interface between its camera system and the image processing IP. The camera interface can transmit 2 pixels (at 30-bits of image data per pixel) every cycle. The image processing IP can receive 2 pixels at each cycle but can only process one pixel per cycle. Draw a waveform diagram representing an AXI stream transaction of 6 pixels between the camera interface and the image processing IP. **[8 marks]**

(b) With reference to synchronous designs, explain Metastability and its importance in timing analysis. **[5 marks]**

(c) With the help of a diagram, explain a circuit that could help to deal with metastability in signals that cross clock domains in a design. **[6 marks]**

(d) Brielfy describe the memory architecture in a modern FPGA. Explain the rationale for choosing one over the other in a design, and its potential impact on performance. **[6 marks]**