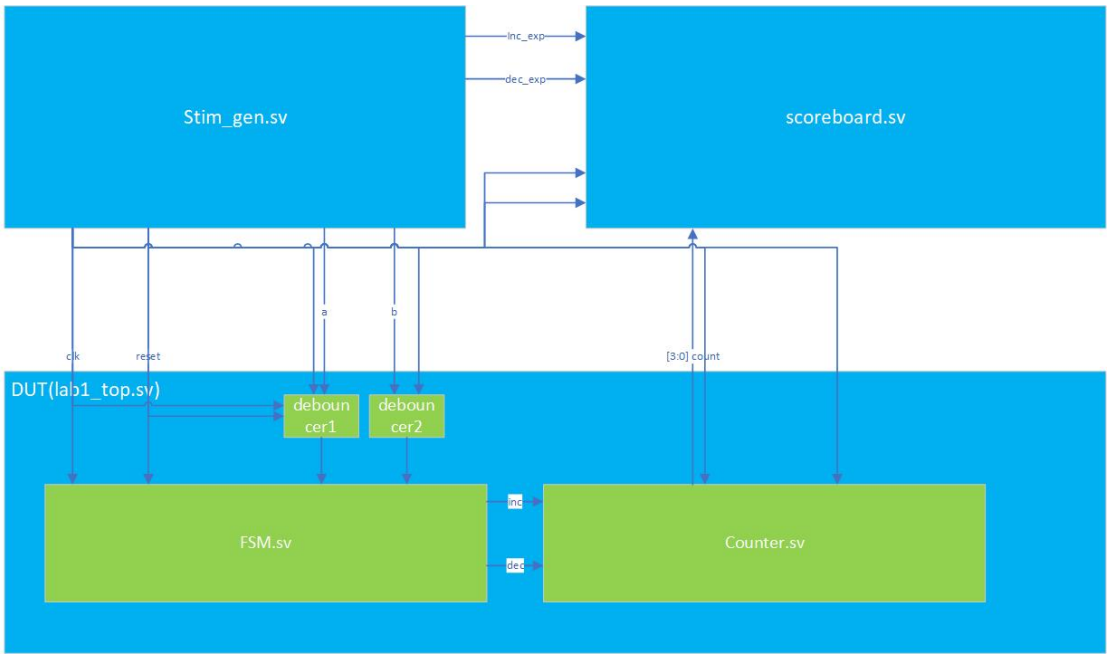
1. Descriptions of the roles of your testbench blocks



1.1 Stim_gen.sv

The module is used to generate the global clock signal and reset signal, and according to the requirements of the test sequence, the corresponding test signal is generated in time order for DUT to process, and the expected result is passed to scoreboard for evaluation. When inc_exp or dec_exp is 1, it means that the total number of expected test results is increased or decreased by one. When inc_exp and dec_exp are both 1, it means that the total number of expected test results is unchanged.

1.2 scoreboard.sv

The module is used to detect whether the result processed by the DUT (the total number of vehicles in the parking lot goes up or down) is consistent with the expected result provided by the incentive, and the judgment result is printed and recorded in a log file.

1.3 DUT

The module connects the finite state machine, the counter and the buffeting device, receives the sensor signal after buffeting, makes judgment, counts and outputs the total number of vehicles in the parking lot.

2. Details of all tested scenarios and their expected results

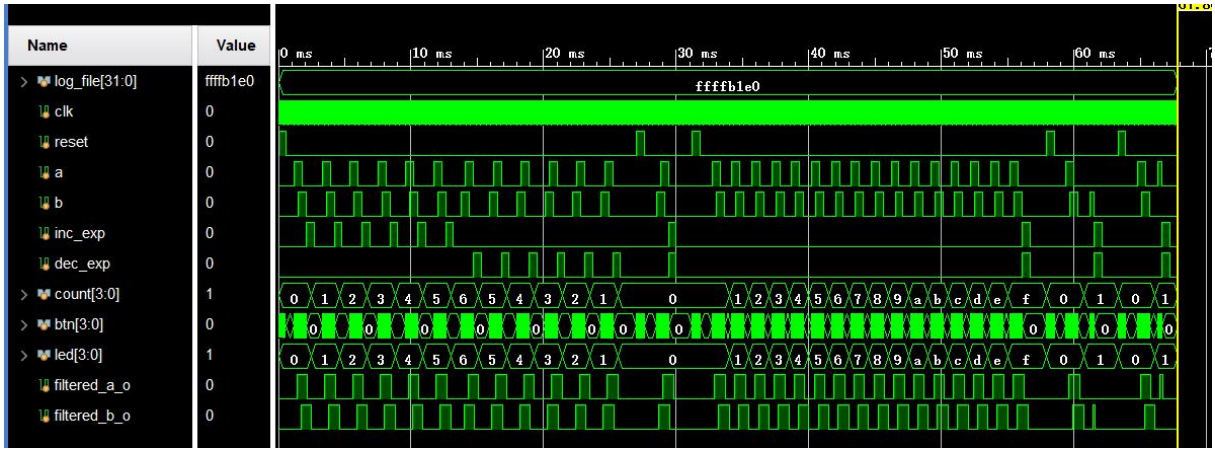
No	Type	Scene	Expected Output
1	Forward	Six cars enter the park normally and sensor a and b are activated orderly	Total number of the car in park increase by 1
2	Forward	Six cars leave the park normally and sensor a and b are activated orderly	Total number of the car in park increase by 1
3	Backward	The car enter the park, but reach the max of the counter(15)	Total number should hold
4	Backward	The car exit the park, but reach the min of the counter(0)	Total number should hold
5	Backward	The car enter the park, but it did not finish the operation	Total number should hold
6	Backward	The car exit the park, but it did not finish the operation	Total number should hold

3. Document the bugs found (intentionally or unintentionally introduced). Show how the testbench caught them

When the sensor signal is too short to meet the conditions for the establishment of buffeting, the process cannot be recorded and recognized.
When the test bench fed a short sensor signal and expected the count to change, the count did not change.

4. Include screen captures of timing diagrams demonstrating test runs and their results, as well as log files produced by the testbench

Timing_diagrams:



Log_file:

score_board_log.txt

```
*******The Test begin*******
inc_exp   dec_exp   hold_exp  inc     dec     hold    pass
begin the forward test
begin the enter test
1         0         0         1       0       0       1
1         0         0         1       0       0       1
1         0         0         1       0       0       1
1         0         0         1       0       0       1
1         0         0         1       0       0       1
1         0         0         1       0       0       1
begin the exit test
0         1         0         0       1       0       1
0         1         0         0       1       0       1
0         1         0         0       1       0       1
0         1         0         0       1       0       1
0         1         0         0       1       0       1
0         1         0         0       1       0       1
begin the backward test
begin the reach_low test
0         0         1         0       0       1       1
begin the reach_max test
0         0         1         0       0       1       1
begin the exit_fail test
0         0         1         0       0       1       1
begin the enter_fail test
0         0         1         0       0       1       1
*******The Test is done*******
```