FACULTY OF ENGINEERING, MATHEMATICS & SCIENCE

SCHOOL OF ENGINEERING

Electronic & Electrical Engineering

Engineering **Trinity Term, 2020**

Senior Sophister

Annual Examinations

INTEGRATED SYSTEMS DESIGN (EEU44C01-1)

6/05/2020 **ONLINE** **12.00 – 16.00**

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Instructions to Candidates:

Answer FOUR questions in total.

Question 1 is COMPULSORY.

Answer any THREE of the remaining questions.

All questions carry equal marks.

Materials Permitted for this Examination:

Calculator

Drawing Instruments

Non-programmable calculators are permitted for this examination. Please indicate the make and model of your calculator on each answer book used.

Q.1

(a) Convert -0.1220703125 to a two's complement 8-bit fixed point representation, highlighting any rounding or truncation used.

(b) An 8-bit and a 10-bit number are added. Assuming no sign bit in either number, how many bits should be used to store the result?

(c) Comment on two differences between Verilog system tasks $monitor and $display.

(d) What problem does truncation cause in a two's complement system specifically?

(e) What potential synthesis issue can you see with the following piece of code:

```
always @ (*) begin
    if (sel == 1'b1) begin
        f = a;
    end
end
```

(f) Why is linear phase an important property of symmetric FIR filters?

(g) If design confidence is the major concern, which is more suitable: Soft IP or Hard IP? Explain briefly.

(h) State the impact of pipelining on system throughput and system latency

(i) If a designer wishes to parallelise a system by N, i.e. to process N consecutive input samples simultaneously, what condition must F_{clk} satisfy with respect to F_{samp}?

(j) What is the role of a synchronisation circuit in a VGA display?

[25 Marks]

Q.2

(a) The plots in **Fig Q.2** A, B, C and D (overleaf) show the magnitude responses of four FIR lowpass filters. One of the filters is not quantised. This filter was designed with a sampling rate of 16 kHz, with passband and stopband frequencies of 2000 Hz and 2350 Hz respectively. The original 120 filter coefficients are quantised to obtain the remaining three filters.

By inspecting the magnitude responses:

i. Identify which of the filters is not quantised.

ii. Of the remaining filters, match the filters to the following levels of quantisation in terms of LSB size: $2^{-16}, 2^{-10}, 2^{-6}$.

iii. Comment on the impact the level of quantisation has on stopband attenuation, passband ripple and transition band width.

Justify your answers with explicit references to the magnitude responses of the filters.

[10 Marks]

(b) A simple 3 tap filter is assumed to have the following impulse response:

$$y(n) = ax(n) + bx(n-1) + cx(n-2)$$

i. Draw a simple diagram of this system.

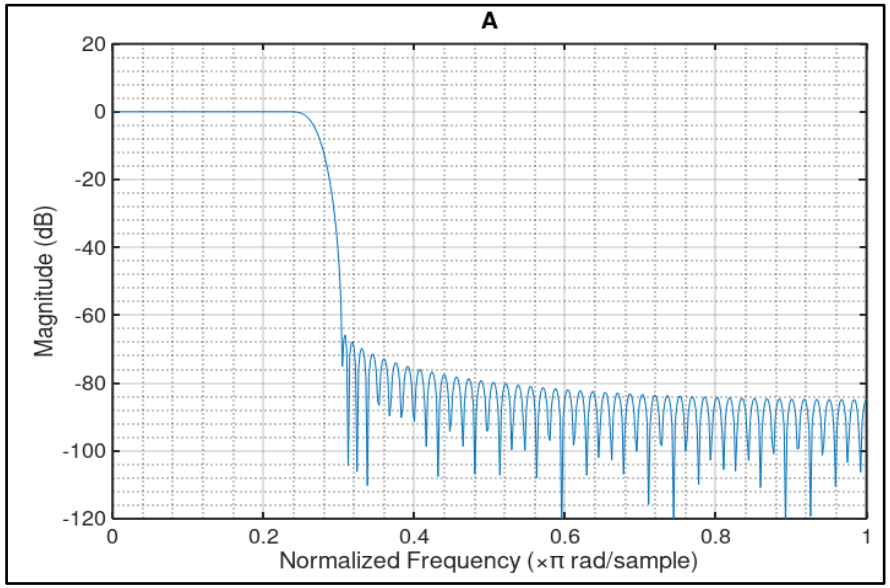
ii. Compute a limit on the F_{clk} of the system, using T_A and T_M to denote the delay through an adder and a multiplier respectively.

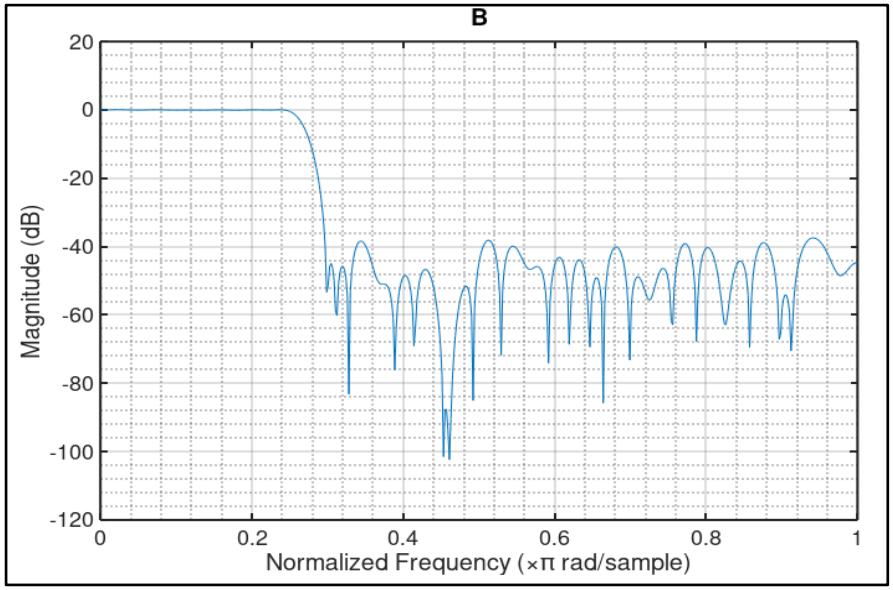
iii. Draw an additional diagram to demonstrate how pipelining could effect $F_{clk,}$

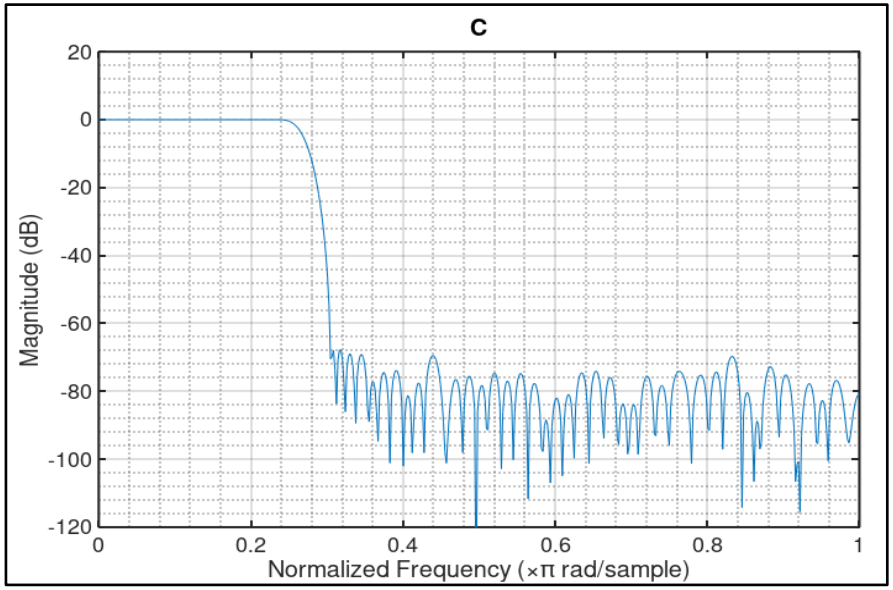
iv. Provide an expression for output y_{pp} the output of the pipelined system.

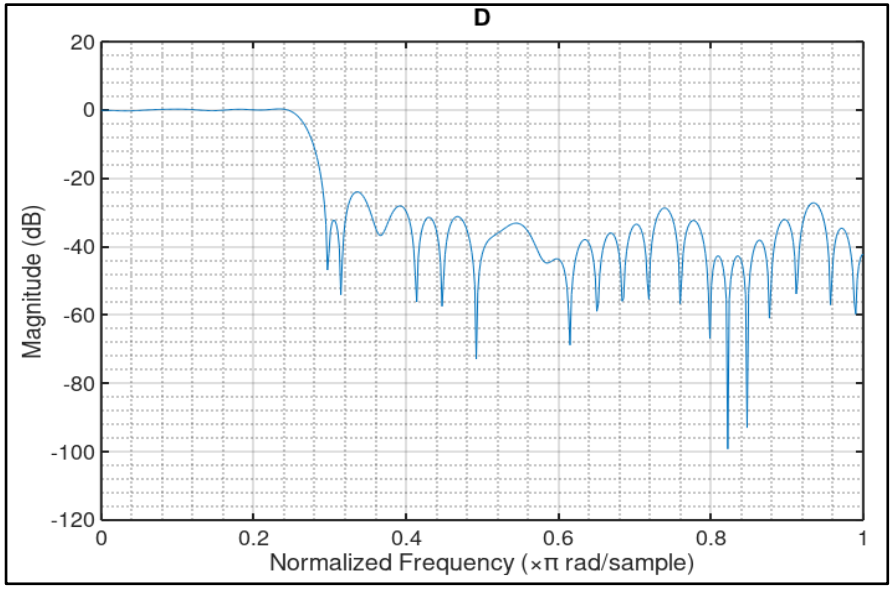
v. Provide an expression for the limit on F_{clk} when pipelining is employed in the system

[15 Marks]









Q.3

(a) In each of the following scenarios, state whether value assigned to c is signed or unsigned and give a reason for your answer.

```
reg         [2:0] a;
reg signed  [1:0] b;
reg signed  [3:0] c;
a = 3'd2;
b = -2'd1;
```

i) `c = a + b;`

ii) `c = 3'd2 + b;`

iii) `c = $signed(a) + b;`

[9 Marks]

(b) A verification engineer is designing a testbench for Verilog code. They wish to enable a counter for N clock cycles before disabling the counter again.

i) Write a Verilog task that will take N as a variable input, set an enable signal high, wait N clock cycles and then set an enable signal low.

[9 Marks]

ii) Explain why we use task and not a function in this circumstance.

[3 Marks]

iii) The verification engineer now wishes to edit the test to make it self checking. Give two reasons for doing this.

[4 Marks]

Q.4

(a) A digital design on an FPGA requiring volatile memory resources may use **block RAM** or **distributed RAM**.

i) Describe the differences between block RAM and distributed RAM

ii) Define the term volatile.

iii) Explain when a system designer might choose to use a block RAM or distributed RAM.

[9 Marks]

(b) Draw a basic diagram of a **DSP slice** from an FPGA.

[6 Marks]

(c) Describe how DSP slices may be used to implement a complex multiplier and draw a simplified diagram to demonstrate your answer.

[10 Marks]

Q.5

(a) What are IP Cores in the context of hardware design? Why are they useful?
What is the difference between Hard IP and Soft IP cores?
Give an example of each IP type.

[10 marks]

(b)

*"Because of the breakdown of **Dennard scaling**… The **power wall** forces designers to ensure that, at any point in time, large fractions of their chips are effectively '**dark silicon**' "*

i) Explain the terms "Dennard Scaling", "Power Wall" and "Dark Silicon".

ii) With reference to the power wall and dark silicon, explain why modern IC designs are increasingly using additional resources (increasing area) to allow lower power operation.

[15 marks]