UNIVERSITY OF DUBLIN

TRINITY COLLEGE

FACULTY OF ENGINEERING, MATHEMATICS & SCIENCE

SCHOOL OF ENGINEERING

Electronic & Electrical Engineering

Senior Sophister
Engineering
Annual Examinations

Trinity Term, 2013

INTEGRATED SYSTEMS DESIGN (4C1)

Date: 8th May 2013 **Venue: Gold Hall(220)** **Time: 9.30 – 11.30**

Dr. Séamas McGettrick

Answer question ONE and ANY THREE of the remaining four questions.

All questions carry equal marks.

Permitted Materials:

Calculator
Drawing Instruments

Q.1 All parts carry equal marks

(a) How do you decide if a signal should be declared as a **wire** or a **reg** type in Verilog?

(b) Convert 9.65845 to a 10-bit fixed-point representation where the radix point occurs after the 5^{th} digit.

(c) Convert -9.65845 to a 10-bit fixed-point representation where the radix point occurs after the 5^{th} digit. What scheme for representing negative numbers did you use? Why did you choose this one?

(d) What is the role of the synchronisation circuit in a VGA controller?

(e) In basic testbenches we manually set the test values and monitor the output waveform to see if the circuit is working. Briefly describe two disadvantages of this type of testbench.

(f) There are two different types of slices in the Spartan 3 FPGA Configurable Logic Blocks, sliceM and sliceL. What is the difference between these two slices?

(g) In the context of FPGAs, what is a Block RAM?

(h) Briefly describe what is meant by blocking assignment statements in Verilog. Where would they be used?

(i) In the context of a VGA display what is the difference between a bit-mapped and a tile-mapped screen?

(j) How does the Analogue to Digital Converter impact the performance of filters in a digital system?

[25 marks]

Q.2

(a) Describe, with the aid of suitable diagrams the differences between a **Linear Phase FIR** filter and a **Transversal FIR filter**.

[13 marks]

(b) You have been asked to design a FIR filter in hardware with the following characteristics:

Number of Coefficients:	52
Coefficient bit width:	16 bits.
Data bit width:	16 bits.

Briefly comment on the sources and effects of arithmetic errors in this system.

Explain with the aid of a diagram how you might expect the performance of this Finite Precision FIR filter to compare with that of a full precision FIR filter, e.g. FIR filter implemented in Matlab.

[12 marks]

Q.3

(a) What is Distributed Arithmetic and when can it be used?

Name one major advantage of Distributed Arithmetic on FPGAs.

[5 marks]

(b) Let x_k be a vector of N-bit two's complement numbers where $|x_k|<1$

Let A_k be a vector of Constant Coefficients.

$$y = \sum_{k=1}^{K} A_k \, x_k$$

Derive an expression for a distributed arithmetic version of y in the equation.

[10 marks]

(c) Sketch a diagram of a bit serial hardware architecture that could implement the equation from (b) above. For this diagram you can assume K = 4.

Explain, with reference to your diagram, how the multiply-add hardware can be replaced by a ROM.

[10 marks]

Q.4

(a) You have been asked to troubleshoot a hardware design. The engineer has tried to implement the design using the Xilinx design tools but no bit file was generated. The following report was given after synthesis:

Logic Utilization	Used	Available	Utilization
Registers	15,541	33,280	46%
LUTs	20,954	33,280	62%
Occupied Slices	13,171	16,640	79%
Multipliers	21	20	105%
BRAMs	15	20	75%

What is the problem with the engineer's design?

Suggest an approach to solve this problem.

This hardware passes all tests in behavioural simulations but does not build. Why does the behavioural simulation not find this error?

NOTE: There is no need to write Verilog code for this circuit

[7 marks]

(b) Define what is meant by the terms **latency** and **throughput** in the context of hardware design.

[6 marks]

(c) Why are timing constraints used in FPGA design? Describe, with the aid of diagrams, how pipelining can be used to meet the timing constraints of a circuit?

How does pipelining a design affect the latency and throughput of the circuit?

[12 marks]

Q.5

(a) What are IP cores in the context of hardware design?

Discuss the type of test and verification strategies that are required for Hard IP, Firm IP and Soft IP cores.

[12 marks]

(b) With reference to Figure Q5 and the ITRS report explain the importance of IP cores in the future of hardware design.

[13 marks]

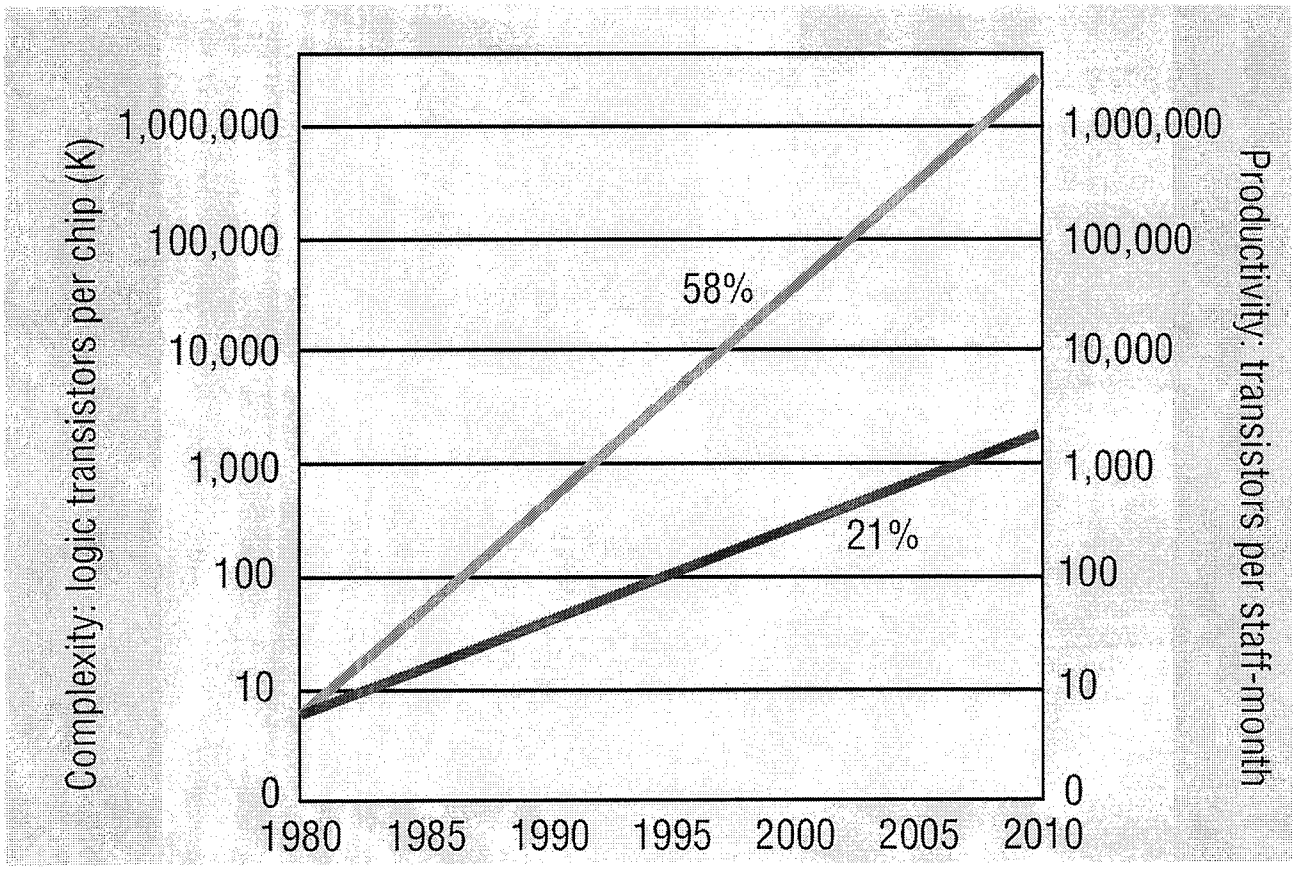

Figure Q5