Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
Ollscoil Átha Cliath | The University of Dublin

FACULTY OF SCIENCE, TECHNOLOGY, ENGINEERING AND MATHEMATICS

SCHOOL OF ENGINEERING

Electronic and Electrical Engineering

Engineering **Semester 2, 2021**
Senior Freshman

Integrated Systems Design

11/05/2021 **Online** **12:00–14:00**

Rhona Wade

Instructions to Candidates:

Answer FOUR questions in total.

ALL questions are COMPULSORY.

All questions carry equal marks.

Materials permitted for this examination:

This is an open book examination.

Q.1 **[Total: 25 marks]**

(a) A direct-form implementation of a 5-tap FIR filter is shown in Figure 1:

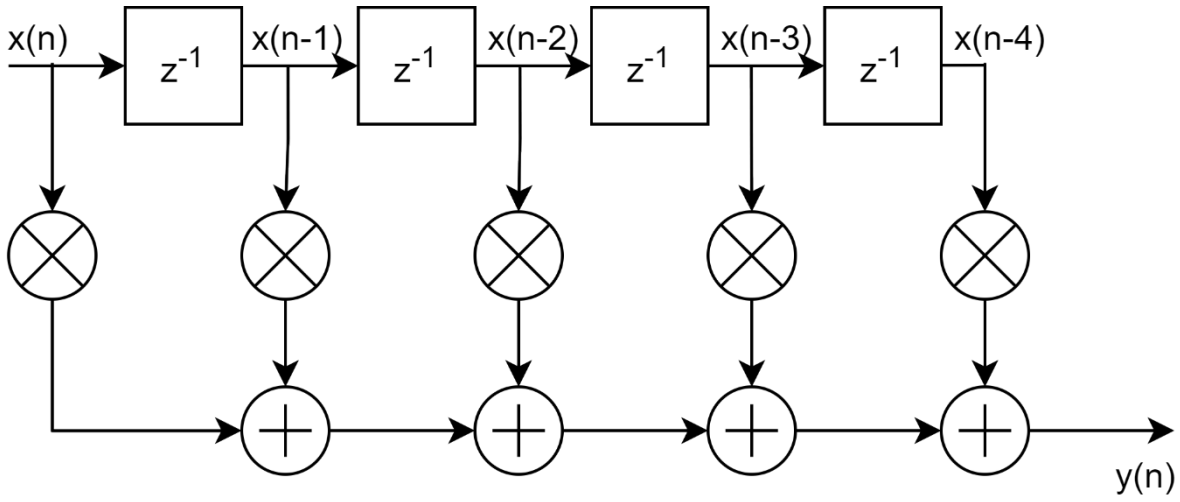

Figure 1. Direct-form implementation of an FIR filter with 5 taps

i. Compute a limit on F_{clk} for this system, using T_A and T_M to denote the delay through an adder and a multiplier respectively. You may assume that x(n) is a register output and y(n) is a register input.
ii. Draw an additional diagram illustrating where pipeline registers should be placed to maximise F_{clk}, while increasing latency by only one clock cycle. You may assume that $T_M > 2T_A$.
iii. Provide an expression for the new maximum F_{clk} of this pipelined system.

[19 marks]

(b) To implement an FIR filter in hardware, the filter tap values must be quantized. Describe what impact this has on the performance of the filter, with reference to passband ripple, transition bandwidth and stopband attenuation.

[6 marks]

Q.2 **[Total: 25 marks]**

(a) A set of traffic lights at a pedestrian crossing is to be controlled by a Finite State Machine. You are required to provide the following:

- A state diagram to define the state transition logic and any Mealy outputs,
- A brief description of each state's behaviour; Moore outputs, any flags used etc.,
- A brief justification of design choices (e.g. count_max values chosen per state).

You have the following information:

i. You have access to an external counter with a variable maximum. It will stop counting when it reaches the value set by *count_max* and assert *count_done*. It will continue counting from zero when *count_reset* is asserted for one clock cycle.

ii. Your FSM has four inputs:
   a. *clk*: clock signal
   b. *reset*: synchronous reset signal
   c. *ped_btn*: 1-bit signal that will be high for one clock cycle if a pedestrian has pushed the button at the crossing
   d. *count_done*: 1-bit signal from an external counter that will be high when the counter has reached its max value (set by FSM output *count_max*)

iii. Your FSM must provide four outputs:
   a. *car_gar*: 3-bit 1-hot signal to control the traffic light facing cars (MSB controls green light, LSB controls red light)
   b. *ped_gar*: 3-bit 1-hot signal to control the traffic light facing pedestrians (MSB controls green light, LSB controls red light)
   c. *count_max*: 10-bit signal to set the value the counter will stop at
   d. *count_reset*: 1-bit signal to reset the counter value to zero

iv. The sequence for both the car's traffic lights and the pedestrian's traffic lights should be GREEN-AMBER-RED.

v. If the car's traffic lights have only just gone green, then the pedestrians should wait longer for their light to go green

vi. You may assume that when your system is implemented on a real device, 1024 clock cycles will be mapped to a duration of 32 seconds.

Q.3 **[Total: 25 marks]**

(a) Draw a basic diagram of a DSP slice from an FPGA and describe its key features.

[6 marks]

(b) Explain why multiplying by a fixed coefficient in an ASIC design is cheaper and lower power than a completely variable multiplication.

[3 marks]

(c) Provide two reasons why the Vivado synthesis & implementation flow may infer a DSP slice for a low complexity, fixed multiplication.

[6 marks]

(d) Draw a waveform diagram representing an AXI stream transaction for an AXI manager transmitting three 6-bit words. Assume the AXI subordinate can capture two words at a time, but takes two clock cycles to process the data after it is captured.

[10 marks]

Q.4 **[Total: 25 marks]**

(a) In each of the following scenarios, state whether the value assigned to d is signed or unsigned and give a reason for your answer.

```
reg        [2:0] a;
reg signed [2:0] b;
reg signed [1:0] c;
reg signed [3:0] d;

assign a = 3'd2;
assign b = 3'd2;
assign c = -2d'1;
```

i) `d = a + c;`

ii) `d = b[1:0] + c;`

iii) `d = $signed(a) + b;`

[9 marks]

(b) A verification engineer is designing a testbench for Verilog code. They wish to create a 1-bit stimulus signal "*div2*" that will invert its value on each clock cycle for N clock cycles (see waveform in Figure 2.)

i) Write a Verilog task that will take N as a variable input, initialise a 1-bit signal div2 at zero, then invert its value on every clock cycle for N clock cycles.

[10 marks]

ii) Explain why we use a task and not a function in this circumstance.

[2 marks]

iii) The verification engineer now wishes to edit the test to make it self-checking. Give two reasons for doing this.

[4 marks]