# Integrated Systems Design

Course Overview, Semester 1 22/23

# Introduction

## Dr. Libin K Mathew

- Over 4 years of Experience in Research and Development.
- Started career at Panasonic R&D Center Singapore
- Then works as a Scientist at A*STAR Singapore as Scientst.
- Questions are encouraged.
- Currently working as Teaching Fellow, Trinity College Dublin

# Course Overview

- ISD (4C1, 5M01) builds on digital design fundamentals from 3C7
- Digital design module is a pre-requisite
  - Revise course material if rusty!
- ISD takes a systems perspective
  - Top level specification with focus on design choices
  - Anticipate impact of decisions on overall design performance verses cost.
- Learning outcomes:
  - Understand and develop system specifications
  - Implement designs using Verilog HDL on Basys3 Boards
  - Develop automated testbenches
  - Assess system cost and performance

# Course Content

1. Overview of Digital Design principles and Verilog Language
2. Advanced Testbench Design
3. Digital Arithmetic: Signed numbers and Finite Precision Effects
4. FIR Filter: Design and Implementation
5. Digital System Interfaces
6. Digital Performance: Synthesis, Power and Timing
7. FPGA Resources
8. Industry Review

# Assessment

- 5 ECTS course: ~150 hours student effort
- 30%: Continuous Assessment
  - 3 graded lab assignments
- 70%: End of Semester Exam
  - Focus will be on demonstrating understanding of topics covered, not repetition of information

# Lectures

- Notes uploaded to Blackboard prior to lectures
- Skeleton notes only
  - Additional detail and examples explored during class
- Two 1 hour lectures per week ( Thursdays 11-12am and Fridays 9-10 am)

# Labs

- Weekly lab session
- Xilinx Vivado software: Download link: https://www.xilinx.com/support/download.html
- Will be using a Xilinx PYNQ board
- System Verilog (.sv files)
  - Very little change from Verilog 2001 (.v files)
  - Remember to use . sv suffix when creating RTL files!
- Labs all take place on Wednesday evenings
- Must have Vivado (v2018.2) installed and ready for first lab
- Mac issues: Contact Cormac Molloy

# Labs

- First submission is ungraded
  - FSM design
  - Code submitted for feedback
- Three graded labs (30% CA)
  - Automated Testbench for FSM, Design and Implementation of FIR, Calculator Design
  - Submit code and complete assessment for each lab
- Good comments are essential!
  - Structural comments divide code into different sections e.g. g.“Variable
  - Explain purpose of code blocks
  - Detail needed for more complex code

# Late Assignment Policy

- If a deadline is problematic for entire class, flag this early
- Late assignments will be accepted up to 1 week following a deadline, but marks will be halved.
- No marks available if assignment is more than 1 week late

# Plagiarism

- Plagiarism is taken extremely seriously
- All work must be your own
- All assignment material is examined and compared
- Having the same code/solution as someone else and passing it off as your own is plagiarism
- Any instances of plagiarism is UNACCEPTABLE and will result in loss of ALL marks for all parties

# Useful Resources

- PYNQ board reference library
  - http://www.pynq.io/board.html
- Verilog 2001 Reference
  - http://Sutherland-hdl.com/pdfs/verilog_2001_ref_guide.pdf
- Other resources:
  - Stack Overflow
  - Conference papers (Cliff Cummings (http://www.sunburst-design.com/papers/ ) and Stuart Sutherland (https://www.sutherland-hdl.com/papers.html ) are notable authors)
  - Asic World

# Questions?

- Post questions about lectures topics or labs on Blackboard Forum
- Can also contact me or Dr. Shreejith directly via trinity email, Libin.mathew@tcd.ie, shankers@tcd.ie