Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
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EEU44C01-1

FACULTY OF SCIENCE, TECHNOLOGY, ENGINEERING AND MATHEMATICS

SCHOOL OF ENGINEERING

Electronic and Electrical Engineering

Engineering **Semester 2, 2022**

Senior Sophister

Integrated Systems Design

06/05/2022 **RDS Main Hall** **14:00–16:00**

Asst. Prof. S. Shanker, George Duffy

Instructions to candidates:

Answer all questions.

Acronyms used in this paper:

ASIC	Application Specific Integrated Circuits
FPGA	Field Programmable Gate Arrays
FSM	Finite State Machine
LUT	Look-Up Table
IP	Intellectual Property

All symbols have usual meanings

Q.1 **[Total: 25 marks]**

(a) In each of the following scenarios, state whether the value assigned to d is **signed** or **unsigned**. Give reason(s) for your answer.

```
reg          [2:0] a;
reg signed   [2:0] b;
reg signed   [1:0] c;
reg signed   [3:0] d;
assign a = 3'd2;
assign b = 3'd2;
assign c = -2'd1;
```

i) d = b + c;

ii) d = $signed(a) + c[0];

iii) d = $signed(a) + b;

[9 marks]

(b) A verification engineer is designing a testbench for Verilog code. They wish to generate N periods of a 1-bit clock signal div8. The period length of div8 should be 8 times larger than the period of input clock clk. Write a Verilog task that will take N as a variable input, initialise a 1-bit signal div8 at zero, then generate N periods of the clock signal div8. The duty cycle of div8 should be $1/8$ (i.e. div8 should be high for $1/8$ of its period). You may assume div8 is already declared outside the task.

[10 marks]

(c) Referring back to part b, explain why we use a **task** and not a **function** in this circumstance. **[2 marks]**

(d) The verification engineer now wishes to edit the test to make it self-checking. Provide two reasons supporting this design choice for the test bench. **[4 marks]**

Q.2 **[Total: 25 marks]**

A design requires the detection of a particular 6-bit pattern on a serial input. This is to be controlled by a Finite State Machine. You are given the following information:

i) The sequence your FSM should detect is $0 \rightarrow 1 \rightarrow 1 \rightarrow 0 \rightarrow 0 \rightarrow 1$

ii) Your FSM has 4 inputs:

   (a) **clk:** clock signal

   (b) **reset:** active-high, synchronous reset signal

   (c) **serial_in:** 1-bit serial data which is considered valid when **serial_in_vld** is high.

   (d) **serial_in_vld:** 1-bit signal which indicates that the value on **serial_in** is valid for this clock cycle.

iii) Your FSM has 2 outputs:

   (a) **seq_found:** 1-bit signal indicates that the sequence has been detected. This should stay high until the next valid input

   (b) **seq_interrupted:** 1-bit signal that indicates that after at least 3 valid bits the sequence has been interrupted.

iv) Valid sequences may overlap

(a) Provide a state diagram to define the state transition logic and any outputs. **[10 marks]**

(b) Define a test plan for your design, giving a brief outline of each testcase that you would use to verify your design. **[10 marks]**

(c) Provide a brief justification of design choices (e.g. number of states/ bits used to represent them, possible edge cases considered, moore vs mealy). **[5 marks]**

Q.3 **[Total: 25 marks]**

(a) A 3-tap filter is assumed to have the following impulse response:

$$y(n) = \sum_{k=0}^{3} a_k \times x(n-k)$$

i) Draw a simple diagram of this system.

ii) Compute a limit on the Fclk of the system, using T_A and T_M to denote the delay through an adder and a multiplier respectively.

iii) Draw an additional diagram to demonstrate how pipelining could affect Fclk.

iv) Provide an expression for output y_{pp} the output of the pipelined system.

v) Determine the latency and throughput of the non-pipelined and the pipelined model.

[15 marks]

(b) Draw a waveform diagram representing an AXI stream transaction for an AXI manager transmitting six 8-bit words. Assume the AXI subordinate can capture four words per clock cycle and processes two word per clock cycle. **[10 marks]**

Q.4 **[Total: 25 marks]**

(a) Define the terms **truncation** and **rounding** in the context of hardware arithmetic. Briefly explain their effects in terms of error and hardware cost. **[5 marks]**

(b) Draw the basic diagram of a **DSP Slice** from an FPGA and describe how they can be used for building symmetric FIR filters. **[10 marks]**

(c) What is the difference between Hard IP and Soft IP cores? Give an example of each of them. **[4 marks]**

(d) An algorithm you are implementing on an FPGA involves multiplication with a fixed constant. Show how you would implement this without using DSP blocks and comment on the hardware cost and performance impact of this approach. **[6 marks]**