Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
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FACULTY OF ENGINEERING, MATHEMATICS & SCIENCE

SCHOOL OF ENGINEERING

Electronic & Electrical Engineering

Engineering **Semester 2, 2019**

Senior Sophister

Annual Examinations

INTEGRATED SYSTEMS DESIGN (EEU44C01-1)

24th April 2019 **RDS Simmonscourt** **09.30 – 11.30**

Rhona Wade

Instructions to Candidates:

Answer FOUR questions in total.

Question 1 is COMPULSORY.

Answer any THREE of the remaining questions.

All questions carry equal marks.

Materials Permitted for this Examination:

Calculator

Drawing Instruments

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Q.1

(a) Convert -0.1220703125 to a two's complement 8-bit fixed point representation, highlighting any rounding or truncation used.

(b) An 8-bit and a 10-bit number are multiplied. Assuming no sign bit in either number, how many bits should be used to store the result?

(c) Comment on two differences between Verilog system tasks $monitor and $display.

(d) If memory is described as ***volatile***, what does this mean?

(e) Outline briefly the difference between distributed RAM and block RAM on FPGAs.

(f) What impact does an ADC have on digital filter performance?

(g) In a basic testbench we manually drive the test stimulus and observe the waveforms to assess a system. Briefly describe two disadvantages of this type of testbench.

(h) If design confidence is the major concern, which is more suitable: Soft IP or Hard IP? Explain briefly.

(i) What potential synthesis issue can you see with the following piece of code:

```
always @ (*) begin
    if (sel == 1'b1) begin
        f = a;
    end
end
```

(j) What is the role of a synchronisation circuit in a VGA display?

[25 marks]

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Q.2

(a) The plots in **Fig Q.2** A, B, C and D (overleaf) show the magnitude responses of four FIR lowpass filters. One of the filters is not quantised. This filter was designed with a sampling rate of 16 kHz, with passband and stopband frequencies of 2000 Hz and 2350 Hz respectively. The original 120 filter coefficients are quantised to obtain the remaining three filters.

By inspecting the magnitude responses:

i. Identify which of the filters is not quantised.

ii. Of the remaining filters, match the filters to the following levels of quantisation in terms of LSB size: $2^{-16}, 2^{-10}, 2^{-6}$.

iii. If the filter has been designed to remove a 2.5 kHz tone from a digitised speech signal, discuss the impact of different levels of quantisation on system performance.

Justify your answers with explicit references to the magnitude responses of the filters.

[15 marks]

(b) Describe with the aid of a diagram an implementation of a **linear-phase FIR filter**. With reference to group delay, describe why phase linearity is a useful property for a filter.

[10 marks]

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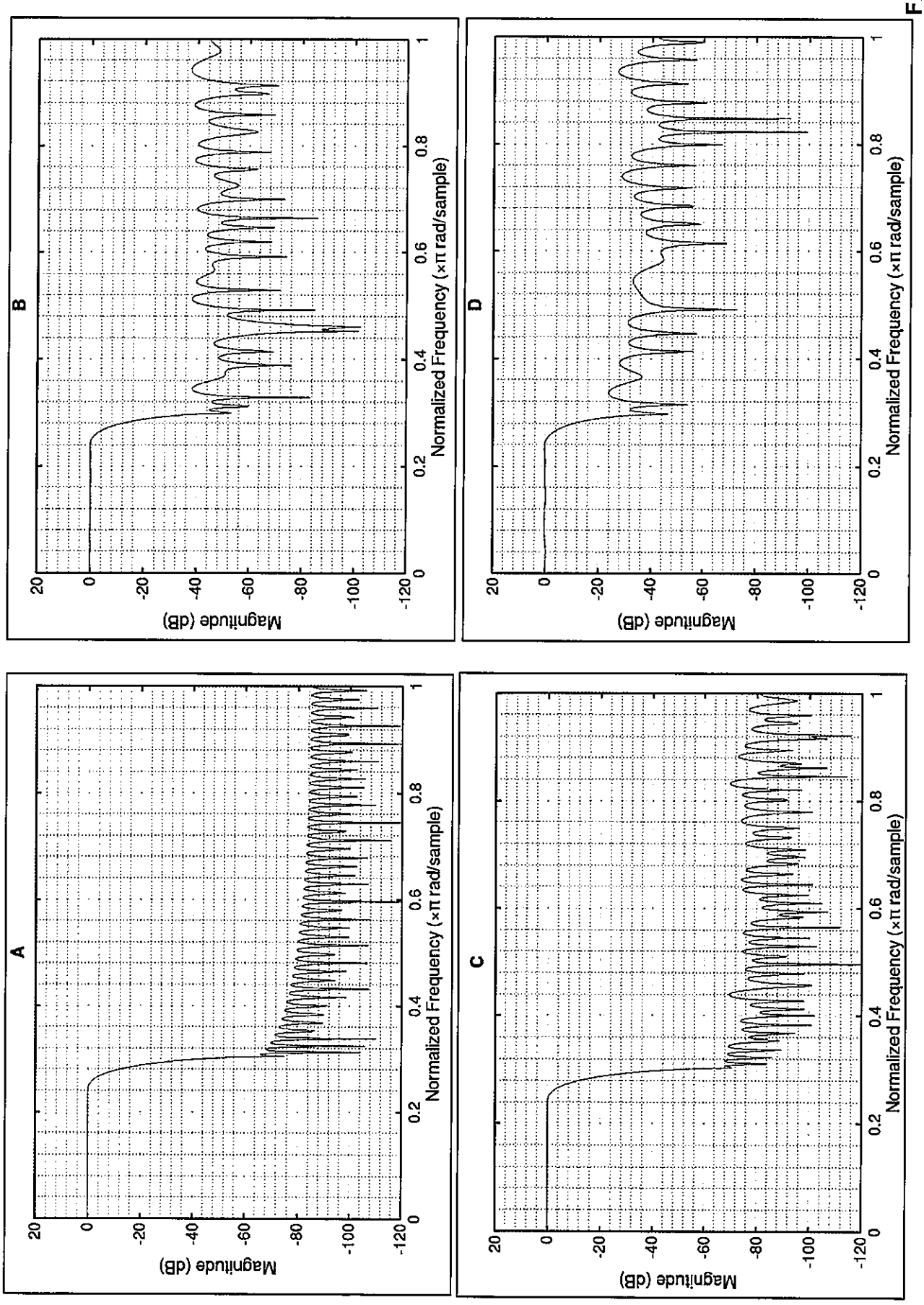
A
B
C
D
Magnitude (dB)
Normalized Frequency (×π rad/sample)
20
0
-20
-40
-60
-80
-100
-120
0
0.2
0.4
0.6
0.8
1

Fig Q.2

Q.3

(a) Define what is meant by **latency** and **throughput** in the context of hardware design. Briefly explain how each of these properties impact data output from an FIR filter.

[7 marks]

(b) **Parallelism** and **pipelining** are two design methods that can be used to increase the throughput of a digital system.

(i) Explain with the aid of a diagram how **pipelining** can be used to increase the throughput of an FIR filter. Use T_A and T_M to denote the delay through an adder and a multiplier respectively.

[8 marks]

(ii) Show mathematically that pipelining adds latency but does not otherwise change the output of a pipelined FIR filter of length three. You may assume the impulse response of the filter before pipelining is given as

$$y(n) = ax(n) + bx(n-1) + cx(n-2)$$

[6 marks]

(iii) What is the necessary relationship between sample frequency F_{sample} and clock frequency F_{clock} to implement the **parallelised** system shown in **Fig Q.3**.

[4 marks]

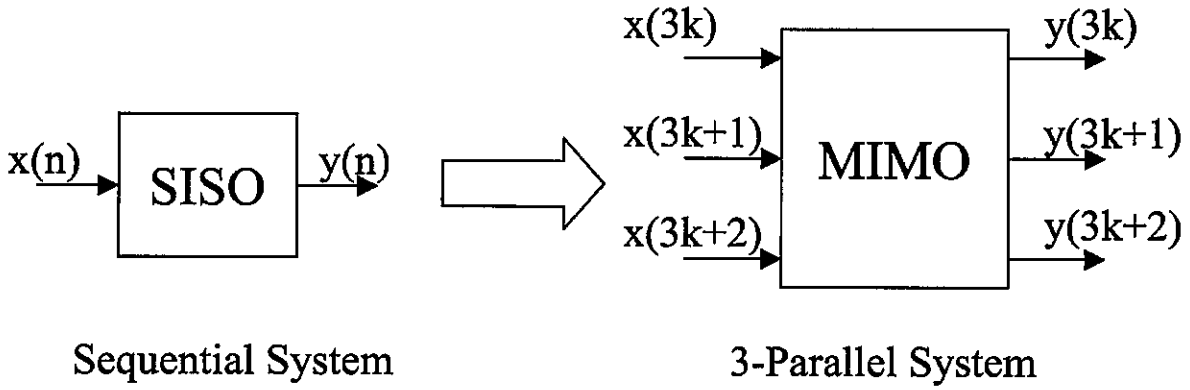

Fig Q.3

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Q.4

(a) Define what is meant by **truncation** and **rounding** in the context of hardware arithmetic. Explain why truncation causes bias specifically in two's complement numbering systems. Provide an upper bound on truncation error due to coefficient rounding in an N tap FIR filter.

[7 Marks]

(b) Define what is meant by **saturation** and **wrapping** in the context of hardware arithmetic. Comment on the comparative hardware cost of these schemes.

[4 Marks]

(c) Show how **multiplication** by a constant can be implemented as a combination of shifts and adders. Comment on the hardware cost of this approach to multiplication.

[4 Marks]

(d) Draw a basic diagram of a **DSP slice** from an FPGA. Describe how DSP slices may be used to implement symmetric FIR filters.

[10 Marks]

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Q.5

(a) What are IP Cores in the context of hardware design? Why are they useful? What is the difference between Hard IP and Soft IP cores? Give an example of each IP type.

[10 marks]

(b)

"Moore's Law is dead. Moore's Law is over."

– Mike Muller, CTO of ARM

Discuss whether or not you agree with this statement. Refer to trends in the semiconductor industry to support your argument.

[15 marks]

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