IHP

SG13G2

Layout Rules

Rev. 0.1 (2023-04-20)

License

Contents

1 General

1.1 Scope

This document describes the design rules for IHPs SG13G2 SiGe BiCMOS technology.

1.2 List of abbreviations

Table 1.1: List of abbreviations used within this document

Abbreviation	Explanation
BiCMOS	Bipolar CMOS
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
IHP	Innovations for High Performance Microelectronics
MIM	Metal-Insulator-Metal
NMOS	Negative Channel Metal Oxide Semiconductor
PMOS	Positive Channel Metal Oxide Semiconductor
RD	Reference Document
SiGe	Silicon Germanium

1.3 Reference documents

[RD 1] IHP SG13G2 Process specification Rev. 1.3

2 Layer table

This chapter is a documentation of IHP layers definition which is valid in all technologies.

Remark: Only the layers described in the following table are allowed to be used in layout designs. Do not use layers exclusively reserved for internal usage.

Layer name	Purpose	GDS Number	GDS Datatype	Description
L0	drawing	0	0	Reserved for internal use
Activ	drawing	1	0	Defines active regions in substrate, where transistors, diodes and/or capacitors will be fabricated
Activ	label	1	1	Lable in activ layer
Activ	pin	1	2	Pin in active layer
Activ	net	1	3	
Activ	boundary	1	4	
Activ	lvs	1	19	
Activ	mask	1	20	added to Active:drawing at mask generation
Activ	filler	1	22	Activ filler layer
Activ	nofill	1	23	Filler exclusion definition layer
Activ	OPC	1	26	Activ outer OPC definition layer
Activ	iOPC	1	27	Activ inner OPC definition layer
Activ	noqrc	1	28	No parasitics extraction
L2	drawing	2	0	Reserved for internal use
BiWind	drawing	3	0	Defines active npn collector region
BiWind	OPC	3	26	BiWind OPC definition layer
GatPoly	drawing	5	0	Defines polysilicon gates and interconnect, GatPoly = GatPoly OR PolyRes see section
GatPoly	label	5	1	
GatPoly	pin	5	2	Defines polysilicon gates and interconnect, GatPoly = GatPoly OR PolyRes see section
GatPoly	net	5	3	
GatPoly	boundary	5	4	
GatPoly	filler	5	22	Gatfiller layer
GatPoly	nofill	5	23	Filler exclusion definition layer
GatPoly	OPC	5	26	GatPoly outer OPC definition layer
GatPoly	iOPC	5	27	GatPoly inner OPC definition layer
GatPoly	noqrc	5	28	No parasitics extraction
Cont	drawing	6	0	Defines 1-st metal contacts to Activ, GatPoly

Cont	net	6	3	
Cont	boundary	6	4	
Cont	OPC	6	26	Cont OPC definition layer
nSD	drawing	7	0	nSD = NOT (pSD OR nSDBlock), or nSD=pSD is recognized as Rhigh
nSD	block	7	21	Defines areas which do not receive S/D implants
Metal1	drawing	8	0	Defines 1-st metal interconnect
Metal1	label	8	1	
Metal1	pin	8	2	
Metal1	net	8	3	
Metal1	boundary	8	4	
Metal1	mask	8	20	added to Metal1:drawing at mask generation
Metal1	filler	8	22	Metal1 filler layer
Metal1	nofill	8	23	Filler exclusion definition layer
Metal1	slit	8	24	Metal Slit definition layer
Metal1	text	8	25	Text layer for Metal1, used for LVS
Metal1	OPC	8	26	Metal1 OPC definition layer
Metal1	noqrc	8	28	No parasitics extraction
Metal1	res	8	29	Wire resistor
Metal1	iprobe	8	33	Current probe (capable for QRC)
Metal1	diffprb	8	34	Differential current probe (capable for QRC)
Passiv	drawing	9	0	Defines regions where passivation coating is removed
Passiv	label	9	1	
Passiv	pin	9	2	
Passiv	net	9	3	
Passiv	boundary	9	4	
Passiv	pdl	9	40	Plasma dicing line
Passiv	sbump	9	36	
Passiv	pillar	9	35	
Metal2	drawing	10	0	Defines 2-nd metal interconnect
Metal2	label	10	1	
Metal2	pin	10	2	
Metal2	net	10	3	
Metal2	boundary	10	4	
Metal2	mask	10	20	added to Metal2:drawing at mask generation
Metal2	filler	10	22	Metal2 filler layer
Metal2	nofill	10	23	Filler exclusion definition layer

Metal2	slit	10	24	Metal Slit definition layer
Metal2	text	10	25	Text layer for Metal2, used for LVS
Metal2	OPC	10	26	Metal2 OPC definition layer
Metal2	noqrc	10	28	No parasitics extraction
Metal2	res	10	29	Wire resistor
Metal2	iprobe	10	33	Current probe (capable for QRC)
Metal2	diffprb	10	34	Differential current probe (capable for QRC)
BasPoly	drawing	13	0	Defines npn base poly region
BasPoly	label	13	1	
BasPoly	pin	13	2	
BasPoly	net	13	3	
BasPoly	boundary	13	4	
pSD	drawing	14	0	Defines areas to receive P+ source/drain implant
NLDB	drawing	15	0	Reserved for internal LDMOS development
DigiBnd	drawing	16	0	surrounds areas were digital DRC is valid
DigiBnd	drawing0	16	10	Used to exclude recommended rules in digital blocks, for instance for SG25_dcell library
Via1	drawing	19	0	Defines 1-st metal to 2-nd metal contact
Via1	net	19	3	
Via1	boundary	19	4	
BackMetal1	drawing	20	0	Defines 1-st back-side metal interconnect
BackMetal1	label	20	1	
BackMetal1	pin	20	2	
BackMetal1	net	20	3	
BackMetal1	boundary	20	4	
BackMetal1	mask	20	20	added to BackMetal1:drawing at mask generation
BackMetal1	filler	20	22	BackMetal1 filler layer
BackMetal1	nofill	20	23	Filler exclusion definition layer
BackMetal1	slit	20	24	Metal Slit definition layer
BackMetal1	text	20	25	Text layer for BackMetal1, used for LVS
BackMetal1	OPC	20	26	BackMetal1 OPC definition layer
BackMetal1	noqrc	20	28	No parasitics extraction
BackMetal1	res	20	29	Wire resistor
BackMetal1	iprobe	20	33	Current probe (capable for QRC)
BackMetal1	diffprb	20	34	Differential current probe (capable for QRC)
BackPassiv	drawing	23	0	Defines regions where passivation coating is removed

RES	drawing	24	0	Identifies resistor areas
RES	label	24	1	
SRAM	drawing	25	0	Identifies memory areas
SRAM	label	25	1	
SRAM	boundary	25	4	
TRANS	drawing	26	0	Identifies bipolar transistor areas
IND	drawing	27	0	Identifies inductor areas
IND	pin	27	2	
IND	boundary	27	4	
IND	text	27	25	
SalBlock	drawing	28	0	Defines non salicided Activ and GatPoly, BasPoly areas
Via2	drawing	29	0	Defines 2-nd metal to 3-rd metal contact Via2 = Via2 OR Vmim see section
Via2	net	29	3	
Via2	boundary	29	4	
Metal3	drawing	30	0	Defines 3-rd metal interconnect
Metal3	label	30	1	
Metal3	pin	30	2	
Metal3	net	30	3	
Metal3	boundary	30	4	
Metal3	mask	30	20	added to Metal3:drawing at mask generation
Metal3	filler	30	22	Metal3 filler layer
Metal3	nofill	30	23	Filler exclusion definition layer
Metal3	slit	30	24	Metal Slit definition layer
Metal3	text	30	25	Text layer for Metal3, used for LVS
Metal3	OPC	30	26	Metal3 OPC definition layer
Metal3	noqrc	30	28	No parasitics extraction
Metal3	res	30	29	Wire resistor
Metal3	iprobe	30	33	Current probe (capable for QRC)
Metal3	diffprb	30	34	Differential current probe (capable for QRC)
NWell	drawing	31	0	Defines the regions that receive P-Channel VT adjust, P-Channel Punch-Through and N-Well implants
NWell	label	31	1	
NWell	pin	31	2	
NWell	net	31	3	
NWell	boundary	31	4	
nBuLay	drawing	32	0	Defines bipolar sub collector and isolated NMOS devices

nBuLay	label	32	1	
nBuLay	pin	32	2	
nBuLay	net	32	3	
nBuLay	boundary	32	4	
nBuLay	block	32	21	Defines areas where no nBuLay implant is allowed
EmWind	drawing	33	0	Defines npn emitter window
EmWind	OPC	33	26	EmWind OPC definition layer
DeepCo	drawing	35	0	Defines deep collector regions
MIM	drawing	36	0	Defines Metal-Insulator-Metal capacitor area
MIM	net	36	3	
MIM	boundary	36	4	
EdgeSeal	drawing	39	0	Edge Seal definition layer, reserved for internal use only
EdgeSeal	boundary	39	4	Defines the outer extends of the sealring
Substrate	drawing	40	0	Substrate recognition layer for LVS
Substrate	text	40	25	Substrate recognition text for LVS
dfpad	drawing	41	0	Pad recognition layer
dfpad	pillar	41	35	Copper pillar pad recognition layer
dfpad	sbump	41	36	Solder bump pad recognition layer
ThickGateOx	drawing	44	0	Thick Gate Oxide
PLDB	drawing	45	0	Reserved for internal LDMOS development
PWell	drawing	46	0	Reserved for internal use
PWell	label	46	1	
PWell	pin	46	2	
PWell	net	46	3	
PWell	boundary	46	4	
PWell	block	46	21	Defines areas where no well implants are allowed PWL:=NOT(NWell OR PWellBlock)
Via3	drawing	49	0	Defines 3-rd metal to 4-th metal contact
Via3	net	49	3	
Via3	boundary	49	4	
Metal4	drawing	50	0	Defines 4-th metal interconnect
Metal4	label	50	1	
Metal4	pin	50	2	Defines 4-th metal interconnect
Metal4	net	50	3	
Metal4	boundary	50	4	
Metal4	mask	50	20	added to Metal4:drawing at mask generation

Metal4	filler	50	22	Metal4 filler layer, only for thick and thin metal 5 option
Metal4	nofill	50	23	Filler exclusion definition layer, only for thick and thin metal 5 option
Metal4	slit	50	24	Metal Slit definition layer
Metal4	text	50	25	Text layer for Metal4, used for LVS
Metal4	OPC	50	26	Metal4 OPC definition layer
Metal4	noqrc	50	28	No parasitics extraction
Metal4	res	50	29	Wire resistor
Metal4	iprobe	50	33	Current probe (capable for QRC)
Metal4	diffprb	50	34	Differential current probe (capable for QRC)
HeatTrans	drawing	51	0	Defines heat source for transistors
HeatRes	drawing	52	0	Defines heat source for resistors
FBE	drawing	54	0	Fluidic back side etch
EmPoly	drawing	55	0	Defines npn emitter poly region and pnp base poly region
DigiSub	drawing	60	0	Substrate recognition layer for LVS
NoDRC	drawing	62	0	Excludes areas from design rule checking, refer to sec.
TEXT	drawing	63	0	Macrocell name, element text layer
Via4	drawing	66	0	Defines 4-th metal to 5-th metal contact
Via4	net	66	3	
Via4	boundary	66	4	
Metal5	drawing	67	0	Defines 5-th metal interconnect, only for thick metal 5 option
Metal5	label	67	1	
Metal5	pin	67	2	Defines 5-th metal interconnect, only for thick metal 5 option
Metal5	net	67	3	
Metal5	boundary	67	4	
Metal5	mask	67	20	added to Metal5:drawing at mask generation
Metal5	filler	67	22	Metal5 filler layer, reserved for internal use
Metal5	nofill	67	23	Filler exclusion definition layer, reserved for internal use
Metal5	slit	67	24	Metal Slit definition layer, only for thick metal 5 option
Metal5	text	67	25	Text layer for Metal5
Metal5	OPC	67	26	Metal5 OPC definition layer
Metal5	noqrc	67	28	No parasitics extraction
Metal5	res	67	29	Wire resistor
Metal5	iprobe	67	33	Current probe (capable for QRC)

Metal5	diffprb	67	34	Differential current probe (capable for QRC)
RadHard	drawing	68	0	Layer used in special technologies to define regions were special radiation hard design rules should apply
MemCap	drawing	69	0	Defines position of RFMEMS cap
Varicap	drawing	70	0	Well implant for varicap devices
IntBondVia	drawing	72	0	Via on top of interposer's TopMetal2
IntBondMet	drawing	73	0	Metal connected to IntBondVia
DevBondVia	drawing	74	0	Via on top of device's TopMetal2
DevBondMet	drawing	75	0	Metal connected to DevBondVia
DevTrench	drawing	76	0	Deep trench from front side for plasma dicing approach
Redist	drawing	77	0	Redistribution layer for metal wiring after chip IO
GraphBot	drawing	78	0	1st graphene layer
GraphTop	drawing	79	0	2nd graphene layer
AntVia1	drawing	83	0	Deep via between TopMetal2 and AntMetal1
AntMetal2	drawing	84	0	Extra second-metal layer for antenna and passive integration
GraphCont	drawing	85	0	GraphBot, GraphTop and GraphGat to GraphMetal1 or GraphMet1L contact
SiWG	drawing	86	0	Backend integrated Si waveguide
SiWG	filler	86	22	Si waveguide filler layer
SiWG	nofill	86	23	Si waveguide filler exclusion layer
SiGrating	drawing	87	0	Si waveguide etching layer
SiNGrating	drawing	88	0	SiN waveguide etching layer
GraphPas	drawing	89	0	Additional passivation for graphene structures
EmWind3	drawing	90	0	Defines G3 npn emitter window
EmWiHV3	drawing	91	0	Defines G3 HV npn emitter window
RedBuLay	drawing	92	0	Burried Layer with reduced dose for isolated NLDMOS
SMOS	drawing	93	0	Extraction recognition layer for special CMOS devices
GraphPad	drawing	97	0	Passivation opening
Polimide	drawing	98	0	Reserved for future use
Polimide	label	98	1	
Polimide	pin	98	2	
Polimide	net	98	3	
Recog	drawing	99	0	general device recognition shape for device extraction
Recog	pin	99	2	general device pin

Recog	esd	99	30	ESD device recognition layer
Recog	diode	99	31	Active diode recognition layer
Recog	tsv	99	32	TSV device recognition layer
Recog	iprobe	99	33	Current probe (capable for QRC)
Recog	diffprb	99	34	Differential current probe (capable for QRC)
Recog	pillar	99	35	Copper pillar pad recognition layer
Recog	sbump	99	36	Solder bump pad recognition layer
Recog	otp	99	37	OTP device recognition layer
Recog	pdiode	99	38	Enables extraction of parasitic diodes
Recog	mom	99	39	Metal-on-metal (MOM) capacitor recognition layer
Recog	pcm	99	100	Process control structure recognition layer
ColOpen	drawing	101	0	Defines additional collector opening in SG13 HBTs
GraphMetal1	drawing	109	0	Graphene-metal standard interconnect
GraphMetal1	filler	109	22	Graphene-metal filler layer
GraphMetal1	nofill	109	23	Graphene-metal filler exclusion layer
GraphMetal1	slit	109	24	Graphene-metal slitting layer
GraphMetal1	OPC	109	26	Graphene-metal opc
GraphMet1L	drawing	110	0	Graphene-metal lift-off interconnect
GraphMet1L	filler	110	22	Graphene-metal lift-off filler layer
GraphMet1L	nofill	110	23	Graphene-metal lift-off filler exclusion layer
GraphMet1L	slit	110	24	Graphene-metal lift-off slitting layer
GraphMet1L	OPC	110	26	Graphene-metal lift-off opc
EXTBlock	drawing	111	0	Block tip and halo implants
NLDD	drawing	112	0	Dedicated pwell body for NLDMOS
PLDD	drawing	113	0	Dedicated nwell body for PLDMOS
NExt	drawing	114	0	Reserved for internal LDMOS development
PExt	drawing	115	0	Reserved for internal use
NExtHV	drawing	116	0	Reserved for internal use
PExtHV	drawing	117	0	Reserved for internal use
GraphGate	drawing	118	0	Graphene GFET gate
SiNWG	drawing	119	0	Backend integrated SiN waveguide
SiNWG	filler	119	22	SiN waveguide filler layer
SiNWG	nofill	119	23	SiN waveguide filler exclusion layer
MEMPAD	drawing	124	0	Dedicated to open Pads in RF-MEMS module
TopVia1	drawing	125	0	Defines 3-rd (or 5-th) metal to TopMetal1 contact

TopVia1	net	125	3	
TopVia1	boundary	125	4	
TopMetal1	drawing	126	0	Defines 1-st thick TopMetal layer
TopMetal1	label	126	1	
TopMetal1	pin	126	2	Defines 1-st thick TopMetal layer
TopMetal1	net	126	3	
TopMetal1	boundary	126	4	
TopMetal1	mask	126	20	added to TopMetal1:drawing at mask generation
TopMetal1	filler	126	22	TopMetal1 filler layer
TopMetal1	nofill	126	23	TopMet1Flr exclusion layer
TopMetal1	slit	126	24	TopMet1 Slit definition layer
TopMetal1	text	126	25	Text layer for TopMetal1, used for LVS
TopMetal1	noqrc	126	28	No parasitics extraction
TopMetal1	res	126	29	Wire resistor
TopMetal1	iprobe	126	33	Current probe (capable for QRC)
TopMetal1	diffprb	126	34	Differential current probe (capable for QRC)
INLDPWL	drawing	127	0	Dedicated PWell body for isolated NLDMOS
PolyRes	drawing	128	0	used for mark net resistors, see GatPoly = GatPoly OR PolyRes
PolyRes	label	128	1	
PolyRes	pin	128	2	Defines polysilicon gates and interconnect, GatPoly = GatPoly OR PolyRes see section
PolyRes	net	128	3	
PolyRes	boundary	128	4	
Vmim	drawing	129	0	used for mark net mim capacitors see Via2 = Via2 OR Vmim
nBuLayCut	drawing	131	0	P-separation implat INLDMOS (internal use)
AntMetal1	drawing	132	0	Extra first-metal layer for antenna and passive integration
TopVia2	drawing	133	0	Defines via between TopMetal1 and TopMetal2
TopVia2	net	133	3	
TopVia2	boundary	133	4	
TopMetal2	drawing	134	0	Defines 2-nd thick TopMetal layer
TopMetal2	label	134	1	
TopMetal2	pin	134	2	Defines 2-nd thick TopMetal layer
TopMetal2	net	134	3	
TopMetal2	boundary	134	4	
TopMetal2	mask	134	20	added to TopMetal2:drawing at mask generation

TopMetal2	filler	134	22	Filler exclusion layer for TopMetal2
TopMetal2	nofill	134	23	Filler exclusion layer for TopMetal2
TopMetal2	slit	134	24	TopMetal2 Slit definition layer
TopMetal2	text	134	25	Text layer for TopMetal2
TopMetal2	noqrc	134	28	No parasitics extraction
TopMetal2	res	134	29	Wire resistor
TopMetal2	iprobe	134	33	Current probe (capable for QRC)
TopMetal2	diffprb	134	34	Differential current probe (capable for QRC)
SNSRing	drawing	135	0	Sensor package ring
Sensor	drawing	136	0	
SNSArms	drawing	137	0	Arms of the Sensor
SNSCMOSVia	drawing	138	0	Defines via between BiCMOS wafer and sensor
ColWind	drawing	139	0	Defines enclosed active transistor region
FLM	drawing	142	0	Defines fluidic channel
HafniumOx	drawing	143	0	RRAM – reduced MIM layer
MEMVia	drawing	145	0	Local Vias within RFM area
ThinFilmRes	drawing	146	0	ThinFilmRes (V) and recognition layer for RFMEMS
RFMEM	drawing	147	0	Areas for integrated RF MEMS devices
NoRCX	drawing	148	0	No parasitics extraction
NoRCX	m2m3	148	41	No parasitics extraction in Metal2 and Metal3
NoRCX	m2m4	148	42	No parasitics extraction in Metal2 and Metal4
NoRCX	m2m5	148	43	No parasitics extraction in Metal2 and Metal5
NoRCX	m2tm1	148	44	No parasitics extraction in Metal2 and TopMetal1
NoRCX	m2tm2	148	45	No parasitics extraction in Metal2 and TopMetal2
NoRCX	m3m4	148	46	No parasitics extraction in Metal3 and Metal4
NoRCX	m3m5	148	47	No parasitics extraction in Metal3 and Metal5
NoRCX	m3tm1	148	48	No parasitics extraction in Metal3 and TopMetal1
NoRCX	m3tm2	148	49	No parasitics extraction in Metal3 and TopMetal2
NoRCX	m4m5	148	50	No parasitics extraction in Metal4 and Metal5
NoRCX	m4tm1	148	51	No parasitics extraction in Metal4 and TopMetal1
NoRCX	m4tm2	148	52	No parasitics extraction in Metal4 and TopMetal2
NoRCX	m5tm1	148	53	No parasitics extraction in Metal5 and TopMetal1

NoRCX	m5tm2	148	54	No parasitics extraction in Metal5 and TopMetal2
NoRCX	tm1tm2	148	55	No parasitics extraction in TopMetal1 and TopMetal2
NoRCX	m1sub	148	123	No parasitics extraction in Metal1 and Substrate
NoRCX	m2sub	148	124	No parasitics extraction in Metal2 and Substrate
NoRCX	m3sub	148	125	No parasitics extraction in Metal3 and Substrate
NoRCX	m4sub	148	126	No parasitics extraction in Metal4 and Substrate
NoRCX	m5sub	148	127	No parasitics extraction in Metal5 and Substrate
NoRCX	tm1sub	148	300	No parasitics extraction in TopMetal1 and Substrate
NoRCX	tm2sub	148	301	No parasitics extraction in TopMetal2 and Substrate
SNSBotVia	drawing	149	0	Sensor bottom via
SNSTopVia	drawing	151	0	Sensor top via
DeepVia	drawing	152	0	Through Silicon Via
FGEtch	drawing	153	0	At this place the 1-st poly-Si layer (floating-gate) is etched before the 2-nd poly-Si layer (control-gate) is deposited
CtrGat	drawing	154	0	This layer patterns the 2-nd poly-Si layer (control-gate)
FGImp	drawing	155	0	Defines areas where the Floating-gate is doped and the p-well of the flash-cells is formed
EmWiHV	drawing	156	0	EmWind layer for high voltage HBT
LBE	drawing	157	0	For localized back side etch
AlCuStop	drawing	159	0	Reserved for internal use
NoMetFiller	drawing	160	0	Exclude all metall filler
prBoundary	drawing	189	0	
prBoundary	label	189	1	
prBoundary	boundary	189	4	
Exchange0	drawing	190	0	
Exchange0	label	190	1	
Exchange0	pin	190	2	
Exchange0	text	190	25	
Exchange1	drawing	191	0	
Exchange1	label	191	1	
Exchange1	pin	191	2	

Exchange1	text	191	25	
Exchange2	drawing	192	0	
Exchange2	label	192	1	
Exchange2	pin	192	2	
Exchange2	text	192	25	
Exchange3	drawing	193	0	
Exchange3	label	193	1	
Exchange3	pin	193	2	
Exchange3	text	193	25	
Exchange4	drawing	194	0	
Exchange4	label	194	1	
Exchange4	pin	194	2	
Exchange4	text	194	25	

3 Physical layer design rules

3.1 NWell

Rule	Description	Value
NW.a	Min. **NWell** width	**0.62**
NW.b	Min. **NWell** space or notch (same net). NWell regions separated by less than this value will be merged.	**0.62**
NW.b1	Min. **PWell** width between **NWell** regions (different net)	**1.8**
NW.c	Min. **NWell** enclosure of **P+Activ1** (thin gate oxide)	**0.31**
NW.c1	Min. **NWell** enclosure of **P+Activ2** (thick gate oxide)	**0.62**
NW.d	Min. **NWell** space to external **N+Activ1**	**0.31**
NW.d1	Min. **NWell** space to external **N+Activ2**	**0.62**
NW.e	Min. **NWell** enclosure of NWell tie surrounded entirely by **NWell** in **N+Activ1**	**0.24**
NW.e1	Min. **NWell** enclosure of NWell tie surrounded entirely by **NWell** in **N+Activ2**	**0.62**
NW.f	Min. **NWell** space to substrate tie in **P+Activ1**	**0.24**
NW.f1	Min. **NWell** space to substrate tie in **P+Activ2**	**0.62**

Notes

1. **Activ** regions are allowed to cross well boundaries in some ESD protection layouts.
2. Substrate ties for internal logic are required due to p-silicon substrate.
3. **NWell** layers that justify the **nBuLay** conditions after a sizing of -1.0 µm/side are automatically copied to the **nBuLay** layer during mask generation. I.e. suffciently large **NWell** areas additionally receive **nBuLay** implants in order to reduce nwell sheet resistance and hence improve latchup robustness. Use **nBuLay:block** layer to prevent generation of **nBuLay** in **NWell**. Resistor areas marked by the layer **RES** are also excluded from automatic generation of **nBuLay** .
4. **PWell** is defined in all regions without **PWell:block** and without NWell. Goal is a certain **PWell** distance between **NWell** on different nets to prevent punchthrough due to different potentials.

3.2 PWell:block

PWell:block layer is used to generate regions where both **NWell** and **PWell** implants are blocked. The final mask data for mask PW is generated by PW:= NOT (NWell OR PWell:block).

Rule	Description	Value
PWB.a	Min. **PWell:block** width	**0.62**
PWB.b	Min. **PWell:block** space or notch	**0.62**
PWB.c	Min. **PWell:block** space to unrelated **NWell**	**0.62**
PWB.d	Min. **PWell:block** overlap of **NWell**	**0.0**
PWB.e	Min. **PWell:block** space to **N+Activ1** in **PWell** (thin gate oxide)	**0.31**
PWB.e1	Min. **PWell:block** space to **N+Activ2** in **PWell** (thick gate oxide)	**0.62**
PWB.f	Min. **PWell:block** space to **P+Activ1** in **PWell** (thin gate oxide)	**0.24**
PWB.f1	Min. **PWell:block** space to **P+Activ2** in **PWell** (thick gate oxide)	**0.62**

3.3 nBuLay

nBuLay is used for generating isolated n-channel devices.

Rule	Description	Value
NBL.a	Min. **nBuLay** width	**1.0**
NBL.b	Min. **nBuLay** space or notch (same net)	**1.5**
NBL.c	Min. **PWell** width between **nBuLay** (also generated **nBuLay** see Note2) regions (different net)	**3.2**
NBL.d	Min. **PWell** width between **nBuLay** and **NWell** (different net)	**2.2**
NBL.e	Min. **nBuLay** space to unrelated **N+Activ**	**1.0**
NBL.f	Min. **nBuLay** space to unrelated **P+Activ**	**0.5**

Notes

1. **PWell** is defined in all regions without **PWell:block** and without **NWell**. Goal is a certain **PWell** distance between **nBuLay** and **NWell** on different nets to prevent punchthrough due to different potentials
2. **nBuLay** is generated on **NWell** regions. **NWell** layers that justify the **nBuLay** conditions after a sizing of -1.0 µm/side are automatically copied to the **nBuLay** layer during mask generation. I.e. suffciently large **NWell** areas additionally receive **nBuLay** implants in order to reduce nwell sheet resistance and hence improve latchup robustness. Use **nBuLay:block** layer to prevent generation of **nBuLay** in **NWell**. Resistor areas marked by the layer **RES** are also excluded from automatic generation of **nBuLay**.

3.4 nBuLay:block

nBuLay:block is used for generating **NWell** structures, which are prevented from **nBuLay** implant.

Rule	Description	Value
NBL.a	Min. **nBuLay:block** width	**1.5**
NBL.b	Min. **nBuLay:block** space or notch	**1.0**
NBL.c	Min. **nBuLay** enclosure of **nBuLay:block**	**1.0**
NBL.d	Min. **nBuLay:block** space to unrelated **nBuLay**	**1.5**

Notes

1. **nBuLay** is used for generating isolated nmos devices (see rules nmosi).
2. Latchup prevention has to be carefully considered whenever **nBuLay:block** layer is used.

3.5 Activ

Rule	Description	Value
Act.a	Min. **Activ** width	**0.15**
Act.b	Min. **Activ** space or notch	**0.21**
Act.c	Min. **Activ** drain/source extension	**0.23**
Act.d	Min. **Activ** area (µm²)	**0.122**
Act.e	Min. **Activ** enclosed area (µm²)	**0.15**

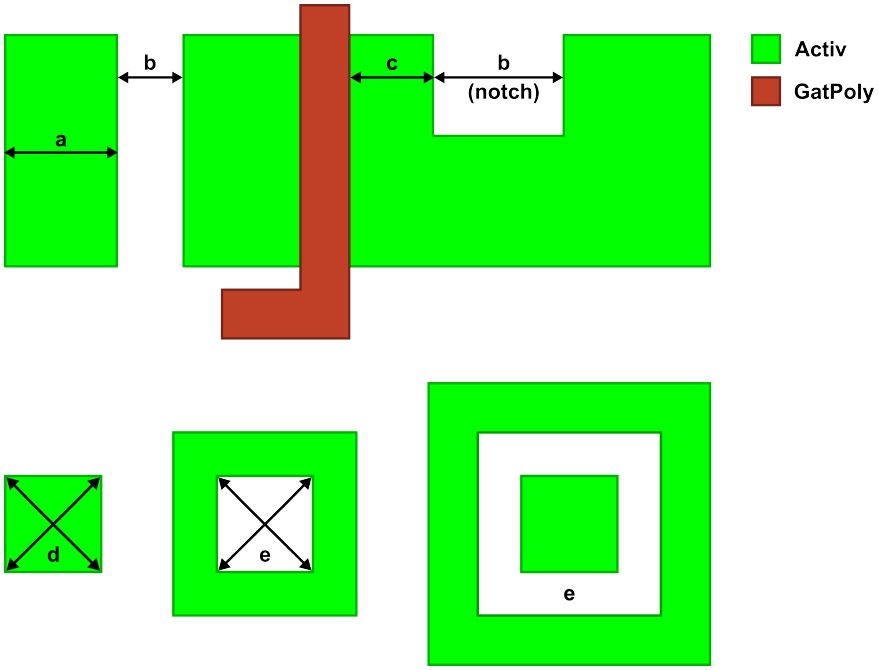

Figure 3.1: Activ dimensions

3.6 Activ:filler

Activ:filler patterns are required in order to improve wafer homogeneity in CMP process steps.

Rule	Description	Value
AFil.a	Max. **Activ:filler** width	**5.0**
AFil.a1	Min. **Activ:filler** width	**1.0**
AFil.b	Min. **Activ:filler** space	**1.0**
AFil.c	Min. **Activ:filler** space to **Cont**, **GatPoly**	**1.1**
AFil.c1	Min. **Activ:filler** space to **Activ**	**0.42**
AFil.d	Min. **Activ:filler** space to **NWell**, **nBuLay**	**1.0**
AFil.e	Min. **Activ:filler** space to **TRANS**	**1.0**
AFil.g	Min. global **Activ** density [%]	**35.0**
AFil.g1	Max. global **Activ** density [%]	**55.0**
AFil.g2	Min. **Activ** coverage ratio for any 800 x 800 µm² chip area [%]	**25.0**
AFil.g3	Max. **Activ** coverage ratio for any 800 x 800 µm² chip area [%]	**65.0**
AFil.i	Min. **Activ:filler** space to edges of **PWell:block**	**1.5**
AFil.j	Min. **nSD:block** and **SalBlock** enclosure of **Activ:filler** inside **PWell:block**	**0.25**

Notes

1. **Activ:nofill** layer can be used for filler pattern exclusion within specific device areas such as inductors or transformers as long as AFil.g2 and AFil.g3 are fulfilled. For larger sensitive areas it is recommended to minimize the conductivity of ActFillers by using **SalBlock**, **nSD:block** and **PWell:block**.
2. Default filler size 3.4 x 3.4 µm2 and 1.6 µm spacing is recommended with pattern density of approx. 46%. Offset in 4.7 is 2.5 µm. Depending on layout, filler size can be changed between 2.3 µm and 4.6 µm which lead to pattern densites between 35% and 55%.

3.7 ThickGateOxide

Rule	Description	Value
TGO.a	Min. **ThickGateOx** extension over **Activ**	**0.27**
TGO.b	Min. space between **ThickGateOx** and **Activ** outside thick gate oxide region	**0.27**
TGO.a	Min. **ThickGateOx** extension over **GatPoly** over **Activ**	**0.34**
TGO.d	Min. space between **ThickGateOx** and **GatPoly** over **Activ** outside thick gate oxide region	**0.34**
TGO.e	Min. **ThickGateOx** space (merge if less than this value)	**0.86**
TGO.f	Min. **ThickGateOx** width	**0.86**

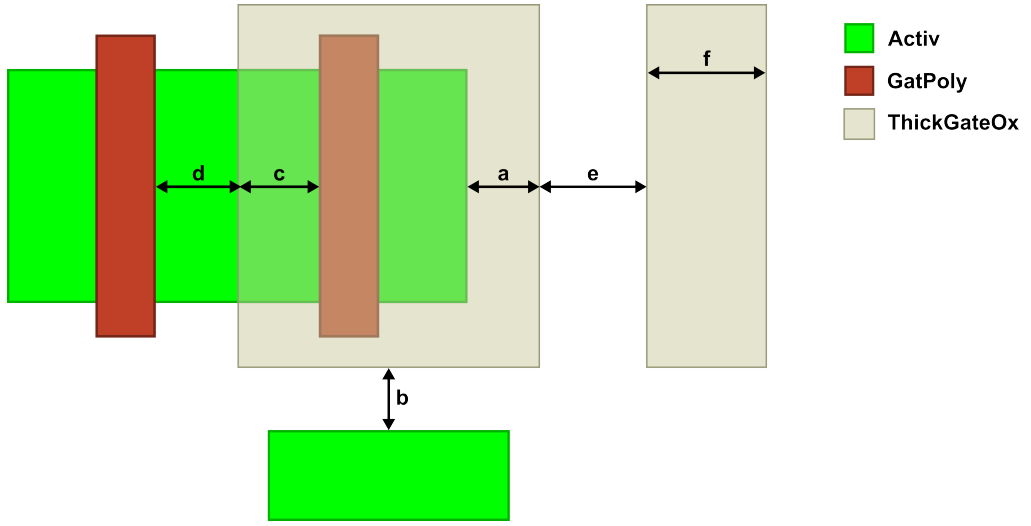

Figure 3.2: ThickGateOx dimensions

3.8 GatPoly

Rule	Description	Value
Gat.a	Min. **GatPoly** width	**0.13**
Gat.a1	Min. **GatPoly** width for channel length of 1.2 V NFET	**0.13**
Gat.a2	Min. **GatPoly** width for channel length of 1.2 V PFET	**0.13**
Gat.a3	Min. **GatPoly** width for channel length of 3.3 V NFET	**0.45**
Gat.a4	Min. **GatPoly** width for channel length of 3.3 V PFET	**0.4**
Gat.b	Min. **GatPoly** space or notch	**0.18**
Gat.b1	Min. space between unrelated 3.3 V **GatPoly** over **Activ** regions	**0.25**
Gat.c	Min. **GatPoly** and **GatPoly:filler** extension over **Activ** (end cap)	**0.18**
Gat.d	Min. **GatPoly** space to **Activ**	**0.07**
Gat.e	Min. **GatPoly** area (µm²)	**0.09**
Gat.f	45-degree and 90-degree angles for **GatPoly** on **Activ** area are not allowed	
Gat.g	Min. **GatPoly** width for 45-degree bent gates (on field oxide) if the bend **GatPoly** length is > 0.39 µm	**0.16**

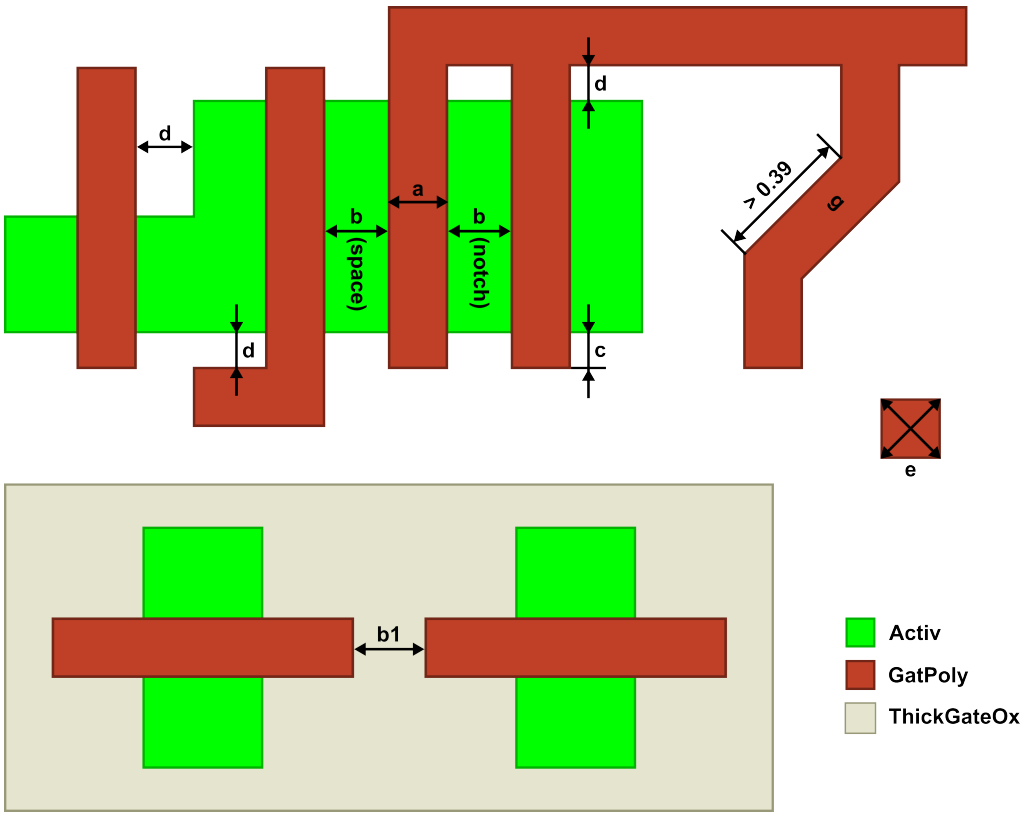

Figure 3.3: GatPoly dimensions

3.9 GatPoly:filler

GatPoly:filler patterns are required in order to improve wafer homogeneity in CMP process steps.

Rule	Description	Value
GFil.a	Max. **GatPoly:filler** width	**5.0**
GFil.b	Min. **GatPoly:filler** width	**0.7**
GFil.c	Min. **GatPoly:filler** space	**0.8**
GFil.d	Min. **GatPoly:filler** space to **Activ**, **GatPoly**, **Cont**, **pSD**, **nSD:block**, **SalBlock**	**1.1**
GFil.e	Min. **GatPoly:filler** space to **NWell**, **nBuLay**	**1.1**
GFil.f	Min. **GatPoly:filler** space to **TRANS**	**1.1**
GFil.g	Min. global **GatPoly** density [%]	**15.0**
GFil.i	Max. **GatPoly.nofill** area (µm²)	**400 x 400**
GFil.j	Min. **GatPoly.nofill** space	**20.0**

Notes

1. **GatPoly:nofill** layer can be used for filler pattern exclusion within specific device areas such as inductors or transformers.
2. Default filler size 5 x 1.4 µm2 and 3.6 µm spacing with an x-offset of 0 µm and an y-offset of 2.5 µm is recommended with pattern density of approx. 28%. Scripts, provided with IHP design kits, generate **GatPoly:filler** together with **Activ:filler**. Both fillers are laying above each other. Further recommended minimum spacing to already existing **GatPoly:filler** is 10 µm.

3.10 pSD

Rule	Description	Value
pSD.a	Min. **pSD** width	**0.31**
pSD.b	Min. **pSD** space or notch (Note 1)	**0.31**
pSD.c	Min. **pSD** enclosure of **P+Activ** in **NWell**	**0.18**
pSD.c1	Min. **pSD** enclosure of **P+Activ** in **PWell**	**0.03**
pSD.d	Min. **pSD** space to unrelated **N+Activ** in **PWell**	**0.18**
pSD.d1	Min. **pSD** space to **N+Activ** in **NWell**	**0.03**
pSD.e	Min. **pSD** overlap of **Activ** at one position when forming abutted substrate tie (Note 2)	**0.3**
pSD.f	Min. **Activ** extension over **pSD** at one position when forming abutted **NWell** tie (Note 2)	**0.3**
pSD.g	Min. **N+Activ** or **P+Activ** area (µm²) when forming abutted tie (Note 2)	**0.09**
pSD.i	Min. **pSD** enclosure of PFET gate (thin gate oxide)	**0.3**
pSD.i1	Min. **pSD** enclosure of PFET gate (thick gate oxide)	**0.4**
pSD.j	Min. **pSD** enclosure of NFET gate (thin gate oxide)	**0.3**
pSD.j1	Min. **pSD** enclosure of NFET gate (thick gate oxide)	**0.4**
pSD.k	Min. **pSD** area (µm²)	**0.25**
pSD.l	Min. **pSD** enclosed area (µm²)	**0.25**
pSD.m	Min. **pSD** space to n-type poly resistors	**0.18**
pSD.n	Min. **pSD** enclosure of p-type poly resistors	**0.18**

Notes

1. **pSD** regions separated by less than this value will be merged.
2. These rules are for abutted ties: An electrical connection from P+Activ to NWell tie (or N+ Activ to P-sub tie) is made through the source/drain silicide. For a good electrical connection rule pSD.g is important together with rule pSD.e or pSD.f (see figure below).

3.11 nSD:block

nSD:block layer is used to generate regions where n+ S/D implants are blocked. The final mask data **nSD** are generated by: nSD: = NOT (pSD OR nSD:block).

Rule	Description	Value
nSDB.a	Min. **nSD:block** width	**0.31**
nSDB.b	Min. **nSD:block** space or notch	**0.31**
nSDB.c	Min. **nSD:block** space to unrelated **pSD**	**0.31**
nSDB.d	Min. **nSD:block** overlap of **pSD** (Note 1)	**0.0**
nSDB.e	Min. **nSD:block** space to **Cont** (Note 2)	**0.0**

Notes

1. **nSD:block** and **pSD** are allowed to overlap or to be line-on-line.
2. **nSD:block** and **Cont** do not overlap.

3.12 EXTBlock

EXTBlock layer is used to generate regions where all tip and halo implants are blocked.

Rule	Description	Value
EXT.a	Min. **EXTBlock** width	**0.31**
EXT.b	Min. **EXTBlock** space or notch	**0.31**
EXT.c	Min. **EXTBlock** space to **pSD**	**0.31**

3.13 SalBlock

SalBlock is used to block salicidation of **GatPoly** or source/drain areas.

Rule	Description	Value
Sal.a	Min. **SalBlock** width	**0.42**
Sal.b	Min. **SalBlock** space or notch	**0.42**
Sal.c	Min. **SalBlock** extension over **Activ** or **GatPoly**	**0.2**
Sal.d	Min. **SalBlock** space to unrelated **Activ** or **GatPoly**	**0.2**
Sal.d	Min. **SalBlock** space to **Cont**	**0.2**

3.14 Cont

Rule	Description	Value
Cnt.a	Min. and max. **Cont** width	**0.16**
Cnt.b	Min. **Cont** space	**0.18**
Cnt.b1	Min. **Cont** space in a contact array of more than 4 rows and more then 4 columns (Note 1)	**0.2**
Cnt.c	Min. **Activ** enclosure of **Cont**	**0.07**
Cnt.d	Min. **GatPoly** enclosure of **Cont**	**0.07**
Cnt.e	Min. **Cont** on **GatPoly** space to **Activ**	**0.14**
Cnt.f	Min. **Cont** on **Activ** space to **GatPoly**	**0.11**
Cnt.g	**Cont** must be within **Activ** or **GatPoly**	
Cnt.g1	Min. **pSD** space to **Cont** on **nSD-Activ**	**0.09**
Cnt.g2	Min. **pSD** overlap of **Cont** on **pSD-Activ**	**0.09**
Cnt.h	**Cont** must be covered with **Metal1**	
Cnt.j	**Cont** on **GatPoly** over **Activ** is not allowed	

Notes

1. Cnt.b1 is only required in one direction. The distance of the other direction must be at least Cnt.b.

3.15 ContBar

Any **Cont** shape not being a square with 0.16 µm x 0.16 µm width is considered a **ContBar**.

Rule	Description	Value
CntB.a	Min. and max. **ContBar** width	**0.16**
CntB.a1	Min. **ContBar** length	**0.34**
CntB.b	Min. **ContBar** space	**0.28**
CntB.b1	Min. **ContBar** space with common run > 5 µm	**0.36**
CntB.b2	Min. **ContBar** space to **Cont**	**0.22**
CntB.c	Min. **Activ** enclosure of **ContBar**	**0.07**
CntB.d	Min. **GatPoly** enclosure of **ContBar**	**0.07**
CntB.e	Min. **ContBar** on **GatPoly** space to **Activ**	**0.14**
CntB.f	Min. **ContBar** on **Activ** space to **GatPoly**	**0.11**
CntB.g	**ContBar** must be within **Activ** or **GatPoly**	
CntB.g1	Min. **pSD** space to **ContBar** on **nSD-Activ**	**0.09**
CntB.g1	Min. **pSD** overlap of **ContBar** on **pSD-Activ**	**0.09**
CntB.h	**ContBar** must be covered with **Metal1**	
CntB.h1	Min. **Metal1** enclosure of **ContBar**	**0.05**
CntB.j	**ContBar** on **GatPoly** over **Activ** is not allowed	

3.16 Metal1

Rule	Description	Value
M1.a	Min. **Metal1** width	**0.16**
M1.b	Min. **Metal1** space or notch	**0.18**
M1.c	Min. **Metal1** enclosure of **Cont**	**0.0**
M1.c1	Min. **Metal1** endcap enclosure of **Cont** (Note 1)	**0.05**
M1.d	Min. **Metal1** area (µm²)	**0.09**
M1.e	Min. space of **Metal1** lines if, at least one line is wider than 0.3 µm and the parallel run is more than 1.0 µm	**0.22**
M1.f	Min. space of **Metal1** lines if, at least one line is wider than 10.0 µm and the parallel run is more than 10.0 µm	**0.6**
M1.g	Min. 45-degree bent **Metal1** width if the bent metal length is > 0.5 µm	**0.2**
M1.i	Min. space of **Metal1** lines of which at least one is bent by 45-degree	**0.2**
M1.j	Min. global **Metal1** density [%]	**35.0**
M1.k	Max. global **Metal1** density [%]	**60.0**

Notes

1. For contacts at **Metal1** corners at least one side must be treated as an endcap and for the other sides rule M1.c can be applied.

3.17 Metal(n=2-5)

Rule	Description	Value
Mn.a	Min. **Metal(n)** width	**0.2**
Mn.b	Min. **Metal(n)** space or notch	**0.21**
Mn.c	Min. **Metal(n)** enclosure of **Via(n-1)**	**0.005**
Mn.c1	Min. **Metal(n)** endcap enclosure of **Via(n-1)** (Note 1)	**0.05**
Mn.d	Min. **Metal(n)** area (µm²)	**0.144**
Mn.e	Min. space of **Metal(n)** lines if, at least one line is wider than 0.39 µm and the parallel run is more than 1.0 µm	**0.24**
Mn.f	Min. space of **Metal(n)** lines if, at least one line is wider than 10.0 µm and the parallel run is more than 10.0 µm	**0.6**
Mn.g	Min. 45-degree bent **Metal(n)** width if the bent metal length is > 0.5 µm	**0.24**
Mn.i	Min. space of **Metal(n)** lines of which at least one is bent by 45-degree	**0.24**
Mn.j	Min. global **Metal(n)** density [%]	**35.0**
Mn.k	Max. global **Metal(n)** density [%]	**60.0**

Notes

1. For vias at **Metal(n)** corners at least one side must be treated as an endcap and for the other sides rule Mn.c can be applied.

3.18 Metal(n=1-5):filler

Metal(n):filler pattern are required in order to reduce layout sensitivity in metal etch and CMP process steps.

Rule	Description	Value
MFil.a1	Min. **Metal(n):filler** width	**1.0**
MFil.a2	Max. **Metal(n):filler** width	**5.0**
MFil.b	Min. **Metal(n):filler** space	**0.6**
MFil.c	Min. **Metal(n):filler** space to **Metal(n)**	**0.42**
MFil.d	Min. **Metal(n):filler** space to **TRANS**	**1.0**
MFil.h	Min. **Metal(n)** and **Metal(n):filler** coverage ratio for any 800 x 800 µm² chip area [%]	**25.0**
MFil.k	Max. **Metal(n)** and **Metal(n):filler** coverage ratio for any 800 x 800 µm² chip area [%]	**75.0**

Notes

1. A smaller coverage or larger filler exclusion area leads to smaller metal lines and higher sheet resistance. Sheet resistance of minimum width **Metal(n)** lines is increasing by 10% if metal coverage is lower than 30%.
2. **Metal(n):filler** are automatically generated during the tape out procedure, For sensitive areas of the circuit, designers should exclude **Metal(n):filler** using the **Metal(n):nofill** or **NoMetFiller** exclusion layer, or should place defined metal structures to prevent metal fill.
3. Default filler size 5 x 2 µm² and 1.2 µm spacing with an offset of 3.1 µm is recommended with pattern density of approx. 50%.

3.19 Via1

Rule	Description	Value
V1.a	Min. and max. **Via1** width	**0.19**
V1.b	Min. **Via1** space	**0.22**
V1.b1	Min. **Via1** space in an array of more than 3 rows and more then 3 columns (Note 1)	**0.29**
V1.c	Min. **Metal1** enclosure of **Via1**	**0.01**
V1.c1	Min. **Metal1** endcap enclosure of **Via1** (Note 2)	**0.05**

Notes

1. V1.b1 is only required in one direction. The distance of the other direction must be at least V1.b.
2. For **Via1** at **Metal1** corners at least one side must be treated as an endcap and for the other sides rule V1.c can be applied.

3.20 Via(n=2-4)

Rule	Description	Value
Vn.a	Min. and max. **Via(n)** width	**0.19**
Vn.b	Min. **Via(n)** space	**0.22**
Vn.b1	Min. **Via(n)** space in an array of more than 3 rows and more then 3 columns (Note 1)	**0.29**
Vn.c	Min. **Metal(n)** enclosure of **Via(n)**	**0.005**
Vn.c1	Min. **Metal(n)** endcap enclosure of **Via(n)** (Note 2)	**0.05**

Notes

1. Vn.b1 is only required in one direction. The distance of the other direction must be at least Vn.b.
2. For **Via(n)** at **Metal(n)** corners at least one side must be treated as an endcap and for the other sides rule Vn.c can be applied.

3.21 TopVia1

Rule	Description	Value
TV1.a	Min. and max. **TopVia1** width	**0.42**
TV1.b	Min. **TopVia1** space	**0.42**
TV1.c	Min. **Metal5** enclosure of **TopVia1**	**0.1**
TV1.d	Min. **TopMetal1** enclosure of **TopVia1**	**0.42**

3.22 TopMetal1

Rule	Description	Value
TM1.a	Min. **TopMetal1** width	**1.64**
TM1.b	Min. **TopMetal1** space or notch	**1.64**
TM1.c	Min. global **TopMetal1** density [%]	**25.0**
TM1.d	Max. global **TopMetal1** density [%]	**70.0**

3.23 TopMetal1:filler

Rule	Description	Value
TM1Fil.a	Min. **TopMetal1:filler** width	**5.0**
TM1Fil.a1	Max. **TopMetal1:filler** width	**10.0**
TM1Fil.b	Min. **TopMetal1:filler** space	**3.0**
TM1Fil.c	Min. **TopMetal1:filler** space to **TopMetal1**	**3.0**
TM1Fil.d	Min. **TopMetal1:filler** space to **TRANS**	**4.9**

Notes

1. Default filler size 5 x 10 µm2 and 3 µm spacing with an offset of 7.5 µm is recommended with pattern density of approx. 50%

3.24 TopVia2

Rule	Description	Value
TV2.a	Min. and max. **TopVia2** width	**0.9**
TV2.b	Min. **TopVia2** space	**1.06**
TV2.c	Min. **TopMetal1** enclosure of **TopVia2**	**0.5**
TV2.d	Min. **TopMetal2** enclosure of **TopVia2**	**0.5**

3.25 TopMetal2

Rule	Description	Value
TM2.a	Min. **TopMetal2** width	**2.0**
TM2.b	Min. **TopMetal2** space or notch	**2.0**
TM2.bR	Min. space of **TopMetal2** lines if, at least one line is wider than 5.0 µm and the parallel run is more than 50.0 µm (Note 1, 2)	**5.0**
TM2.c	Min. global **TopMetal2** density [%]	**25.0**
TM2.d	Max. global **TopMetal2** density [%]	**70.0**

Notes

1. Violations can cause potential issues with TAPEs during backgrinding.
2. Not checked within **IND** regions.

3.26 TopMetal2:filler

Rule	Description	Value
TM2Fil.a	Min. **TopMetal2:filler** width	**5.0**
TM2Fil.a1	Max. **TopMetal2:filler** width	**10.0**
TM2Fil.b	Min. **TopMetal2:filler** space	**3.0**
TM2Fil.c	Min. **TopMetal2:filler** space to **TopMetal2**	**3.0**
TM2Fil.d	Min. **TopMetal2:filler** space to **TRANS**	**4.9**

Notes

1. Default filler size 5 x 10 µm2 and 3 µm spacing with an offset of 7.5 µm is recommended with pattern density of approx. 50%

3.27 Passiv

Rule	Description	Value
Pas.a	Min. **Passiv** width	**2.1**
Pas.b	Min. **Passiv** space or notch	**3.5**
Pas.c	Min. **TopMetal2** enclosure of **Passiv** (Note 1)	**2.1**

Notes

1. Not checked outside of sealring (edge-seal-passive)

4 Device layout rules

4.1 Pad dimensions

Device recognition: Pad = (**Passiv** + **Passiv:sbump** + **Passiv:pillar**) + **dfpad**

Pad rules are tested only within **dfpad** recognition layer. Pad rules are only tested on metal structures which are on same net as **TopMetal2**. The following design rules must be also applied to solder bump pads and Cu pillar pads. Please be aware that within a pad, the minimum passive design rules must also be satisfied.

Rule	Description	Value
Pad.aR	Min. recommended **Pad** width	**30.0**
Pad.a1	Max. **Pad** width	**150.0**
Pad.bR	Min. recommended **Pad** space	**8.4**
Pad.d	Min. **Pad** space to **EdgeSeal**	**7.5**
Pad.dR	Min. recommended **Pad** to **EdgeSeal** space (Note 1)	**25.0**
Pad.d1R	Min. recommended **Pad** to **Activ** (inside chip area) space	**11.2**
Pad.eR	Min. recommended **Metal(n)**, **TopMetal1**, **TopMetal2** exit width	**7.0**
Pad.fR	Min. recommended **Metal(n)**, **TopMetal1**, **TopMetal2** exit length	**7.0**
Pad.gR	**TopMetal1** (within **dfpad**) enclosure of **TopVia2**	**1.4**
Pad.i	**dfpad** without **TopMetal2** not allowed	
Pad.jR	No devices under **Pad** allowed (Note 2)	
Pad.kR	**TopVia2** under **Pad** not allowed (Note 3)	

Notes

1. Distance of **Pad** opening to **EdgeSeal** strongly depends on bonding procedure. For Flip Chip or manual bonding a bigger distance may be required. We strongly recommend 25 µm distance for wedge-wedge wire bonding.
2. Components under pads can be damaged by mechanical stress.
3. **TopVia2** may be damaged during packaging process, we recommend not to use them below **Passiv**.

4.1.1 Solder bump rules

Device recognition: SBumpPad = **Passiv:sbump** + **dfpad**

These rules are valid within pads used for solder bumping and flip chip assembling. These pad rules are valid for 60 µm passive opening and 80 µm bump ball size. Bump ball standard is PacTech SAC305 (SnAgCu).

For different geometries refer to design rule manual of our partner PacTech or the design rule manual of your specific bumping provider.

Rule	Description	Value
Padb.a	**SBumpPad** size	**60.0**
Padb.b	Min. **SBumpPad** space	**70.0**
Padb.c	Min. **TopMetal2** (within **dfpad**) enclosure of **SBumpPad**	**10.0**
Padb.d	Min. **SBumpPad** space to **EdgeSeal**	**50.0**
Padb.e	Min. **SBumpPad** pitch (Note 1)	**130.0**
Padb.f	Allowed passivation opening shape (Note 1, 2, 3)	**Octagon Circle**

Notes

1. This rule is not checked during DRC.
2. We recommend to use Solder Bump option in Pcell provided in the PDK.
3. Underlying **TopMetal2** may have a different shape.

4.1.2 Copper pillar rules

Device recognition: CuPillarPad = **Passiv:pillar** + **dfpad**

These rules are valid within pads used for assembly with copper pillars. The given pad rules are valid for a number of different geometries offered by our partner PacTech given in table 4.1.

Important: Please note that pad opening may have an impact on final testing. If the passivation openings are too small, wafer-level testing may be prevented because the pad metal cannot be sufficiently contacted.

Table 4.1: Valid pad geometries and design rules for Cu pillars.

Passiv opening	35	40	45	**Padc.a**
Opening spacing	40	40	50	**Padc.b**
Opening enclosure	7.5	7.5	7.5	**Padc.c**
CuPillarPad pitch	75	80	95	**Padc.e**
Cu pillar height	50 ± 7	55 ± 7	65 ± 7	
Cu pillar diameter	44 ± 3	49 ± 3	54 ± 3	
Cu height (A)	28 ± 2	32 ± 2	42 ± 2	
SnAg height* (B)	16 ± 1	16 ± 1	19 ± 2	

Notes

1. Passivation openings highlighted in green are suited for on-wafer measurements
2. Pads with passivation openings of 45 µm and 55 µm are suited for PCB applications. Minimum recommended pitch 250 µm; recommended standard pitch 500 µm.

* Thickness of optional SnAg cap after reflow at peak temp 260 degree C would be higher than that of after plating/ before reflow in the factor of 1.4 - 1.7, depending on the SnAg height as well.

For different geometries than listed in table 4.1, refer to the design rule manual of our partner PacTech or the design rule manual of your specific bumping provider.

The following table defines design rules for PacTech's copper pillar option with minimum passivation opening, copper pillar height and copper pillar pitch.

Rule	**Description**	**Value**
Padc.a	**CuPillarPad** size	**Table 4.1**
Padc.b	Min. **CuPillarPad** space	**Table 4.1**
Padc.c	Min. **TopMetal2** (within **dfpad**) enclosure of **CuPillarPad**	**Table 4.1**
Padc.d	Min. **CuPillarPad** space to **EdgeSeal**	**30.0**
Padc.e	Min. **CuPillarPad** pitch (Note 1)	**Table 4.1**
Padc.f	Allowed passivation opening shape (Note 1, 2, 3)	**Circle**

Notes

1. This rule is not checked during DRC.
2. We recommend to use Cu Pillar option in Pcell provided in the PDK.
3. Underlying **TopMetal2** may have a different shape.

4.2 EdgeSeal

Device recognition: EdgeSeal

The edge seal (chip guard ring) is a complete unbroken ring around the active chip area. Refer to Fig. xx for the edge seal shape at the chip level.

Rule	Description	Value
Seal.a	Min. **EdgeSeal-Activ**, **EdgeSeal-pSD**, **EdgeSeal-Metal(n=1-5)**, **EdgeSeal-TopMetal1**, **EdgeSeal-TopMetal2** width	**3.5**
Seal.b	Min. **Activ** space to **EdgeSeal-Activ**, **EdgeSeal-pSD**, **EdgeSeal-Metal(n=1-5)**, **EdgeSeal-TopMetal1**, **EdgeSeal-TopMetal2**	**4.9**
Seal.c	**EdgeSeal-Cont** ring width (Note 1)	**0.16**
Seal.c1	**EdgeSeal-Via(n=1-4)** ring width (Note 1)	**0.19**
Seal.c2	**EdgeSeal-TopVia1** ring width (Note 1)	**0.42**
Seal.c3	**EdgeSeal-TopVia2** ring width (Note 1)	**0.9**
Seal.d	Min. **EdgeSeal-Activ** enclosure of **EdgeSeal-Cont**, **EdgeSeal-Metal(n=1-5)**, **EdgeSeal-TopMetal1**, **EdgeSeal-TopMetal2** ring	**1.3**
Seal.e	Min. **EdgeSeal-Passiv** width	**4.2**
Seal.f	Min. **EdgeSeal-Passiv** space to **EdgeSeal-Activ**, **EdgeSeal-Metal(n=1-5)**, **EdgeSeal-TopMetal1**, **EdgeSeal-TopMetal2** (Note 2)	**1.0**
Seal.k	Min. **EdgeSeal** 45-degree corner length (Note 3)	**21.0**
Seal.l	No structures outside sealring boundary allowed	

Notes

1. Corresponding standard metal and via rules are not checked within **EdgeSeal** layer.
2. **EdgeSeal-Passiv** has to be outside of the sealring.
3. Not checked during DRC.
4. Fig. xx j - represents distance between Edge Seal and border filler ring (30 µm) and passive opening. Cutting edge is around 20-40 µm outside of Edge Seal for MPW Foundry dices.

4.3 MIM

Metal-Insulator-Metal (MIM) capacitors are formed by a thin dielectric layer and conductor placed between **TopMetal1** and **Metal5**.

Device recognition: MIM capacitor = **MIM** + **Metal5**

Within **MIM** capacitor layer **Vmim** can be used instead of **TopVia1**.

Background: Most EDA tools cannot distinguish between interconnects and electrical components which are formed by the same conductive layers. Within the MIM device, TopVia1 can be replaced with Vmim to prevent false short circuit detection.

Rule	Description	Value
MIM.a	Min. **MIM** width	**1.14**
MIM.b	Min. **MIM** space	**0.6**
MIM.c	Min. **Metal5** enclosure of **MIM**	**0.6**
MIM.d	Min. **MIM** enclosure of **TopVia1**	**0.36**
MIM.e	Min. **TopMetal1** space to **MIM**	**0.6**
MIM.f	Min. **MIM** area per MIM device (µm²)	**1.3**
MIM.g	Max. **MIM** area per MIM device (µm²)	**5625.0**
MIM.gR	Max. recommended total **MIM** area per chip (µm²)	**174800.0**
MIM.h	**TopVia1** must be over **MIM**	
MIM.i	**Via4** under **MIM** is allowed	

Yield Enhancement Guideline: Wherever MIM-Metal5 is tied to Activ (nSD/pSD), use TopVia1 and TopMetal1 to perform the connection. See Fig. xx.

4.4 Rsil

Device recognition: Rsil = **RES** + **GatPoly**

Rsil represents the salicided n+ doped **GatPoly** resistor.

Rule	Description	Value
Rsil.a	Min. **GatPoly** width	**0.5**
Rsil.b	Min. **RES** space to **Cont**	**0.12**
Rsil.c	Min. **RES** extension over **GatPoly**	**0.0**
Rsil.d	Min. **pSD** space to **GatPoly**	**0.18**
Rsil.e	Min. **EXTBlock** space to **GatPoly**	**0.18**
Rsil.f	Min. **RES** length	**0.5**

Notes

1. **RES** represents the resistor definition layer and is required for back annotation.

4.5 Rppd

Device recognition: Rppd = **SalBlock** + **GatPoly** + **pSD**

Rppd represents the unsalicided p+ doped **GatPoly** resistor.

Rule	Description	Value
Rppd.a	Min. **GatPoly** width	**0.5**
Rppd.b	Min. **pSD** enclosure of **GatPoly**	**0.18**
Rppd.c	Min. and max. **SalBlock** space to **Cont**	**0.2**
Rppd.d	Min. **EXTBlock** enclosure of **GatPoly**	**0.18**
Rppd.e	Min. **SalBlock** length	**0.5**

4.6 Rhigh

Device recognition: Rhigh = **SalBlock** + **GatPoly** + **pSD** + **nSD**

Rhigh represents an unsalicided partial compensated low n-doped **GatPoly** resistor.

Rule	Description	Value
Rhi.a	Min. **GatPoly** width	**0.5**
Rhi.b	**pSD** and **nSD** are identical (Note 1)	
Rhi.c	Min. **pSD** and **nSD** enclosure of **GatPoly**	**0.18**
Rhi.d	Min. and max. **SalBlock** space to **Cont**	**0.2**
Rhi.e	Min. **EXTBlock** enclosure of **GatPoly**	**0.18**
Rhi.f	Min. **SalBlock** length	**0.5**

Notes

1. Use **nSD** only within Rhigh resistor device.

4.7 nmosi and nmosiHV

Device recognition: nmosi is recognized as an nmos device. The difference of nmosi and nmosiHV is given by **ThickGateOx**. There are special device construction rules for this substrate isolated nmos device. These rules will only be tested inside a closed ring of **NWell** AND **nBuLay**.

Rule	Description	Value
nmosi.b	Min. **nBuLay** enclosure of **Iso-PWell-Activ** (Note 1)	**1.24**
nmosi.c	Min. **NWell** space to **Iso-PWell-Activ**	**0.39**
nmosi.d	Min. **NWell-nBuLay** width forming an unbroken ring around any **Iso-PWell-Activ** (Note 2)	**0.62**
nmosi.e1	A separate Iso-PWell contact unabutted to a nmosi device is not allowed	
nmosi.e2	nmosi unabutted to an Iso-PWell-Activ tie is not allowed	
nmosi.f	Min. **nSD:block** width to separate ptap in nmosi	**0.62**
nmosi.g	Min. **SalBlock** overlap of **nSD:block** over **Activ**	**0.15**

Notes

1. Iso-PWell-Activ = **Activ** AND **nBuLay** AND **PWell**
2. NWell-nBuLay = **NWell** AND **nBuLay**
3. NWell which is used as a ring for isolated PWell and carries active p-mos devices has to be carefully layed out in order to prevent latch up.
4. Recommendation: 1 mimimum PWell contact per 50 µm2. To calculate voltage drops in PWell consider an average sheet resistance of 3 kΩ.
5. Recommendation: Use ptapsb Pcell to ensure proper isolated PWell connection. An example can be found in Cadence PDK's example library.

4.8 isolbox

Device recognition: isolbox = TEXT “isolbox” within (**NWell** enclosed by **Recog:diode**)

We recommend to use only layouts offered in PCELL by IHP. The pins ”isosub” and ”bn” are not part of the pcell and have to pe placed manually to give designer more flexibility.

PCell parameter	Model parameter	Description	Min	Value	Max
W		Outer **NWell** width	DRC		
L		Outer **NWell** length	DRC		
PWellBlock width	XD	**PWell:block** ring width	DRC		
NWell width		**NWell** ring width		1.05	
	PW	Isolated **PWell** perimeter	DRC		
	AW	Isolated **PWell** area	DRC		
	PB	Outer **NWell** perimeter	DRC		
	AB	N-doped area (**NWell** and **nBuLay**)	DRC		

4.9 Schottky diode

Device recognition: schottky_nbl1 = **ContBar** enclosed by (**SalBlock** and **nSD:block** and **PWell:block** and not **nBuLay**)

The following rules do not apply: NW.c1, NW.e1, PWB.f1, CntB.a, LU.d

Rule	Description	Value
Sdiod.a	Min. and max. **PWell:block** enclosure of **ContBar**	**0.25**
Sdiod.b	Min. and max. **nSD:block** enclosure of **ContBar**	**0.4**
Sdiod.c	Min. and max. **SalBlock** enclosure of **ContBar**	**0.45**
Sdiod.d	Min. and max. **ContBar** width inside **nBuLay**	**0.3**
Sdiod.e	Min. and max. **ContBar** length inside **nBuLay**	**1.0**

4.10 ESD protection devices

For ESD protection of the chip, special clamp devices are provided. Please refer to the ESD documents for details about protection level. Also note that it is recommended to have I/O MOS devices with channel length of at least 0.36 µm.

4.10.1 nmoscl_2

Clamp device for limiting supply voltage.

Device recognition: nmoscl_2 = TEXT “nmoscl_2” within **Recog:esd**

Following rules do not apply: nmosi.e, Gat.a3

4.10.2 nmoscl_4

Clamp device for limiting supply voltage.

Device recognition: nmoscl_4 = TEXT “nmoscl_4” within **Recog:esd**

Following rules do not apply: nmosi.e, Gat.a3

4.10.3 scr1

Device recognition: scr1 = TEXT “scr1” within **Recog:esd**

Following rules do not apply: nmosi.c, nmosi.g, LU.d, Gat.a

5 Special rules

5.1 Grid rules

- All rules are defined in microns [µm] by default if there is no other unit mentioned
- All features are on a drawing grid of 5 nm (0.005 µm)
- Shapes with acute angles <87° are not allowed on any layer
- Following layers are only allowed on 90, 180 degree angles: Cont, Via1, Via2, Via3, Via4, TopVia1, TopVia2
- Following layers are only allowed on 90, 135, 180, 225, and 270 degree angles: GatPoly, Activ, Metal1, Metal2, Metal3, Metal4, Metal5, TopMetal1, TopMetal2
- Self-intersecting polygons must be avoided
- Design elements, which are snapped to grid must not violate any geometries in this document.

There are several layers which are not considered for mask generation. Offgrid and angle checks are not applied on the following layers: DigiBnd, RES, SRAM, IND, OPCBlk, EdgeSeal, dfpad, HeatTrans, HeatRes, DigiSub, NoDRC, TEXT, RadHard, Flash, SMOS, Scribe, Recog, NoRCX, NoMetFiller

5.2 Antenna rules

Antenna Rules are not checked by default. Antenna rule checking must be switched on separately.

Gate = **GatPoly** over **Activ**

Rule	Description	Value
Ant.a	Max. ratio of **GatPoly** over field oxide area to connected **Gate** area	**200.0**
Ant.b	Max. ratio of cumulative metal area (from **Metal1** to **TopMetal2**) to connected **Gate** area (without protection diode)	**200.0**
Ant.c	Max. ratio of **Cont** area to connected **Gate** area	**20.0**
Ant.d	Max. ratio of cumulative via area (from **Via1** to **TopVia2**) to connected **Gate** area (without protection diode)	**20.0**
Ant.e	Max. ratio of cumulative metal area (from **Metal1** to **TopMetal2**) to connected **Gate** area (with protection diode)	**20000.0**
Ant.f	Max. ratio of cumulative via area (from **Via1** to **TopVia2**) to connected **Gate** area (with protection diode)	**500.0**
Ant.g	Size of protection diode (µm²)	**0.16**

Notes

1. Ant.a to Ant.d are determined by using gate leakage current (shift of 10% for nominal devices) as failure criterion.
2. The rules apply for both types of oxide.
3. Vn_area = cumulative area Cont, Via1 to TopVia2
4. Via_area = cumulative area Via1 to TopVia2
5. PDarea (µm²) = 0.02 x (Vn_area / (GatPoly over Activ)_area)

Recommendations

- To get DRC clean layouts it is recommended to connect the antenna node to the output of the driver at low metal level to reduce the antenna area or connect the antenna node to a diode.
- To get DRC clean layouts it is recommended to use stacked vias to connect large metal or via areas as shown in Figure xx.
- To protect the gate of an isolated nMOS transistors it is recommended to place the antenna-protection diode in a separate (non isolated) p-body region.
- For applications which are especially sensitive to Vt variation or mismatch (sense amplifers, certain analog circuits, etc.), each gate should be tied directly to an nSD/PWell or pSD/NWell diode in Metal1.

5.3 Latch-up guidelines

5.3.1 Latch-up protection on output buffers

1. Connect source of NMOS and PMOS devices to VSS and VDD, respectively.
2. Connect drain of NMOS and PMOS devices directly to the output pad.
3. Place guard rings (VSS, VDD ties) around any NMOS and PMOS devices, which are directly tied to a pad.
4. Double guard rings (N-Well isolator and P+ isolator) should be inserted between n-channel and p-channel output buffers.
5. Double guard rings (N-Well isolator and P+ isolator) should be inserted between output buffers and internal circuit area.

5.3.2 Additional rules for subtrate and NWell ties

Rule	Description	Value
LU.a	Max. space from any portion of **P+Activ** inside **NWell** to an **nSD-NWell** tie	**20.0**
LU.b	Max. space from any portion of **N+Activ** inside **PWell** to an **pSD-PWell** tie	**20.0**
LU.c	Max. extention of an abutted **NWell** tie beyond **Cont**	**6.0**
LU.c1	Max. extention of a substrate tie beyond **Cont**	**6.0**
LU.d	Max. extention of **NWell** tie **Activ** tie beyond **Cont**	**6.0**
LU.d1	Max. extention of an substrate tie **Activ** beyond **Cont**	**6.0**

5.4 Metal slits

Metal stands for all metal layers (**Metal(n=1-5)**, **TopMetal1** and **TopMetal2**).

Metal = **Metal(n=1-5)** + **TopMetal1** + **TopMetal2**

Rule	Description	Value
Slt.a	Min. **Metal:slit** width	**2.8**
Slt.b	Max. **Metal:slit** width	**20.0**
Slt.c	Max. **Metal** width without requiring a slit	**30.0**
Slt.e	No slits required on bond pads	
Slt.e1	No slits required on **MIM**	
Slt.f	Min. **Metal** enclosure of **Metal:slit**	**1.0**
Slt.g	Min. **Metal5:slit** and **TopMetal1:slit** space to **MIM**	**0.6**
Slt.h1	Min. **Metal1:slit** space to **Cont** and **Via1**	**0.3**
Slt.h2	Min. **Metal(n):slit** space to **Via(n-1)** and **Via(n)**	**0.3**
Slt.h3	Min. **TopMetal1:slit** space to **TopVia1** and **TopVia2**	**1.0**
Slt.h4	Min. **TopMetal2:slit** space to **TopVia2**	**1.0**
Slt.i	Min. **Metal:slit** density for any **Metal** plate bigger than 35 µm x 35 µm [%]	**6.0**

5.5 IND layer

The layer **IND** is a recognition layer for inductors and transmission lines. Because this is a device recognition layer LVS and parasitic extraction will not work within this layer for metal and GatPoly lines. Within this layer there is by default no filler generation.

Following rules will not be checked within this layer: Metal slit rules, AFil.gR, AFil.i, MFil.hR, MFil.g

5.6 Layer generation

tbd.

5.7 NoDRC

This layer can be used for non-design rule compliant structures such as logos, specific test elements, etc. There is no filler generation within **NoDRC**. Each of these elements needs a written waiver from the foundry in order to make sure it is manufacturable.

5.8 Pin layer rules

Circuit designers should use only drawing purpose 0 (data types) for layouts. Only exception is pin purpose 2 for symbolic pins. Data type 2 (purpose pin) is used for symbolic connectivity information. Pin areas must be fully covered by drawing. These rules are testing this because Pin areas are not used for mask generation.

Rule	Description	Value
Pin.a	Min. **Activ** enclosure of **Activ:pin**	**0.0**
Pin.b	Min. **GatPoly** enclosure of **GatPoly:pin**	**0.0**
Pin.e	Min. **Metal1** enclosure of **Metal1:pin**	**0.0**
Pin.f	Min. **Metal(n=2-5)** enclosure of **Metal(n=2-5):pin**	**0.0**
Pin.g	Min. **TopMetal1** enclosure of **TopMetal1:pin**	**0.0**
Pin.h	Min. **TopMetal2** enclosure of **TopMetal2:pin**	**0.0**

5.9 Forbidden layers

Following layers are forbidden in designs submitted for all 0.13 µm technologies.

Layer name	Purpose	GDS Number	GDS Datatype
BiWind	drawn	3	0
PEmWind	drawn	11	0
BasPoly	drawn	13	0
DeepCo	drawn	35	0
PEmPoly	drawn	53	0
EmPoly	gen./drawn	53	0
LDMOS	drawn	57	0
PBiWind	drawn	58	0
Flash	drawn	71	0
ColWind	drawn	139	0

6 Bipolar design rules

Device recognition: For device recognition **TRANS** layer in combination with TEXT labels and layer combinations are used for device recognition.

Bipolar design rules are not disclosed due to IP reasons. Additional layers will be added during the tape out procedure for mask generation. Changing the given layouts may result in catastrophic device malfunction. The IHP library provides a number of predefined devices shown in the follow sections. Do not modify these layouts/abstracts.

Strict design rule: Do not flatten the HBT layout cells and do not place any shapes, except metal for connections, in bipolar **TRANS** regions. Use pins on given metals to connect base, emitter and collector with corresponding metal shapes. Any modification in bipolar transistor results in non-working device.

6.1 Pre-defined transistor layouts

Device	Min. emitter size (µm²)	Parameter	Comment
npn13G2	0.07 x 0.9	le 0.9u, Nx 1..10, Nx x (0.07u x le)	le for scaling of emitter length, Nx for scaling number of emitters in a row
npn13G2L	0.07 x 1.0	le 1.0u..2.5u, Nx 1..4, Nx x (0.07u x le)	le for scaling of emitter length, Nx for scaling number of emitters in a row
npn13G2V	0.12 x 1.0	le 1.0u..5.0u, Nx 1..10, Nx x (0.12u x le)	le for scaling of emitter length, Nx for scaling number of emitters in a row

6.2 Schematic cross-section

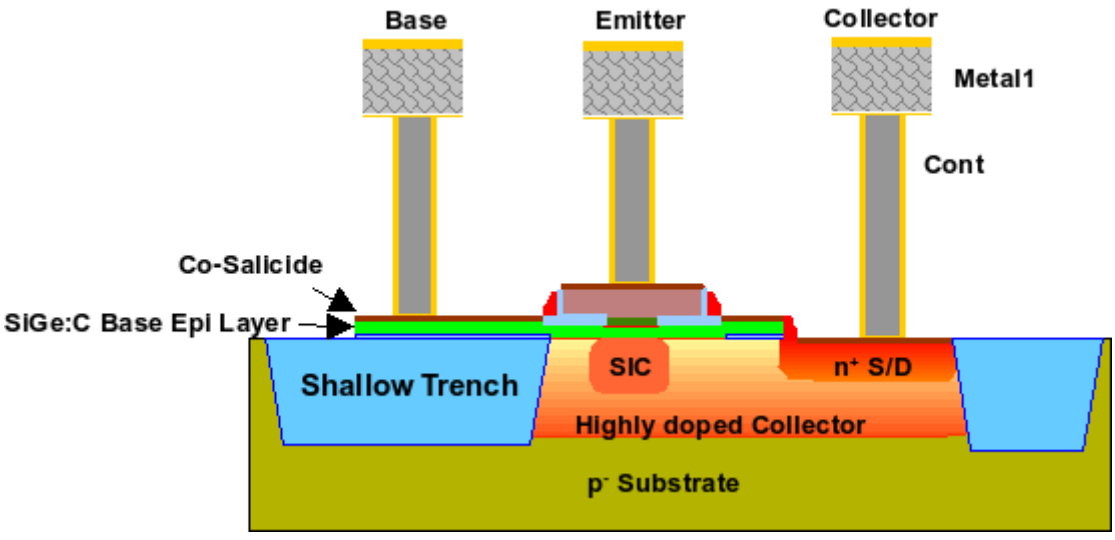

Figure 6.1: Schematic cross-section of the SiGe:C hetero bipolar transistor in SG13G2 technology

6.3 Design rules

The **NPN Substrate-Tie** is formed by **Active** and **pSD** ring. Within **NPN Substrate-Tie** and **TRANS**, **ContBar** is allowed.

The following rules do not apply: nSDB.e

6.3.1 General design rules

Rule	Description	Value
npnG2.a	NPN Substrate-Tie = **Activ** AND **pSD**	
npnG2.b	**NPN Substrate-Tie** must enclose **TRANS**	
npnG2.c	**pSD** enclosure of **Activ** inside **NPN Substrate-Tie**	**0.2**
npnG2.d	Min. unrelated **N+Activ**, **NWell**, **PWell:block**, **nBuLay**, **nSD:block** space to **TRANS**	**1.21**
npnG2.d1	Min. unrelated **GatPoly** space to **TRANS**	**0.9**
npnG2.d2	Min. unrelated **SalBlock** space to **TRANS**	**0.9**
npnG2.e	Min. unrelated **Cont** space to **TRANS**	**0.27**
npnG2.f	**NPN Substrate-Ties** are allowed to overlap each other	

6.3.2 Device related design rules

Rule	Description	Value
npn13G2.a	Min. and max. **SG13G2** emitter length	**0.9**
npn13G2.bR	Max. recommended total number of **SG13G2** emitters per chip	**4000.0**
npn13G2L.a	Min. **SG13G2L** emitter length	**1.0**
npn13G2L.b	Max. **SG13G2L** emitter length	**2.5**
npn13G2L.cR	Max. recommended total number of **SG13G2L** emitters per chip	**800.0**
npn13G2V.a	Min. **SG13G2V** emitter length	**1.0**
npn13G2V.b	Max. **SG13G2V** emitter length	**5.0**
npn13G2V.cR	Max. recommended total number of **SG13G2V** emitters per chip	**800.0**

7 Rules of digital design

7.1 DigiBnd layer

Digital designs can be marked by the **DigiBnd** layer. Either you fill the complete area with this layer or you can use a closed band. The edge is used to mark the inner area as digital design block. For more detail refer to Design Kit User Guide, please.

Within the **DigiBnd** layer follow Design rules are changed compared to the analog flow.

7.2 NWell

Refer to section 3.1 for NWell standard rule definitions.

Rule	Description	Value
NW.c1	Min. **NWell** enclosure of **P+Activ2** (thick gate oxide)	**0.31**
NW.d1	Min. **NWell** space to external **N+Activ2**	**0.31**
NW.e1	Min. **NWell** enclosure of **NWell** tie entirely surrounded by **NWell** in **N+Activ2**	**0.24**
NW.f1	Min. **NWell** space to substrate tie in **P+Activ2**	**0.24**

7.3 Cont

Refer to section 3.14 for Cont standard rule definitions.

Rule	Description	Value
Cnt.c	Min. **Activ** enclosure of **Cont**	**0.05**

7.4 nmosi and nmosiHV

Refer to section 4.7 for nmosi and nmosiHV standard rule definitions.

Rule	Description	Value
nmosi.e1	A separate Iso-PWell contact unabutted to a nmosi device is not allowed	**not used**
nmosi.e2	nmosi unabutted to an Iso-PWell-Activ tie is not allowed	**not used**

7.5 DigiSub layer

The **DigiSub** layer is used to define different substrate potentials for LVS and parasitic extraction. It is not a physical layer and does not provide a physical isolation. For more details read the Design Kit User Guide, please.

7.6 SRAM layer

The **SRAM** layer describes areas with SRAM cells generated by IHP SRAM generator. Within this layer there are special push rules, different to the standard DRC.

7.6.1 NWell

Refer to section 3.1 for NWell standard rule definitions.

Rule	Description	Value
NW.c	Min. **NWell** enclosure of **P+Activ1** (thin gate oxide)	**0.149**
NW.d	Min. **NWell** space to external **N+Activ1**	**0.24**

7.6.2 Activ

Refer to section 3.5 for Activ standard rule definitions.

Rule	Description	Value
Act.c	Min. **Activ** drain/source extension	**0.189**

7.6.3 GatPoly

Refer to section 3.8 for GatPoly standard rule definitions.

Rule	Description	Value
Gat.a	Min. **GatPoly** width	**0.069**
Gat.b	Min. **GatPoly** space or notch	**0.149**
Gat.c	Min. **GatPoly** extension over **Activ** (end cap)	**0.079**
Gat.d	Min. **GatPoly** space to **Activ**	**0.029**

7.6.4 pSD

Refer to section 3.10 for pSD standard rule definitions.

Rule	Description	Value
pSD.e	Min. **pSD** overlap of **Activ** when forming abutted substrate tie	**0.28**
pSD.g	Min. **N+Activ** or **P+Activ** width when forming abutted tie	**0.15**
pSD.g	Min. **pSD** enclosure of PFET gate (thin gate oxide)	**0.068**
pSD.g	Min. **pSD** space to NFET gate (thin gate oxide)	**0.239**

7.6.5 Cont

Refer to section 3.14 for Cont standard rule definitions.

Rule	Description	Value
Cnt.c	Min. **Activ** enclosure of **Cont**	**0.006**
Cnt.d	Min. **GatPoly** enclosure of **Cont**	**0.009**
Cnt.f	Min. **Cont** on **Activ** space to **GatPoly**	**0.059**
Cnt.g2	Min. **pSD** overlap of **Cont** on **pSD-Activ**	**0.075**

7.6.6 Metal1

Refer to section 3.16 for Metal1 standard rule definitions.

Rule	Description	Value
M1.b	Min. **Metal1** space or notch	**0.159**
M1.c1	Min. **Metal1** endcap enclosure of **Cont**	**0.005**
M1.i	Min. space of **Metal1** lines of which at least one is bent by 45-degree	**0.18**

7.7 Metal(n=2-5)

Refer to section 3.17 for Metal(n=2-5) standard rule definitions.

Rule	Description	Value
M1.b	Min. **Metal(n)** space or notch	**0.169**
M1.c1	Min. **Metal(n)** endcap enclosure of **Via(n-1)**	**0.02**

7.8 Via1

Refer to section 3.19 for Via1 standard rule definitions.

Rule	Description	Value
V1.c1	Min. **Metal1** endcap enclosure of **Via1**	**0.005**

7.9 Via(n=2-4)

Refer to section 3.20 for Via(n=2-4) standard rule definitions.

Rule	Description	Value
Vn.c1	Min. **Metal(n)** endcap enclosure of **Via(n)**	**0.005**

8 Localized backside etching (LBE)

Backside Etching module is not tested under all conditions yet. Usage of this feature is without warranty.

Wafer thickness is 700 µm by default.

Areas with removed silicon are defined by LBE layer GDSII number 157.

Rule	Description	Value
LBE.a	Min. **LBE** width	**100.0**
LBE.b	Max. **LBE** width	**1500.0**
LBE.b1	Max. **LBE** area (µm²)	**250000.0**
LBE.b2	Min. **LBE** area (µm²)	**30000.0**
LBE.c	Min. **LBE** space or notch	**100.0**
LBE.d	Min. **LBE** space to inner edge of **EdgeSeal**	**150.0**
LBE.e	Min. **LBE** space to **dfpad** and **Passiv**	**50.0**
LBE.f	Min. **LBE** space to **Activ**	**30.0**
LBE.h	No **LBE** ring allowed	
LBE.i	Max. global **LBE** density [%]	**20.0**

9 Through-silicon via for grounding (TSV_G)

This module is not tested under all conditions yet. Usage of this feature is without warranty.

Areas with etched TSV ring are recognized by **DeepVia** layer GDS number 152. No grid check is performed on layer **DeepVia**.

Rule	Description	Value
TSV_G.a	**DeepVia** has to be a ring structure	
TSV_G.b	Min. and max. **DeepVia** width	**3.0**
TSV_G.c	**DeepVia** ring diameter	**25.0**
TSV_G.d	Min. **DeepVia** space	**25.0**
TSV_G.e	Min. **DeepVia** space to **Activ**, **Activ:filler**, **GatPoly**, **GatPoly:filler** and **Cont**	**5.0**
TSV_G.f	Min. **PWell:block** enclosure of **DeepVia**	**2.5**
TSV_G.g	Min. **Metal1** enclosure of **DeepVia**	**1.5**
TSV_G.h	Min. **Metal1** width over **DeepVia**	**28.0**
TSV_G.i	Max. global **DeepVia** density [%]	**1.0**
TSV_G.j	Max. **DeepVia** coverage ratio for any 500.0 x 500.0 µm² chip area [%]	**10.0**

10 Change history

Revision	Date	Changes
Rev. 0.1	2023-04-20	Initial revision

11 Known issues

- Not every rule section contains a schematic drawing. They will be added in one of the next revisions.