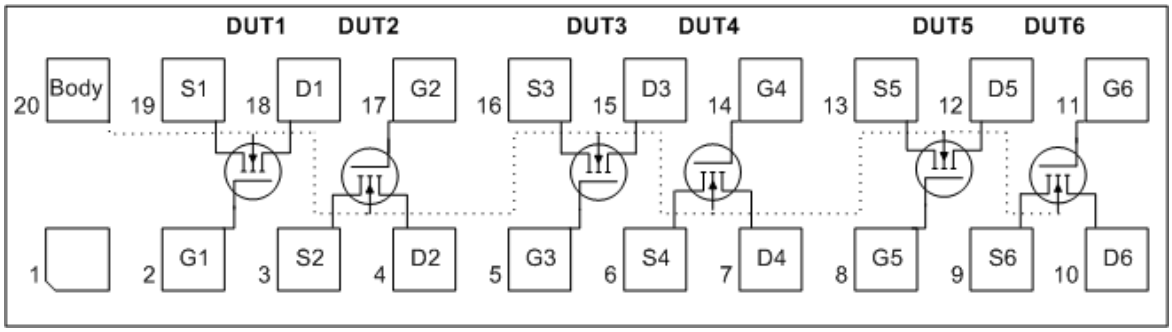
S387: High Voltage PMOS / NMOS FETs Common Body, Vertical Orientation



Vertical Hookup Information

Probe Pad Description	DUT1	DUT2	DUT3	DUT4	DUT5	DUT6
Transistor Type	pmosHV	pmosHV	pmosHV	nmosHV	nmosHV	nmosHV
Common Body	20	20	20	1	1	1
GATPOLY Gate	2	17	5	14	8	11
Source	19	3	16	6	13	9
Drain	18	4	15	7	12	10

Module Rules

MR	Description	Value
1	Maximum Source / Drain Lead Width	5
2	Substrate / Body Lead Width	12
3	Minimum GATPOLY Space to ACTIV	0.1
4	Minimum GATPOLY Interconnect Width	3
5	Length of GATPOLY Extension	0.2
6	Width of GATPOLY Extension	0.13

Design Rules

DR	Description	DUT1	DUT2	DUT3	DUT4	DUT5	DUT6
1	GATPOLY Gate Width per Transistor	10	10	10	10	10	10
2	GATPOLY Gate Length	0.4	0.5	0.6	0.4	0.5	0.6
3	GATPOLY Overhang of ACTIV	0.18	0.18	0.18	0.18	0.18	0.18
4	Minimum ACTIV End Overlap of CONT	0.07	0.07	0.07	0.07	0.07	0.07
5	Minimum ACTIV Side Overlap of CONT	0.07	0.07	0.07	0.07	0.07	0.07
6	Source/Drain CONT Space to Gate	0.11	0.11	0.11	0.11	0.11	0.11
7	METAL1 Overlap of Source/Drain CONT	0.075	0.075	0.075	0.075	0.075	0.075
8	Source/Drain CONT Size X	0.16	0.16	0.16	0.16	0.16	0.16
9	Source/Drain CONT Size Y	0.16	0.16	0.16	0.16	0.16	0.16
10	Source/Drain CONT Spacing	0.18	0.18	0.18	0.18	0.18	0.18
11	Body Space to Source/Drain ACTIV	2.92	2.47	2.02	2.995	2.545	2.095
12	#of Proximity Gates per Side	2	2	2	2	2	2
13	Proximity Gate Space	0.4	0.5	0.6	0.4	0.5	0.6
14	# of Transistor Columns	1	1	1	1	1	1
15	# of Transistor Rows	1	1	1	1	1	1
16	Transistor Column ACTIV Spacing	0.21	0.21	0.21	0.21	0.21	0.21
17	Transistor Row ACTIV Spacing	0.21	0.21	0.21	0.21	0.21	0.21
18	GATPOLY Protection Capacitor Size	0	0	0	0	0	0
19	Gate Protection Diode Size	2.12	2.12	2.12	2.12	2.12	2.12
	# of Source/Drain CONT	29	29	29	1	1	29
	METAL1 Width over Source/Drain CONT	5	5	5	5	5	5
	Total # of Transistors	1	1	1	1	1	1
	Total Gate Width	10	10	10	10	10	10