IHP

SG13G2

Open Source

Layout Rules

Rev. 0.2 (2024-03-08)

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1 General

1.1 Scope

This document describes the design rules for IHPs SG13G2 SiGe BiCMOS technology.

1.2 List of Abbreviations

Table 1.1: List of abbreviations used within this document

Abbreviation	**Explanation**
BiCMOS	Bipolar CMOS
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
IHP	Innovations for High Performance Microelectronics
MIM	Metal-Insulator-Metal
NMOS	Negative Channel Metal Oxide Semiconductor
PMOS	Positive Channel Metal Oxide Semiconductor
RD	Reference Document
SiGe	Silicon Germanium

1.3 Reference Documents

[RD 1] IHP SG13G2 Open Source Process Specification Rev. 1.2

2 Layer Table

This chapter is a documentation of IHP layers definition which is valid in all technologies.

Remark: Only the layers described in the following table are allowed to be used in layout designs. Do not use layers exclusively reserved for internal usage.

Layer name	Purpose	GDS Number	GDS Datatype	Description
Activ	drawing	1	0	Defines active regions in substrate, where transistors, diodes and/or capacitors will be fabricated
Activ	pin	1	2	Activ pin layer
Activ	mask	1	20	added to Active:drawing at mask generation
Activ	filler	1	22	Activ filler layer
Activ	nofill	1	23	Activ filler exclusion layer
Activ	OPC	1	26	Activ outer OPC definition layer
Activ	iOPC	1	27	Activ inner OPC definition layer
Activ	noqrc	1	28	No parasitics extraction
BiWind	drawing	3	0	Defines active npn collector region
BiWind	OPC	3	26	BiWind OPC definition layer
GatPoly	drawing	5	0	Defines polysilicon gates and interconnect
GatPoly	pin	5	2	GatPoly pin layer
GatPoly	filler	5	22	GatPoly filler layer
GatPoly	nofill	5	23	GatPoly filler exclusion layer
GatPoly	OPC	5	26	GatPoly outer OPC definition layer
GatPoly	iOPC	5	27	GatPoly inner OPC definition layer
GatPoly	noqrc	5	28	No parasitics extraction
Cont	drawing	6	0	Defines 1-st metal contacts to Activ, GatPoly
Cont	OPC	6	26	Cont OPC definition layer
nSD	drawing	7	0	Defines areas to receive P+ source/drain implant
nSD	block	7	21	Defines areas which do not receive S/D implants
Metal1	drawing	8	0	Defines 1-st metal interconnect
Metal1	pin	8	2	Metal1 pin layer
Metal1	mask	8	20	added to Metal1:drawing at mask generation
Metal1	filler	8	22	Metal1 filler layer
Metal1	nofill	8	23	Metal1 filler exclusion layer
Metal1	slit	8	24	Metal1 slit definition layer

Metal1	text	8	25	Text layer for Metal1, used for LVS
Metal1	OPC	8	26	Metal1 OPC definition layer
Metal1	noqrc	8	28	No parasitics extraction
Metal1	res	8	29	Wire resistor
Metal1	iprobe	8	33	Current probe
Metal1	diffprb	8	34	Differential current probe
Passiv	drawing	9	0	Defines regions where passivation coating is removed
Passiv	pin	9	2	Passiv pin layer
Passiv	sbump	9	36	Defines passivation openings for solder bump bonding
Passiv	pillar	9	35	Defines passivation openings for copper pillar formation
Passiv	pdl	9	40	Plasma dicing line
Metal2	drawing	10	0	Defines 2-nd metal interconnect
Metal2	pin	10	2	Metal2 pin layer
Metal2	mask	10	20	added to Metal2:drawing at mask generation
Metal2	filler	10	22	Metal2 filler layer
Metal2	nofill	10	23	Metal2 filler exclusion layer
Metal2	slit	10	24	Metal2 slit definition layer
Metal2	text	10	25	Text layer for Metal2, used for LVS
Metal2	OPC	10	26	Metal2 OPC definition layer
Metal2	noqrc	10	28	No parasitics extraction
Metal2	res	10	29	Wire resistor
Metal2	iprobe	10	33	Current probe
Metal2	diffprb	10	34	Differential current probe
BasPoly	drawing	13	0	Defines npn base poly region
BasPoly	pin	13	2	BasPoly pin layer
pSD	drawing	14	0	Defines areas to receive P+ source/drain implant
NLDB	drawing	15	0	Reserved for internal LDMOS development
DigiBnd	drawing	16	0	surrounds areas were digital DRC is valid
Via1	drawing	19	0	Defines 1-st metal to 2-nd metal contact
BackMetal1	drawing	20	0	Defines 1-st back-side metal interconnect
BackMetal1	pin	20	2	BackMetal1 pin layer
BackMetal1	mask	20	20	added to BackMetal1:drawing at mask generation
BackMetal1	filler	20	22	BackMetal1 filler layer
BackMetal1	nofill	20	23	BackMetal1 filler exclusion layer
BackMetal1	slit	20	24	BackMetal1 slit definition layer

BackMetal1	text	20	25	Text layer for BackMetal1, used for LVS
BackMetal1	OPC	20	26	BackMetal1 OPC definition layer
BackMetal1	noqrc	20	28	No parasitics extraction
BackMetal1	res	20	29	Wire resistor
BackMetal1	iprobe	20	33	Current probe
BackMetal1	diffprb	20	34	Differential current probe
BackPassiv	drawing	23	0	Defines regions where passivation coating is removed
RES	drawing	24	0	Identifies resistor areas
SRAM	drawing	25	0	Identifies memory areas
TRANS	drawing	26	0	Identifies bipolar transistor areas
IND	drawing	27	0	Identifies inductor areas
IND	pin	27	2	IND pin layer
IND	text	27	25	
SalBlock	drawing	28	0	Defines non salicided Activ and GatPoly, BasPoly areas
Via2	drawing	29	0	Defines 2-nd metal to 3-rd metal contact
Metal3	drawing	30	0	Defines 3-rd metal interconnect
Metal3	pin	30	2	Metal3 pin layer
Metal3	mask	30	20	added to Metal3:drawing at mask generation
Metal3	filler	30	22	Metal3 filler layer
Metal3	nofill	30	23	Metal3 filler exclusion layer
Metal3	slit	30	24	Metal3 slit definition layer
Metal3	text	30	25	Text layer for Metal3, used for LVS
Metal3	OPC	30	26	Metal3 OPC definition layer
Metal3	noqrc	30	28	No parasitics extraction
Metal3	res	30	29	Wire resistor
Metal3	iprobe	30	33	Current probe
Metal3	diffprb	30	34	Differential current probe
NWell	drawing	31	0	Defines the regions that receive P-Channel VT adjust, P-Channel Punch-Through and N-Well implants
NWell	pin	31	2	NWell pin layer
nBuLay	drawing	32	0	Defines bipolar sub collector and isolated NMOS devices
nBuLay	pin	32	2	nBuLay pin Layer
nBuLay	block	32	21	Defines areas where no nBuLay implant is allowed
EmWind	drawing	33	0	Defines npn emitter window
EmWind	OPC	33	26	EmWind OPC definition layer

DeepCo	drawing	35	0	Defines deep collector regions
MIM	drawing	36	0	Defines Metal-Insulator-Metal capacitor area
EdgeSeal	drawing	39	0	Edge Seal definition layer, reserved for internal use only
Substrate	drawing	40	0	Substrate recognition layer for LVS
Substrate	text	40	25	Substrate recognition text for LVS
dfpad	drawing	41	0	Pad recognition layer
dfpad	pillar	41	35	Copper pillar pad recognition layer
dfpad	sbump	41	36	Solder bump pad recognition layer
ThickGateOx	drawing	44	0	Thick Gate Oxide
PLDB	drawing	45	0	Reserved for internal LDMOS development
PWell	drawing	46	0	Reserved for internal use
PWell	pin	46	2	Pwell pin layer
PWell	block	46	21	Defines areas where no well implants are allowed PWL:=NOT(NWell OR PWellBlock)
IC	drawing	48	0	Reserved for internal use
Via3	drawing	49	0	Defines 3-rd metal to 4-th metal contact
Metal4	drawing	50	0	Defines 4-th metal interconnect
Metal4	pin	50	2	Metal4 pin layer
Metal4	mask	50	20	added to Metal4:drawing at mask generation
Metal4	filler	50	22	Metal4 filler layer
Metal4	nofill	50	23	Metal4 filler exclusion layer
Metal4	slit	50	24	Metal4 slit definition layer
Metal4	text	50	25	Text layer for Metal4, used for LVS
Metal4	OPC	50	26	Metal4 OPC definition layer
Metal4	noqrc	50	28	No parasitics extraction
Metal4	res	50	29	Wire resistor
Metal4	iprobe	50	33	Current probe
Metal4	diffprb	50	34	Differential current probe
HeatTrans	drawing	51	0	Defines heat source for transistors
HeatRes	drawing	52	0	Defines heat source for resistors
FBE	drawing	54	0	Fluidic back side etch
EmPoly	drawing	55	0	Defines npn emitter poly region and pnp base poly region
DigiSub	drawing	60	0	Substrate recognition layer for LVS
NoDRC	drawing	62	0	Excludes areas from design rule checking. Designs with NoDRC are rejected!
TEXT	drawing	63	0	Macrocell name, element text layer
Via4	drawing	66	0	Defines 4-th metal to 5-th metal contact

Metal5	drawing	67	0	Defines 5-th metal interconnect
Metal5	pin	67	2	Metal5 pin layer
Metal5	mask	67	20	added to Metal5:drawing at mask generation
Metal5	filler	67	22	Metal5 filler layer
Metal5	nofill	67	23	Metal5 filler exclusion layer
Metal5	slit	67	24	Metal5 slit definition layer
Metal5	text	67	25	Text layer for Metal5
Metal5	OPC	67	26	Metal5 OPC definition layer
Metal5	noqrc	67	28	No parasitics extraction
Metal5	res	67	29	Wire resistor
Metal5	iprobe	67	33	Current probe
Metal5	diffprb	67	34	Differential current probe
RadHard	drawing	68	0	Defines regions where special radiation hard design rules are applied
MemCap	drawing	69	0	Defines position of RFMEMS cap
Varicap	drawing	70	0	Well implant for varicap devices
IntBondVia	drawing	72	0	Via on top of interposer's TopMetal2
IntBondMet	drawing	73	0	Metal connected to IntBondVia
DevBondVia	drawing	74	0	Via on top of device's TopMetal2
DevBondMet	drawing	75	0	Metal connected to DevBondVia
DevTrench	drawing	76	0	Deep trench from front side for plasma dicing approach
Redist	drawing	77	0	Redistribution layer for metal wiring after chip IO
GraphBot	drawing	78	0	1st graphene layer
GraphTop	drawing	79	0	2nd graphene layer
AntVia1	drawing	83	0	Deep via between TopMetal2 and AntMetal1
AntMetal2	drawing	84	0	Extra second-metal layer for antenna and passive integration
GraphCont	drawing	85	0	GraphBot, GraphTop and GraphGat to GraphMetal1 or GraphMet1L contact
SiWG	drawing	86	0	Backend integrated Si waveguide
SiWG	filler	86	22	SiWG filler layer
SiWG	nofill	86	23	SiWG filler exclusion layer
SiGrating	drawing	87	0	Si waveguide etching layer
SiNGrating	drawing	88	0	SiN waveguide etching layer
GraphPas	drawing	89	0	Additional passivation for graphene structures
EmWind3	drawing	90	0	Defines G3 npn emitter window
EmWiHV3	drawing	91	0	Defines G3 HV npn emitter window

RedBuLay	drawing	92	0	Burried Layer with reduced dose for isolated NLDMOS
SMOS	drawing	93	0	Extraction recognition layer for special CMOS devices
GraphPad	drawing	97	0	Passivation opening
Polimide	drawing	98	0	Reserved for future use
Polimide	pin	98	2	Polimide pin layer
Recog	drawing	99	0	general device recognition shape for device extraction
Recog	pin	99	2	General device pin recognition layer
Recog	esd	99	30	ESD device recognition layer
Recog	diode	99	31	Active diode recognition layer
Recog	tsv	99	32	TSV device recognition layer
Recog	iprobe	99	33	Current probe
Recog	diffprb	99	34	Differential current probe
Recog	pillar	99	35	Copper pillar pad recognition layer
Recog	sbump	99	36	Solder bump pad recognition layer
Recog	otp	99	37	OTP device recognition layer
Recog	pdiode	99	38	Enables extraction of parasitic diodes
Recog	mom	99	39	Metal-on-metal (MOM) capacitor recognition layer
Recog	pcm	99	100	Process control structure recognition layer
ColOpen	drawing	101	0	Defines additional collector opening in SG13 HBTs
GraphMetal1	drawing	109	0	Graphene-metal standard interconnect
GraphMetal1	filler	109	22	GraphMetal1 filler layer
GraphMetal1	nofill	109	23	GraphMetal1 filler exclusion layer
GraphMetal1	slit	109	24	GraphMetal1 slit definition layer
GraphMetal1	OPC	109	26	Graphene-metal opc
GraphMet1L	drawing	110	0	Graphene-metal lift-off interconnect
GraphMet1L	filler	110	22	GraphMet1L filler layer
GraphMet1L	nofill	110	23	GraphMet1L filler exclusion layer
GraphMet1L	slit	110	24	GraphMet1L slit definition layer
GraphMet1L	OPC	110	26	Graphene-metal lift-off opc
EXTBlock	drawing	111	0	Block tip and halo implants
NLDD	drawing	112	0	Dedicated pwell body for NLDMOS
PLDD	drawing	113	0	Dedicated nwell body for PLDMOS
NExt	drawing	114	0	Reserved for internal LDMOS development
PExt	drawing	115	0	Reserved for internal use
NExtHV	drawing	116	0	Reserved for internal use

PExtHV	drawing	117	0	Reserved for internal use
GraphGate	drawing	118	0	Graphene GFET gate
SiNWG	drawing	119	0	Backend integrated SiN waveguide
SiNWG	filler	119	22	SiNWG filler layer
SiNWG	nofill	119	23	SiNWG filler exclusion layer
MEMPAD	drawing	124	0	Dedicated to open Pads in RF-MEMS module
TopVia1	drawing	125	0	Defines 3-rd (or 5-th) metal to TopMetal1 contact
TopMetal1	drawing	126	0	Defines 1-st thick TopMetal layer
TopMetal1	pin	126	2	TopMetal1 pin layer
TopMetal1	mask	126	20	added to TopMetal1:drawing at mask generation
TopMetal1	filler	126	22	TopMetal1 filler layer
TopMetal1	nofill	126	23	TopMetal1 filler exclusion layer
TopMetal1	slit	126	24	TopMetal1 slit definition layer
TopMetal1	text	126	25	Text layer for TopMetal1, used for LVS
TopMetal1	noqrc	126	28	No parasitics extraction
TopMetal1	res	126	29	Wire resistor
TopMetal1	iprobe	126	33	Current probe
TopMetal1	diffprb	126	34	Differential current probe
INLDPWL	drawing	127	0	Dedicated PWell body for isolated NLDMOS
PolyRes	drawing	128	0	used to mark net resistors
PolyRes	pin	128	2	Defines polysilicon gates and interconnect
Vmim	drawing	129	0	used to mark net mim capacitors
nBuLayCut	drawing	131	0	P-separation implat INLDMOS (internal use)
AntMetal1	drawing	132	0	Extra first-metal layer for antenna and passive integration
TopVia2	drawing	133	0	Defines via between TopMetal1 and TopMetal2
TopMetal2	drawing	134	0	Defines 2-nd thick TopMetal layer
TopMetal2	pin	134	2	TopMetal2 pin layer
TopMetal2	mask	134	20	added to TopMetal2:drawing at mask generation
TopMetal2	filler	134	22	TopMetal2 filler layer
TopMetal2	nofill	134	23	TopMetal2 filler exclusion layer
TopMetal2	slit	134	24	TopMetal2 slit definition layer
TopMetal2	text	134	25	Text layer for TopMetal2
TopMetal2	noqrc	134	28	No parasitics extraction
TopMetal2	res	134	29	Wire resistor

TopMetal2	iprobe	134	33	Current probe
TopMetal2	diffprb	134	34	Differential current probe
SNSRing	drawing	135	0	Sensor package ring
Sensor	drawing	136	0	Sensor recognition layer
SNSArms	drawing	137	0	Arms of the Sensor
SNSCMOSVia	drawing	138	0	Defines via between BiCMOS wafer and sensor
ColWind	drawing	139	0	Defines enclosed active transistor region
FLM	drawing	142	0	Defines fluidic channel
HafniumOx	drawing	143	0	MEMRES dielectric layer
MEMVia	drawing	145	0	Local Vias within RFM area
ThinFilmRes	drawing	146	0	ThinFilmRes (V) and recognition layer for RFMEMS
RFMEM	drawing	147	0	Areas for integrated RF MEMS devices
NoRCX	drawing	148	0	No parasitics extraction
NoRCX	m2m3	148	41	No parasitics extraction in Metal2 and Metal3
NoRCX	m2m4	148	42	No parasitics extraction in Metal2 and Metal4
NoRCX	m2m5	148	43	No parasitics extraction in Metal2 and Metal5
NoRCX	m2tm1	148	44	No parasitics extraction in Metal2 and TopMetal1
NoRCX	m2tm2	148	45	No parasitics extraction in Metal2 and TopMetal2
NoRCX	m3m4	148	46	No parasitics extraction in Metal3 and Metal4
NoRCX	m3m5	148	47	No parasitics extraction in Metal3 and Metal5
NoRCX	m3tm1	148	48	No parasitics extraction in Metal3 and TopMetal1
NoRCX	m3tm2	148	49	No parasitics extraction in Metal3 and TopMetal2
NoRCX	m4m5	148	50	No parasitics extraction in Metal4 and Metal5
NoRCX	m4tm1	148	51	No parasitics extraction in Metal4 and TopMetal1
NoRCX	m4tm2	148	52	No parasitics extraction in Metal4 and TopMetal2
NoRCX	m5tm1	148	53	No parasitics extraction in Metal5 and TopMetal1
NoRCX	m5tm2	148	54	No parasitics extraction in Metal5 and TopMetal2
NoRCX	tm1tm2	148	55	No parasitics extraction in TopMetal1 and TopMetal2
NoRCX	m1sub	148	123	No parasitics extraction in Metal1 and Substrate
NoRCX	m2sub	148	124	No parasitics extraction in Metal2 and Substrate

NoRCX	m3sub	148	125	No parasitics extraction in Metal3 and Substrate
NoRCX	m4sub	148	126	No parasitics extraction in Metal4 and Substrate
NoRCX	m5sub	148	127	No parasitics extraction in Metal5 and Substrate
NoRCX	tm1sub	148	300	No parasitics extraction in TopMetal1 and Substrate
NoRCX	tm2sub	148	301	No parasitics extraction in TopMetal2 and Substrate
SNSBotVia	drawing	149	0	Sensor bottom via
SNSTopVia	drawing	151	0	Sensor top via
DeepVia	drawing	152	0	Through Silicon Via
FGEtch	drawing	153	0	At this place the 1-st poly-Si layer (floating-gate) is etched before the 2-nd poly-Si layer (control-gate) is deposited
CtrGat	drawing	154	0	This layer patterns the 2-nd poly-Si layer (control-gate)
FGImp	drawing	155	0	Defines areas where the Floating-gate is doped and the p-well of the flash-cells is formed
EmWiHV	drawing	156	0	EmWind layer for high voltage HBT
LBE	drawing	157	0	For localized back side etch
AlCuStop	drawing	159	0	Reserved for internal use
NoMetFiller	drawing	160	0	Exclude all metall filler
prBoundary	drawing	189	0	Defines boundary of layour cells
Exchange0	drawing	190	0	Support layer for layout data exchange (not used in mask preparation)
Exchange0	pin	190	2	Pin layer of Exchange0
Exchange0	text	190	25	Text layer of Exchange0
Exchange1	drawing	191	0	Support layer for layout data exchange (not used in mask preparation)
Exchange1	pin	191	2	Pin layer of Exchange1
Exchange1	text	191	25	Text layer of Exchange1
Exchange2	drawing	192	0	Support layer for layout data exchange (not used in mask preparation)
Exchange2	pin	192	2	Pin layer of Exchange2
Exchange2	text	192	25	Text layer of Exchange2
Exchange3	drawing	193	0	Support layer for layout data exchange (not used in mask preparation)
Exchange3	pin	193	2	Pin layer of Exchange3
Exchange3	text	193	25	Text layer of Exchange3

Exchange4	drawing	194	0	Support layer for layout data exchange (not used in mask preparation)
Exchange4	pin	194	2	Pin layer of Exchange4
Exchange4	text	194	25	Text layer of Exchange4
isoNWell	drawing	257	0	Defines regions with alternative NWell implant to form isolated NWell

3 General Requirements

3.1 Grid Rules

- All rules are defined in microns [µm] by default if there is no other unit mentioned
- All features are on a drawing grid of 5 nm (0.005 µm)
- Shapes with acute angles <87° are not allowed on any layer
- Following layers are only allowed on 90, 180 degree angles: Cont, Via1, Via2, Via3, Via4, Vmim, TopVia1, TopVia2
- Following layers are only allowed on 90, 135, 180, 225, and 270 degree angles: GatPoly, Activ, Metal1, Metal2, Metal3, Metal4, Metal5, TopMetal1, TopMetal2
- Self-intersecting polygons must be avoided
- Design elements, which are snapped to grid must not violate any geometries in this document.

There are several layers which are not considered for mask generation. Offgrid and angle checks are not applied on the following layers: DigiBnd, RES, SRAM, IND, EdgeSeal, dfpad, HeatTrans, HeatRes, DigiSub, NoDRC, TEXT, RadHard, Flash, SMOS, Scribe, Recog, NoRCX, NoMetFiller

3.2 Forbidden Layers

Following layers are forbidden in designs submitted for all 0.13 µm technologies. Layout data containing these layers will be rejected from the tape-in procedure automatically. Since no waivers are granted, IHP recommends performing the online MPW Rejection Test (https://dk.ihp-microelectronics.com) at an early stage.

Layer name	Purpose	GDS Number	GDS Datatype
BiWind	drawing	3	0
PEmWind	drawing	11	0
BasPoly	drawing	13	0
DeepCo	drawing	35	0
PEmPoly	drawing	53	0
EmPoly	drawing	53	0
LDMOS	drawing	57	0
PBiWind	drawing	58	0
NoDRC	drawing	62	0
Flash	drawing	71	0
ColWind	drawing	139	0

4 Terminology

4.1 Design Rule Terminology

unrelated - two regions which do not touch each other
abut - two edges of two different layers touching each other

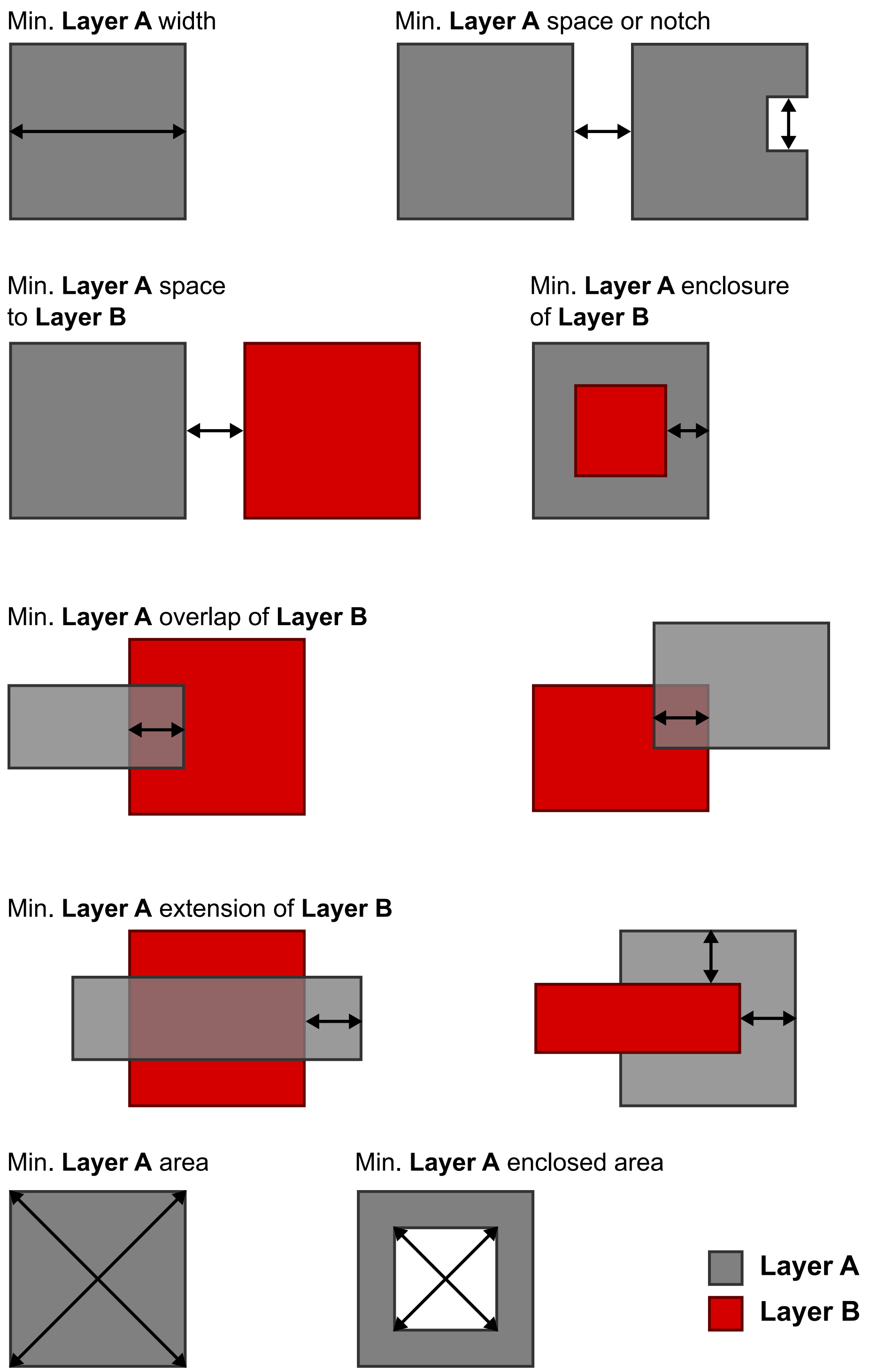

Figure 4.1: Rule check schematics.

4.2 Special Layer Configuration

Various rule definitions require derived layers instead of the original layers defined in chapter 2. The generation rules for the derived layers are described below.

Layer name	Definition
PWell	NOT (**NWell** OR **PWell:block**) OR **PWell:drawing**
nSD[1]	NOT (**pSD** OR **nSD:block**) OR **nSD:drawing**
nBuLay	(((**NWell** ≥ 3.0 µm) sized by -1.0 µm/side) OR **nBuLay:drawing**) AND NOT **nBuLay:block**
NWell tie	(**Activ** AND **nSD**) inside **NWell**
Substrate tie	(**Activ** AND **pSD**) inside **PWell**
N+Activ	**Activ** AND **nSD**
P+Activ	**Activ** AND **pSD**
Gate	**Activ** AND **GatPoly**
NFET	**GatPoly** over (**Activ** AND NOT **pSD**)
PFET	**GatPoly** over ((**Activ** AND **pSD**) inside **NWell**)

[1] **nSD** as a drawing layer only valid if **pSD** and **nSD** are identical. E.g. rhigh resistor (see 6.4)

5 Physical Layer Design Rules

5.1 NWell

Rule	Description	Value
NW.a	Min. **NWell** width	**0.62**
NW.b	Min. **NWell** space or notch (same net). **NWell** regions separated by less than this value will be merged.	**0.62**
NW.b1	Min. **PWell** width between **NWell** regions (different net) (Note 3)	**1.80**
NW.c	Min. **NWell** enclosure of **P+Activ** not inside **ThickGateOx**	**0.31**
NW.c1	Min. **NWell** enclosure of **P+Activ** inside **ThickGateOx**	**0.62**
NW.d	Min. **NWell** space to external **N+Activ** not inside **ThickGateOx**	**0.31**
NW.d1	Min. **NWell** space to external **N+Activ** inside **ThickGateOx**	**0.62**
NW.e	Min. **NWell** enclosure of NWell tie surrounded entirely by **NWell** in **N+Activ** not inside **ThickGateOx**	**0.24**
NW.e1	Min. **NWell** enclosure of NWell tie surrounded entirely by **NWell** in **N+Activ** inside **ThickGateOx**	**0.62**
NW.f	Min. **NWell** space to substrate tie in **P+Activ** not inside **ThickGateOx**	**0.24**
NW.f1	Min. **NWell** space to substrate tie in **P+Activ** inside **ThickGateOx**	**0.62**

Notes

1. **Activ** regions are allowed to cross well boundaries in some ESD protection layouts.
2. Substrate ties for internal logic are required due to p-silicon substrate.
3. A certain distance between **NWell** and **PWell** (see section 4.2) on different nets is required to prevent punchthrough due to different potentials.

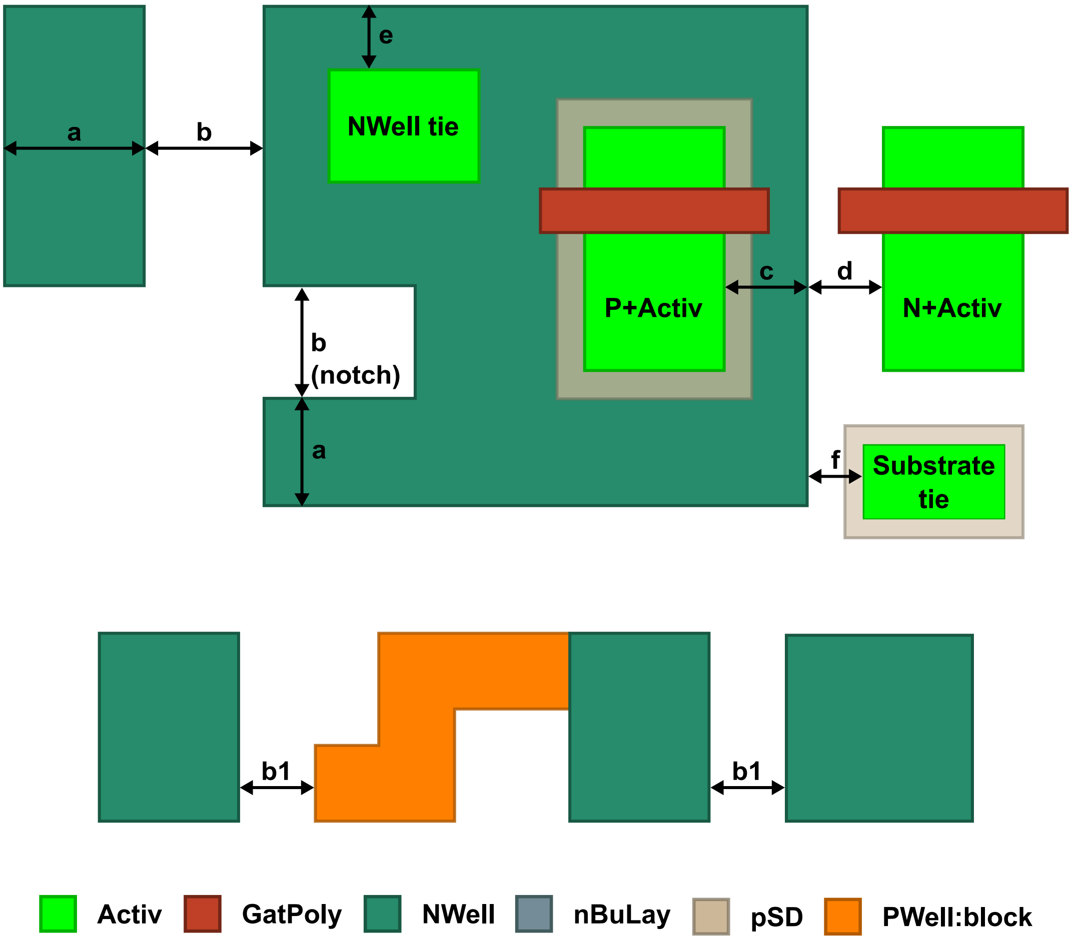

Figure 5.1: **NWell** dimensions (only rule variants without **ThickGatOx** are shown in this figure)

5.2 PWell:block

PWell:block layer is used to generate regions where both **NWell** and **PWell** implants are blocked.

Rule	Description	Value
PWB.a	Min. **PWell:block** width	**0.62**
PWB.b	Min. **PWell:block** space or notch	**0.62**
PWB.c	Min. **PWell:block** space to unrelated **NWell**	**0.62**
PWB.d	Min. **PWell:block** overlap of **NWell**	**0.00**
PWB.e	Min. **PWell:block** space to (**N+Activ** not inside **ThickGateOx**) in **PWell**	**0.31**
PWB.e1	Min. **PWell:block** space to (**N+Activ** inside **ThickGateOx**) in **PWell**	**0.62**
PWB.f	Min. **PWell:block** space to (**P+Activ** not inside **ThickGateOx**) in **PWell**	**0.24**
PWB.f1	Min. **PWell:block** space to (**P+Activ** inside **ThickGateOx**) in **PWell**	**0.62**

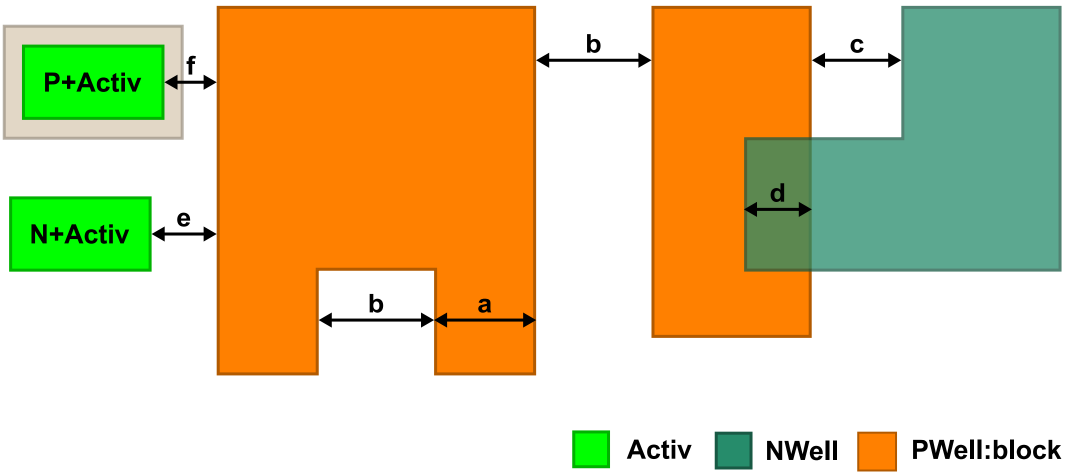

Figure 5.2: PWell:block dimensions

5.3 nBuLay

nBuLay defines regions with deep n-implants (deep nwell). This allows isolated nmos devices to be realized. Furthermore, **nBuLay** may be generated automatically within **NWell** (see 4.2) in order to reduce the resistance of the **NWell**.

Rule	Description	Value
NBL.a	Min. **nBuLay** width	**1.00**
NBL.b	Min. **nBuLay** space or notch (same net)	**1.50**
NBL.c	Min. **PWell** width between **nBuLay** regions (different net) (Note 1)	**3.20**
NBL.d	Min. **PWell** width between **nBuLay** and **NWell** (different net) (Note 1)	**2.20**
NBL.e	Min. **nBuLay** space to unrelated **N+Activ**	**1.00**
NBL.f	Min. **nBuLay** space to unrelated **P+Activ**	**0.50**

Notes

1. A certain **PWell** space to **NWell** and **nBuLay** on different nets is required to prevent punchthrough due to different potentials. Please note that drawn as well as generated **nBuLay** regions are considered (see 4.2).

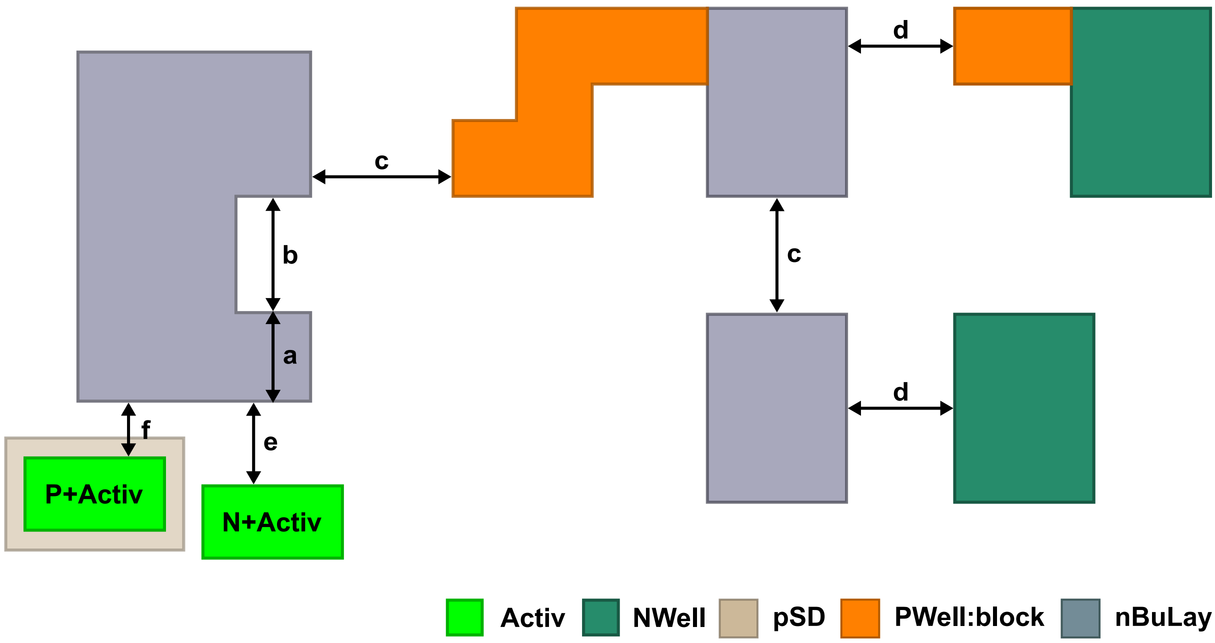

Figure 5.3: nBuLay dimensions

5.4 nBuLay:block

nBuLay:block is used for generating **NWell** structures, which are prevented from **nBuLay** implant. Latchup prevention has to be carefully considered whenever **nBuLay:block** layer is used (see 7.2).

Rule	Description	Value
NBL.a	Min. **nBuLay:block** width	**1.50**
NBL.b	Min. **nBuLay:block** space or notch	**1.00**
NBL.c	Min. **nBuLay** enclosure of **nBuLay:block**	**1.00**
NBL.d	Min. **nBuLay:block** space to unrelated **nBuLay**	**1.50**

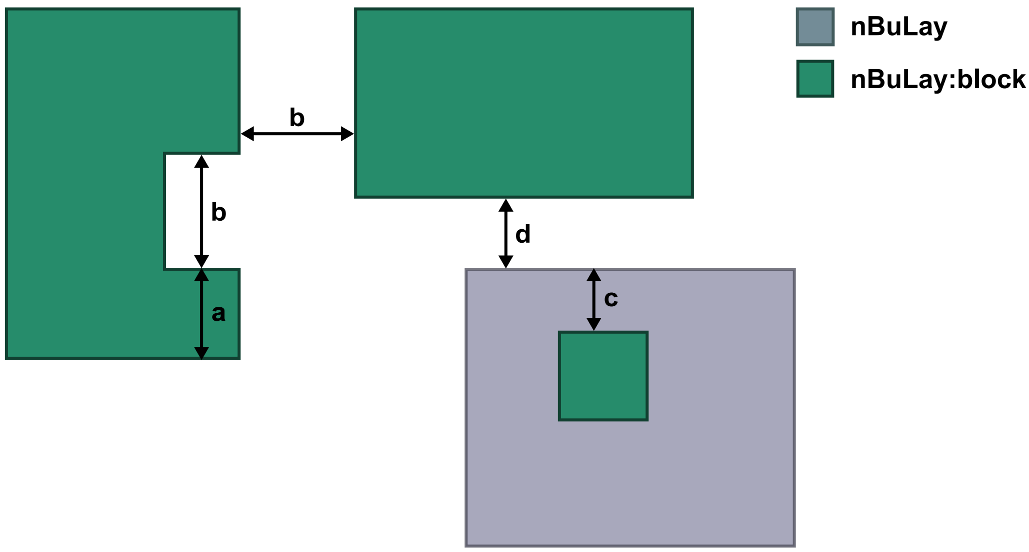

Figure 5.4: nBuLay:block dimensions

5.5 Activ

Rule	Description	Value
Act.a	Min. **Activ** width	**0.15**
Act.b	Min. **Activ** space or notch	**0.21**
Act.c	Min. **Activ** drain/source extension	**0.23**
Act.d	Min. **Activ** area (µm²)	**0.122**
Act.e	Min. **Activ** enclosed area (µm²)	**0.15**

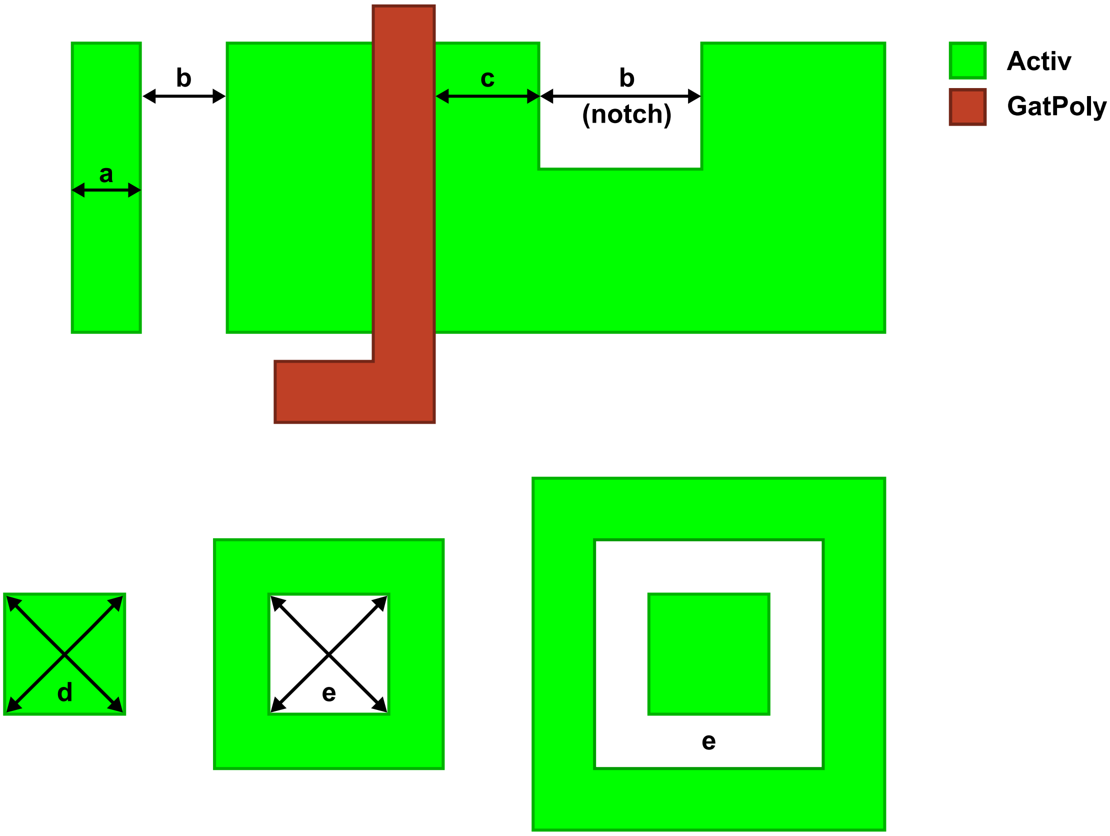

Figure 5.5: Activ dimensions

5.6 Activ:filler

Activ:filler pattern are required in order to reduce layout sensitivity due to etching and CMP process steps.

Rule	Description	Value
AFil.a	Max. **Activ:filler** width	**5.00**
AFil.a1	Min. **Activ:filler** width	**1.00**
AFil.b	Min. **Activ:filler** space	**0.42**
AFil.c	Min. **Activ:filler** space to **Cont**, **GatPoly**	**1.10**
AFil.c1	Min. **Activ:filler** space to **Activ**	**0.42**
AFil.d	Min. **Activ:filler** space to **NWell**, **nBuLay**	**1.00**
AFil.e	Min. **Activ:filler** space to **TRANS**	**1.00**
AFil.g	Min. global **Activ** density [%]	**35.00**
AFil.g1	Max. global **Activ** density [%]	**55.00**
AFil.g2	Min. **Activ** coverage ratio for any 800 x 800 µm² chip area [%]	**25.00**
AFil.g3	Max. **Activ** coverage ratio for any 800 x 800 µm² chip area [%]	**65.00**
AFil.i	Min. **Activ:filler** space to edges of **PWell:block**	**1.50**
AFil.j	Min. **nSD:block** and **SalBlock** enclosure of **Activ:filler** inside **PWell:block**	**0.25**

Notes

1. **Activ:nofill** layer can be used for filler pattern exclusion within specific device areas such as inductors or transformers as long as AFil.g2 and AFil.g3 are fulfilled. For larger sensitive areas it is recommended to minimize the conductivity of **Activ:filler** patterns by using **SalBlock**, **nSD:block** and **PWell:block**.

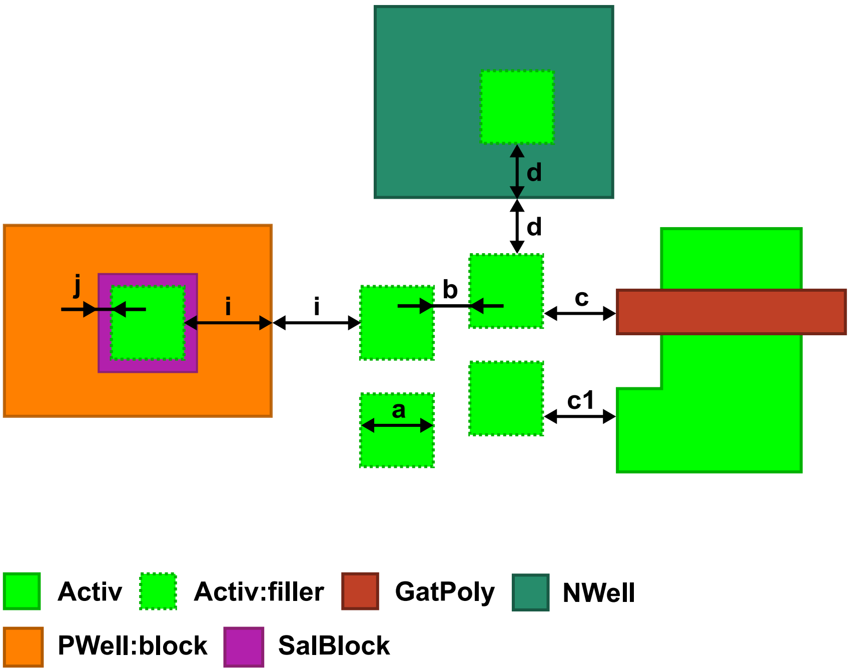

Figure 5.6: Activ:filler dimensions

5.7 ThickGateOxide

Rule	Description	Value
TGO.a	Min. **ThickGateOx** extension over **Activ**	**0.27**
TGO.b	Min. space between **ThickGateOx** and **Activ** outside thick gate oxide region	**0.27**
TGO.c	Min. **ThickGateOx** extension over **GatPoly** over **Activ**	**0.34**
TGO.d	Min. space between **ThickGateOx** and **GatPoly** over **Activ** outside thick gate oxide region	**0.34**
TGO.e	Min. **ThickGateOx** space (merge if less than this value)	**0.86**
TGO.f	Min. **ThickGateOx** width	**0.86**

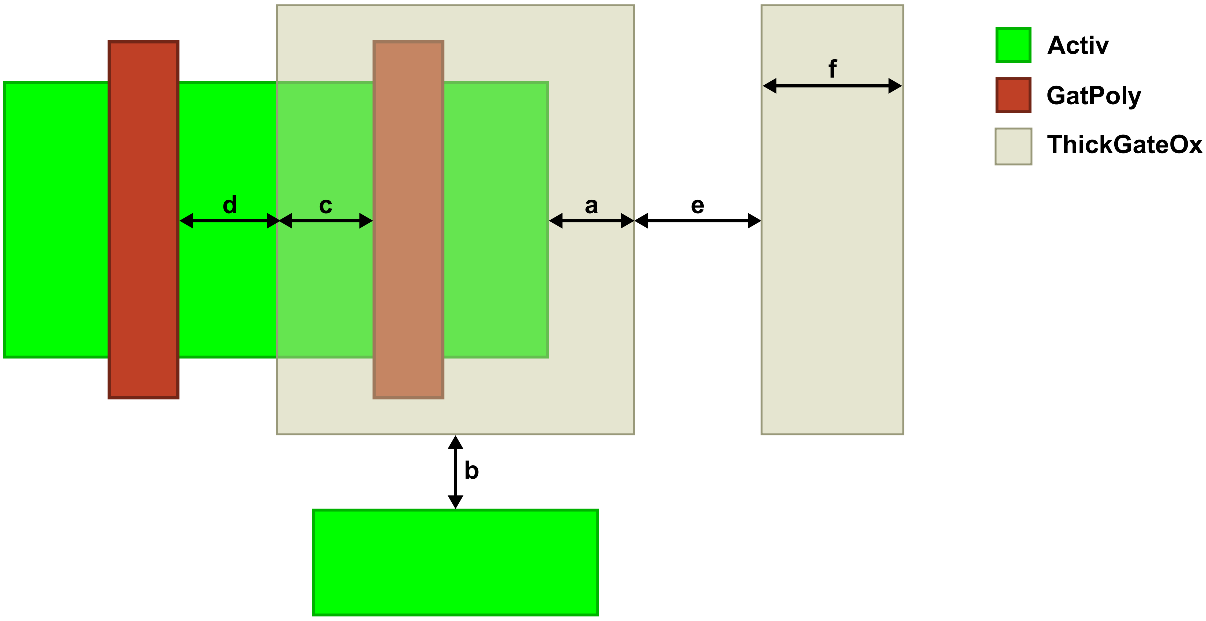

Figure 5.7: ThickGateOx dimensions

5.8 GatPoly

Rule	Description	Value
Gat.a	Min. **GatPoly** width	**0.13**
Gat.a1	Min. **GatPoly** width for channel length of 1.2 V NFET	**0.13**
Gat.a2	Min. **GatPoly** width for channel length of 1.2 V PFET	**0.13**
Gat.a3	Min. **GatPoly** width for channel length of 3.3 V NFET	**0.45**
Gat.a4	Min. **GatPoly** width for channel length of 3.3 V PFET	**0.4**
Gat.b	Min. **GatPoly** space or notch	**0.18**
Gat.b1	Min. space between unrelated 3.3 V **GatPoly** over **Activ** regions	**0.25**
Gat.c	Min. **GatPoly** extension over **Activ** (end cap)	**0.18**
Gat.d	Min. **GatPoly** space to **Activ**	**0.07**
Gat.e	Min. **GatPoly** area (µm²)	**0.09**
Gat.f	45-degree and 90-degree angles for **GatPoly** on **Activ** area are not allowed	
Gat.g	Min. **GatPoly** width for 45-degree bent shapes if the bend **GatPoly** length is > 0.39 µm	**0.16**

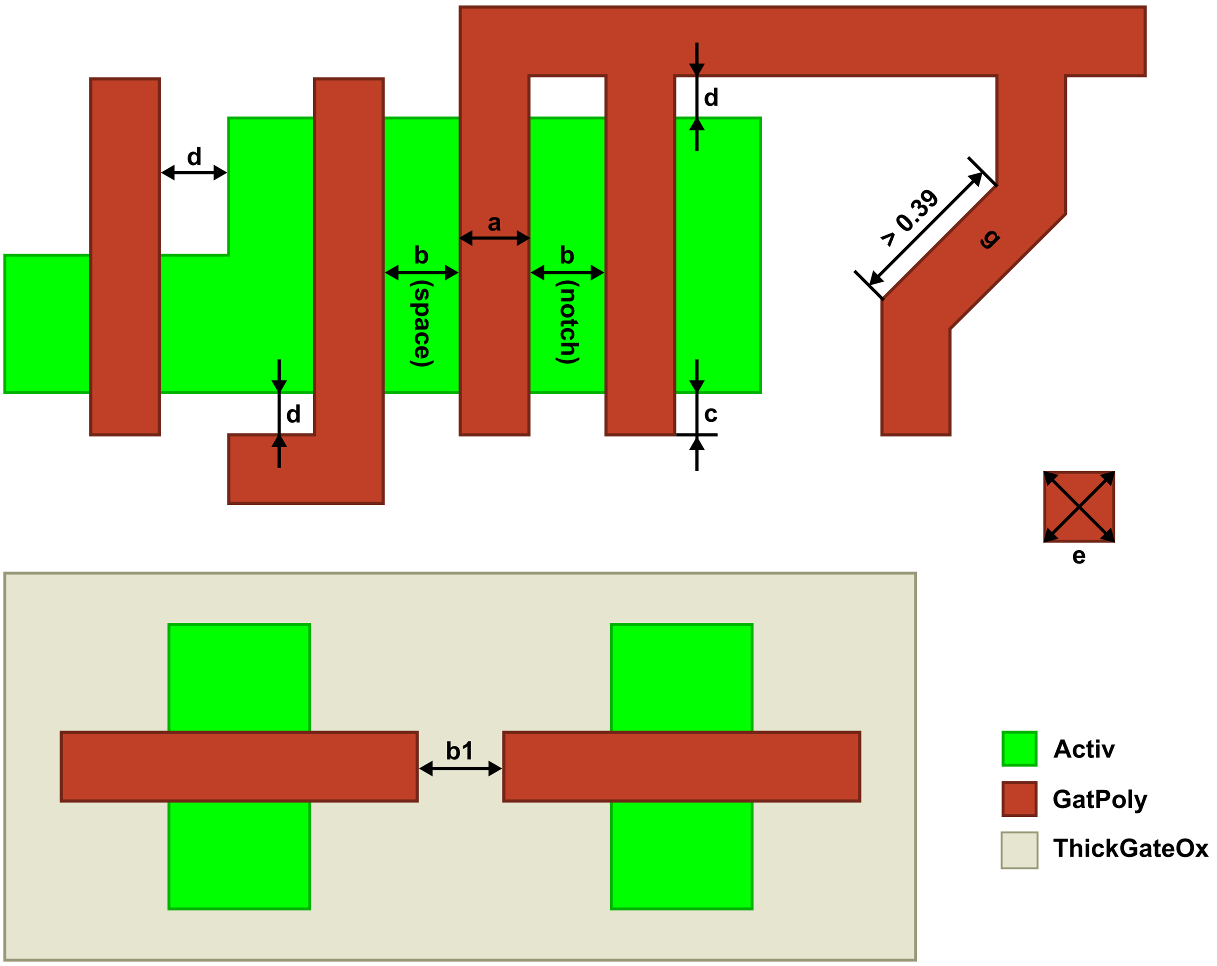

Figure 5.8: GatPoly dimensions

5.9 GatPoly:filler

GatPoly:filler pattern are required in order to reduce layout sensitivity due to etching and CMP process steps.

Rule	Description	Value
GFil.a	Max. **GatPoly:filler** width	**5.00**
GFil.b	Min. **GatPoly:filler** width	**0.70**
GFil.c	Min. **GatPoly:filler** space	**0.80**
GFil.d	Min. **GatPoly:filler** space to **Activ**, **GatPoly**, **Cont**, **pSD**, **nSD:block**, **SalBlock**	**1.10**
GFil.e	Min. **GatPoly:filler** space to **NWell**, **nBuLay**	**1.10**
GFil.f	Min. **GatPoly:filler** space to **TRANS**	**1.10**
GFil.g	Min. global **GatPoly** density [%]	**15.00**
GFil.i	Max. **GatPoly:nofill** area (µm²)	**400 x 400**
GFil.j	Min. **GatPoly:filler** extension over **Activ:filler** (end cap)	**0.18**

Notes

1. **GatPoly:nofill** layer can be used for filler pattern exclusion within specific device areas such as inductors or transformers.

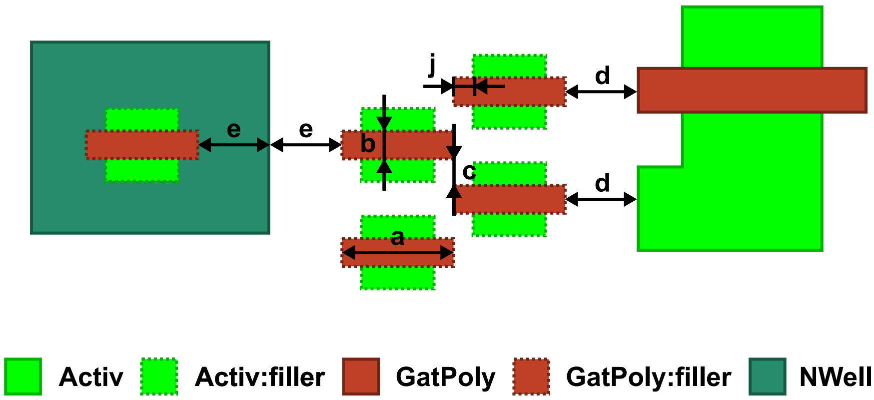

Figure 5.9: GatPoly:filler dimensions

5.10 pSD

Defines regions which receive p+ implants. Typically used for source/drain implants, resistors and substrate ties.

Rule	Description	Value
pSD.a	Min. **pSD** width	**0.31**
pSD.b	Min. **pSD** space or notch (Note 1)	**0.31**
pSD.c	Min. **pSD** enclosure of **P+Activ** in **NWell**	**0.18**
pSD.c1	Min. **pSD** enclosure of **P+Activ** in **PWell**	**0.03**
pSD.d	Min. **pSD** space to unrelated **N+Activ** in **PWell**	**0.18**
pSD.d1	Min. **pSD** space to **N+Activ** in **NWell**	**0.03**
pSD.e	Min. **pSD** overlap of **Activ** at one position when forming abutted substrate tie (Note 2)	**0.30**
pSD.f	Min. **Activ** extension over **pSD** at one position when forming abutted **NWell** tie (Note 2)	**0.30**
pSD.g	Min. **N+Activ** or **P+Activ** area (μm²) when forming abutted tie (Note 2)	**0.09**
pSD.i	Min. **pSD** enclosure of PFET gate not inside **ThickGateOx**	**0.30**
pSD.i1	Min. **pSD** enclosure of PFET gate inside **ThickGateOx**	**0.40**
pSD.j	Min. **pSD** space to NFET gate not inside **ThickGateOx**	**0.30**
pSD.j1	Min. **pSD** space to NFET gate inside **ThickGateOx**	**0.40**
pSD.k	Min. **pSD** area (μm²)	**0.25**
pSD.l	Min. **pSD** enclosed area (μm²)	**0.25**
pSD.m	Min. **pSD** space to n-type poly resistors	**0.18**
pSD.n	Min. **pSD** enclosure of p-type poly resistors	**0.18**

Notes

1. **pSD** regions separated by less than this value will be merged.
2. These rules are for abutted ties: An electrical connection from P+Activ to NWell tie (or N+ Activ to P-sub tie) is made through the source/drain silicide. For a good electrical connection rule pSD.g is important together with rule pSD.e or pSD.f (see Fig. 5.10).

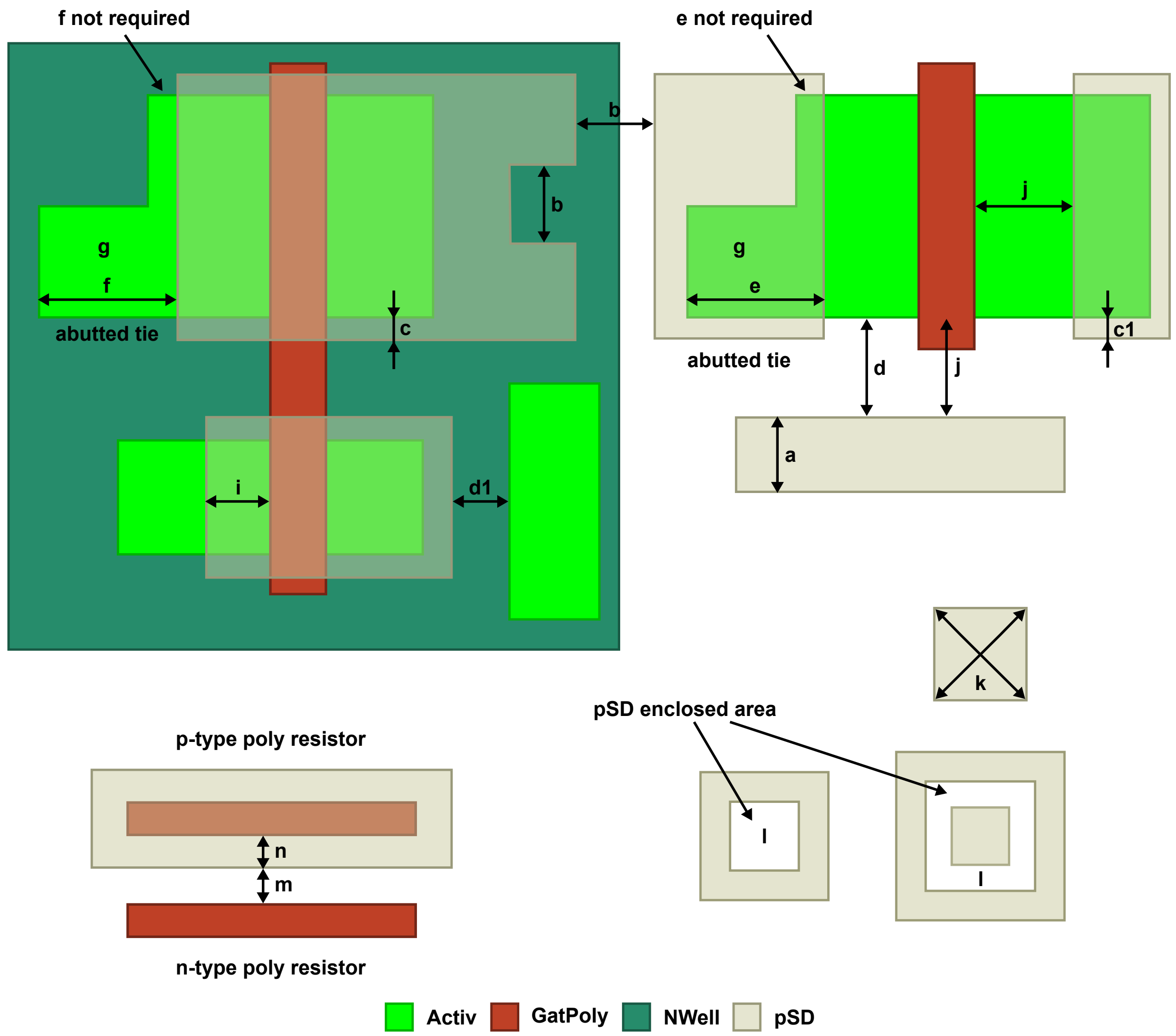

Figure 5.10: pSD dimensions

5.11 nSD:block

nSD:block layer is used to generate regions where n+ S/D implants are blocked. The final mask data **nSD** are generated by: nSD: = NOT (pSD OR nSD:block).

Rule	Description	Value
nSDB.a	Min. **nSD:block** width	**0.31**
nSDB.b	Min. **nSD:block** space or notch	**0.31**
nSDB.c	Min. **nSD:block** space to unrelated **pSD**	**0.31**
nSDB.d	Min. **nSD:block** overlap of **pSD** (Note 1)	**0.00**
nSDB.e	Min. **nSD:block** space to **Cont** (Note 2)	**0.00**

Notes

1. **nSD:block** and **pSD** are allowed to overlap or to be line-on-line.
2. **nSD:block** and **Cont** do not overlap.

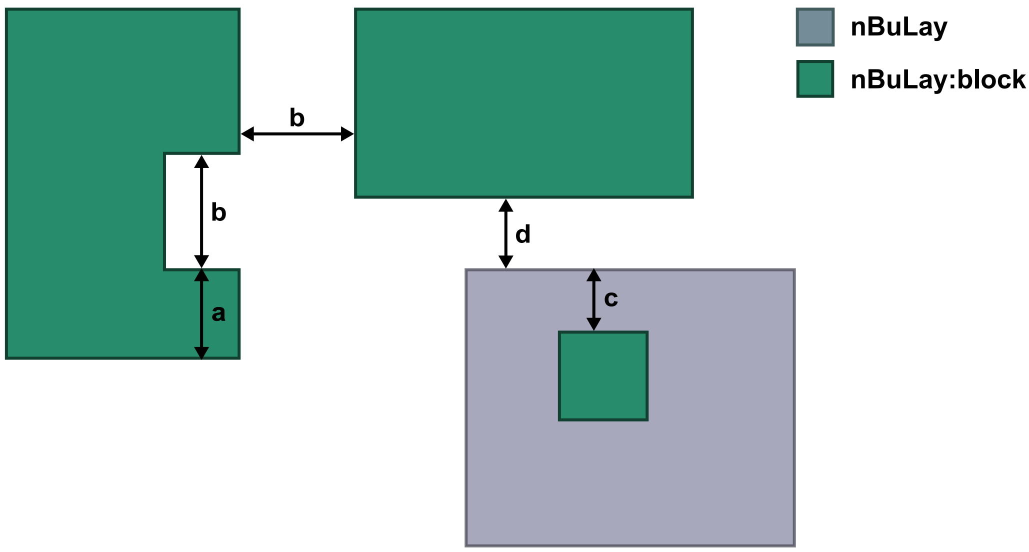

Figure 5.11: nSD:block dimensions

5.12 EXTBlock

EXTBlock layer is used to generate regions where all tip and halo implants are blocked.

Rule	Description	Value
EXT.a	Min. **EXTBlock** width	**0.31**
EXT.b	Min. **EXTBlock** space or notch	**0.31**
EXT.c	Min. **EXTBlock** space to **pSD**	**0.31**

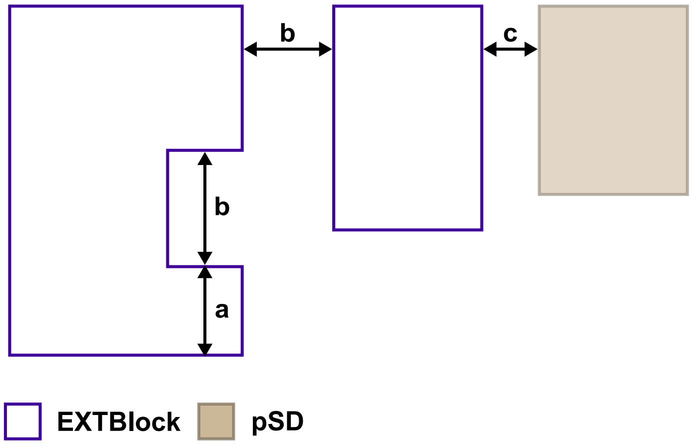

Figure 5.12: EXTBlock dimensions

5.13 SalBlock

SalBlock is used to block salicidation of **GatPoly** or source/drain areas.

Rule	Description	Value
Sal.a	Min. **SalBlock** width	**0.42**
Sal.b	Min. **SalBlock** space or notch	**0.42**
Sal.c	Min. **SalBlock** extension over **Activ** or **GatPoly**	**0.20**
Sal.d	Min. **SalBlock** space to unrelated **Activ** or **GatPoly**	**0.20**
Sal.d	Min. **SalBlock** space to **Cont**	**0.20**

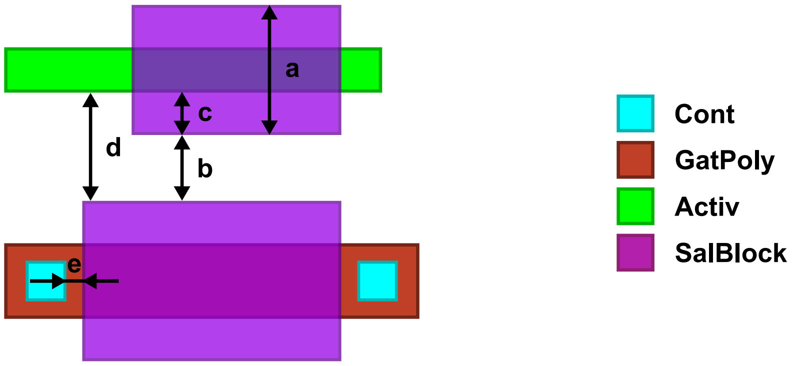

Figure 5.13: SalBlock dimensions

5.14 Cont

This section describes design rules for square-shaped **Cont** regions. All non-square shapes in layer **Cont** are covered in section 5.15.

Rule	Description	Value
Cnt.a	Min. and max. **Cont** width	**0.16**
Cnt.b	Min. **Cont** space	**0.18**
Cnt.b1	Min. **Cont** space in a contact array of more than 4 rows and more then 4 columns (Note 1)	**0.20**
Cnt.c	Min. **Activ** enclosure of **Cont**	**0.07**
Cnt.d	Min. **GatPoly** enclosure of **Cont**	**0.07**
Cnt.e	Min. **Cont** on **GatPoly** space to **Activ**	**0.14**
Cnt.f	Min. **Cont** on **Activ** space to **GatPoly**	**0.11**
Cnt.g	**Cont** must be within **Activ** or **GatPoly**	
Cnt.g1	Min. **pSD** space to **Cont** on **nSD-Activ**	**0.09**
Cnt.g2	Min. **pSD** overlap of **Cont** on **pSD-Activ**	**0.09**
Cnt.h	**Cont** must be covered with **Metal1**	
Cnt.j	**Cont** on **GatPoly** over **Activ** is not allowed	

Notes

1. Cnt.b1 is only required in one direction. The distance of the other direction must be at least Cnt.b.

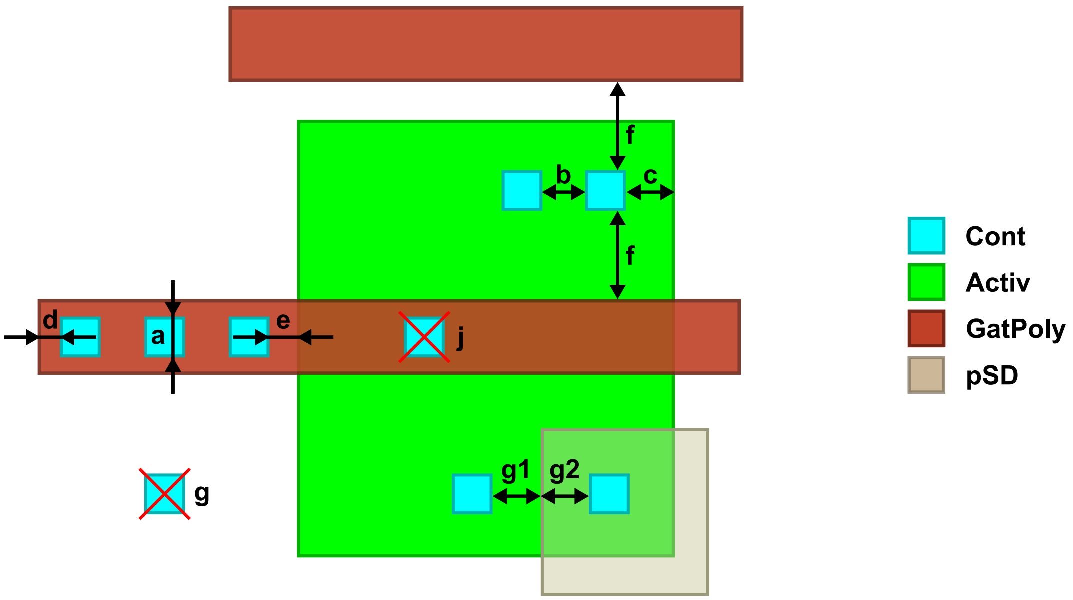

Figure 5.14: Cont dimensions

5.15 ContBar

Any **Cont** shape not being a square shape is considered a **ContBar**.

Rule	Description	Value
CntB.a	Min. and max. **ContBar** width	**0.16**
CntB.a1	Min. **ContBar** length	**0.34**
CntB.b	Min. **ContBar** space	**0.28**
CntB.b1	Min. **ContBar** space with common run > 5 µm	**0.36**
CntB.b2	Min. **ContBar** space to **Cont**	**0.22**
CntB.c	Min. **Activ** enclosure of **ContBar**	**0.07**
CntB.d	Min. **GatPoly** enclosure of **ContBar**	**0.07**
CntB.e	Min. **ContBar** on **GatPoly** space to **Activ**	**0.14**
CntB.f	Min. **ContBar** on **Activ** space to **GatPoly**	**0.11**
CntB.g	**ContBar** must be within **Activ** or **GatPoly**	
CntB.g1	Min. **pSD** space to **ContBar** on **nSD-Activ**	**0.09**
CntB.g1	Min. **pSD** overlap of **ContBar** on **pSD-Activ**	**0.09**
CntB.h	**ContBar** must be covered with **Metal1**	
CntB.h1	Min. **Metal1** enclosure of **ContBar**	**0.05**
CntB.j	**ContBar** on **GatPoly** over **Activ** is not allowed	

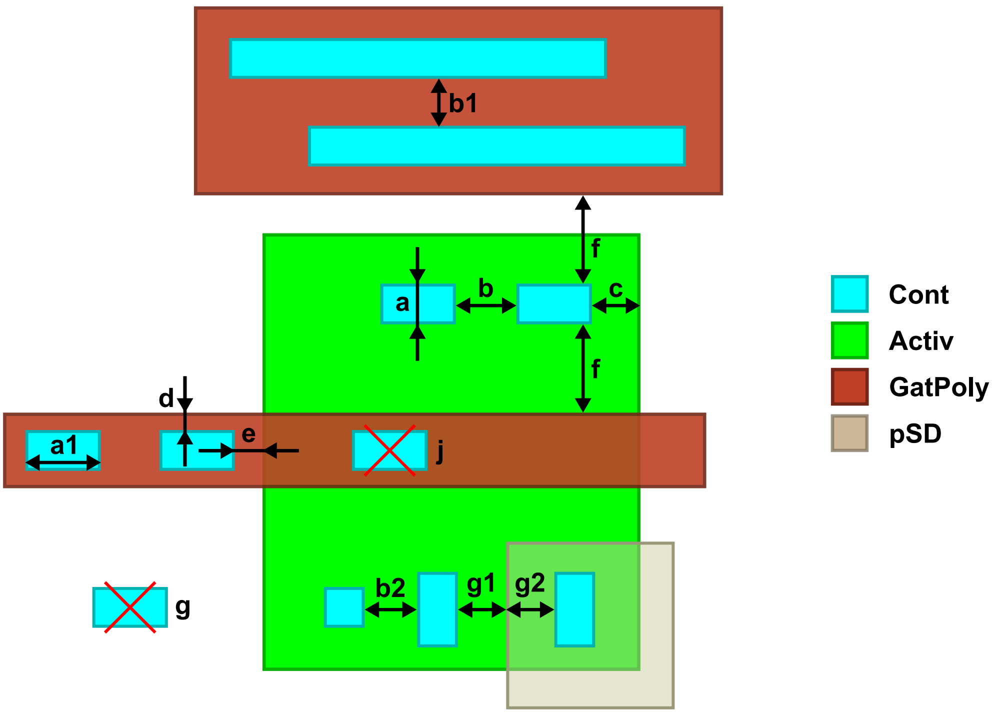

Figure 5.15: ContBar dimensions

5.16 Metal1

Rule	Description	Value
M1.a	Min. **Metal1** width	**0.16**
M1.b	Min. **Metal1** space or notch	**0.18**
M1.c	Min. **Metal1** enclosure of **Cont**	**0.00**
M1.c1	Min. **Metal1** endcap enclosure of **Cont** (Note 1)	**0.05**
M1.d	Min. **Metal1** area (μm²)	**0.09**
M1.e	Min. space of **Metal1** lines if, at least one line is wider than 0.3 μm and the parallel run is more than 1.0 μm	**0.22**
M1.f	Min. space of **Metal1** lines if, at least one line is wider than 10.0 μm and the parallel run is more than 10.0 μm	**0.60**
M1.g	Min. 45-degree bent **Metal1** width if the bent metal length is > 0.5 μm	**0.20**
M1.i	Min. space of **Metal1** lines of which at least one is bent by 45-degree	**0.22**
M1.j	Min. global **Metal1** density [%]	**35.0**
M1.k	Max. global **Metal1** density [%]	**60.0**

Notes

1. For contacts at **Metal1** corners at least one side must be treated as an endcap and for the other sides rule M1.c can be applied.

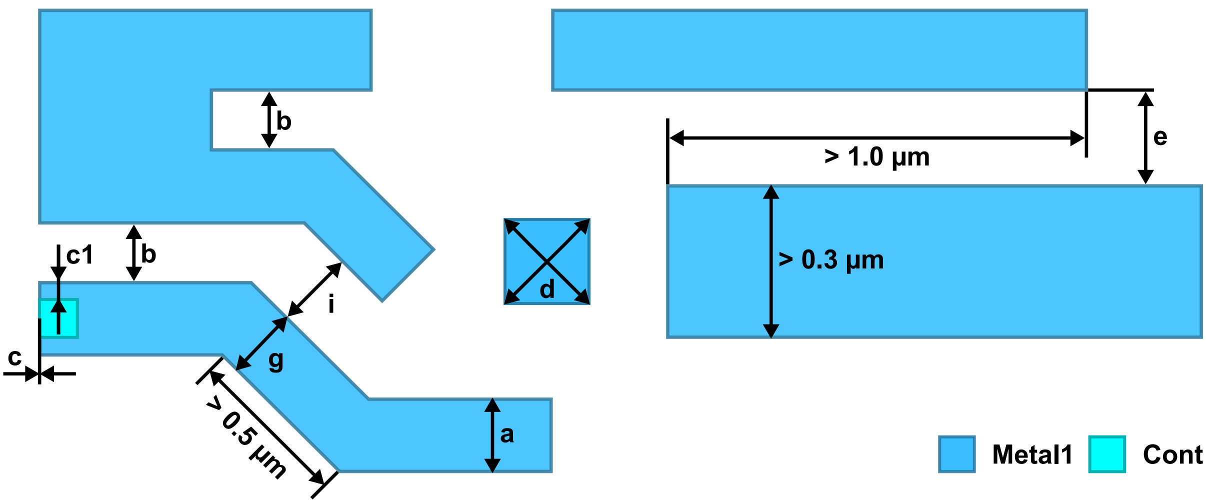

Figure 5.16: Metal1 dimensions

5.17 Metal(n=2-5)

Rule	Description	Value
Mn.a	Min. **Metal(n)** width	**0.20**
Mn.b	Min. **Metal(n)** space or notch	**0.21**
Mn.c	Min. **Metal(n)** enclosure of **Via(n-1)**	**0.005**
Mn.c1	Min. **Metal(n)** endcap enclosure of **Via(n-1)** (Note 1)	**0.05**
Mn.d	Min. **Metal(n)** area (µm²)	**0.144**
Mn.e	Min. space of **Metal(n)** lines if, at least one line is wider than 0.39 µm and the parallel run is more than 1.0 µm	**0.24**
Mn.f	Min. space of **Metal(n)** lines if, at least one line is wider than 10.0 µm and the parallel run is more than 10.0 µm	**0.60**
Mn.g	Min. 45-degree bent **Metal(n)** width if the bent metal length is > 0.5 µm	**0.24**
Mn.i	Min. space of **Metal(n)** lines of which at least one is bent by 45-degree	**0.24**
Mn.j	Min. global **Metal(n)** density [%]	**35.00**
Mn.k	Max. global **Metal(n)** density [%]	**60.00**

Notes

1. For vias at **Metal(n)** corners at least one side must be treated as an endcap and for the other sides rule Mn.c can be applied.

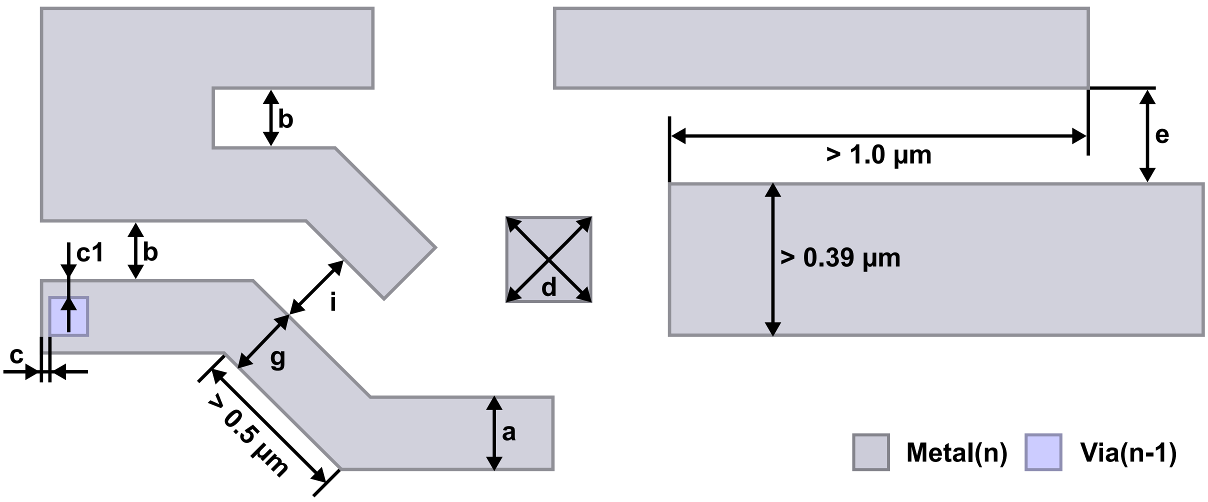

Figure 5.17: Metal(n) dimensions

5.18 Metal(n=1-5):filler

Metal(n):filler pattern are required in order to reduce layout sensitivity due to metal etching and CMP process steps.

Rule	Description	Value
MFil.a1	Min. **Metal(n):filler** width	**1.00**
MFil.a2	Max. **Metal(n):filler** width	**5.00**
MFil.b	Min. **Metal(n):filler** space	**0.42**
MFil.c	Min. **Metal(n):filler** space to **Metal(n)**	**0.42**
MFil.d	Min. **Metal(n):filler** space to **TRANS**	**1.00**
MFil.h	Min. **Metal(n)** and **Metal(n):filler** coverage ratio for any 800 x 800 µm² chip area [%]	**25.00**
MFil.k	Max. **Metal(n)** and **Metal(n):filler** coverage ratio for any 800 x 800 µm² chip area [%]	**75.00**

Notes

1. A smaller coverage or larger filler exclusion area leads to smaller metal lines and higher sheet resistance. Sheet resistance of minimum width **Metal(n)** lines is increasing by 10% if metal coverage is lower than 30%.
2. **Metal(n):filler** must be generated prior to the tape out procedure. For sensitive areas of the circuit, designers should exclude **Metal(n):filler** using the **Metal(n):nofill** or **NoMetFiller** exclusion layer, or should place defined metal structures to prevent metal fill.

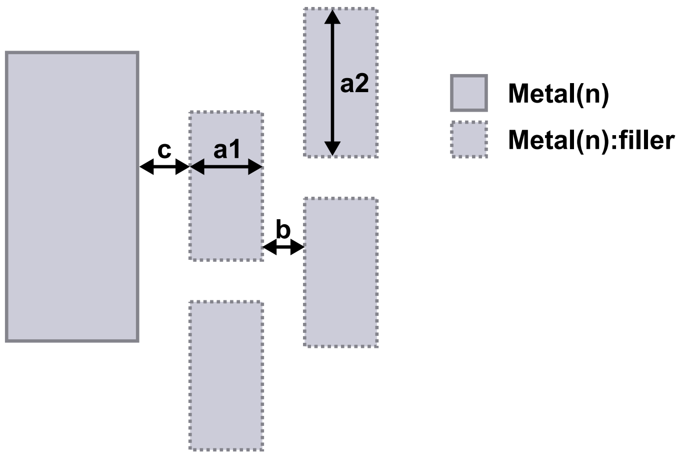

Figure 5.18: Metal(n):filler dimensions

5.19 Via1

Rule	Description	Value
V1.a	Min. and max. **Via1** width	**0.19**
V1.b	Min. **Via1** space	**0.22**
V1.b1	Min. **Via1** space in an array of more than 3 rows and more then 3 columns (Note 1)	**0.29**
V1.c	Min. **Metal1** enclosure of **Via1**	**0.01**
V1.c1	Min. **Metal1** endcap enclosure of **Via1** (Note 2)	**0.05**

Notes

1. V1.b1 is only required in one direction. The distance of the other direction must be at least V1.b.
2. For **Via1** at **Metal1** corners at least one side must be treated as an endcap and for the other sides rule V1.c can be applied.

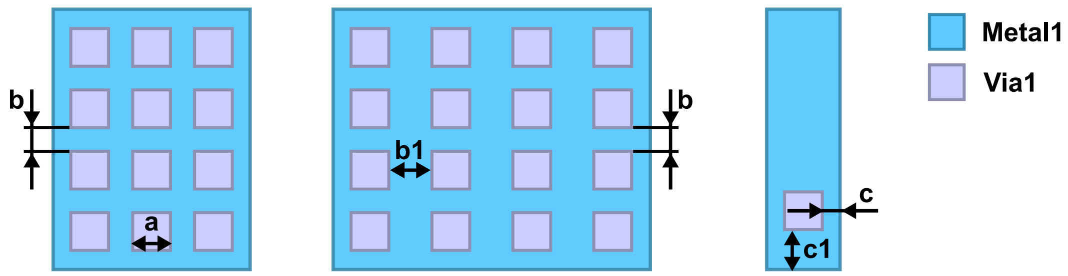

Figure 5.19: Via1 dimensions

5.20 Via(n=2-4)

Rule	Description	Value
Vn.a	Min. and max. **Via(n)** width	**0.19**
Vn.b	Min. **Via(n)** space	**0.22**
Vn.b1	Min. **Via(n)** space in an array of more than 3 rows and more then 3 columns (Note 1)	**0.29**
Vn.c	Min. **Metal(n)** enclosure of **Via(n)**	**0.005**
Vn.c1	Min. **Metal(n)** endcap enclosure of **Via(n)** (Note 2)	**0.05**

Notes

1. Vn.b1 is only required in one direction. The distance of the other direction must be at least Vn.b.
2. For **Via(n)** at **Metal(n)** corners at least one side must be treated as an endcap and for the other sides rule Vn.c can be applied.

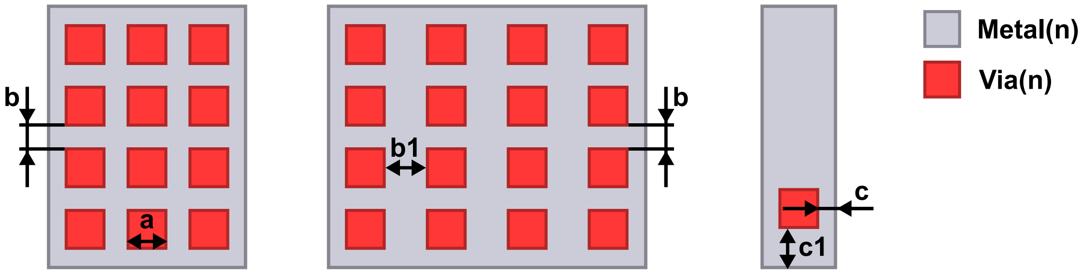

Figure 5.20: Via(n) dimensions

5.21 TopVia1

Rule	Description	Value
TV1.a	Min. and max. **TopVia1** width	**0.42**
TV1.b	Min. **TopVia1** space	**0.42**
TV1.c	Min. **Metal5** enclosure of **TopVia1**	**0.1**
TV1.d	Min. **TopMetal1** enclosure of **TopVia1**	**0.42**

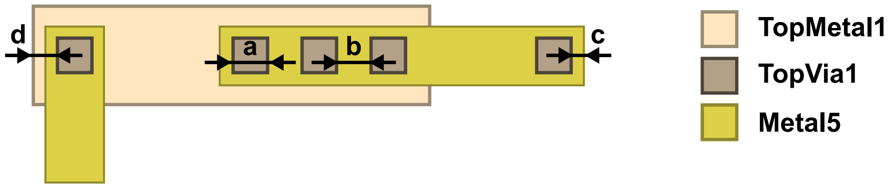

Figure 5.21: TopVia1 dimensions

5.22 TopMetal1

Rule	Description	Value
TM1.a	Min. **TopMetal1** width	**1.64**
TM1.b	Min. **TopMetal1** space or notch	**1.64**
TM1.c	Min. global **TopMetal1** density [%]	**25.00**
TM1.d	Max. global **TopMetal1** density [%]	**70.00**

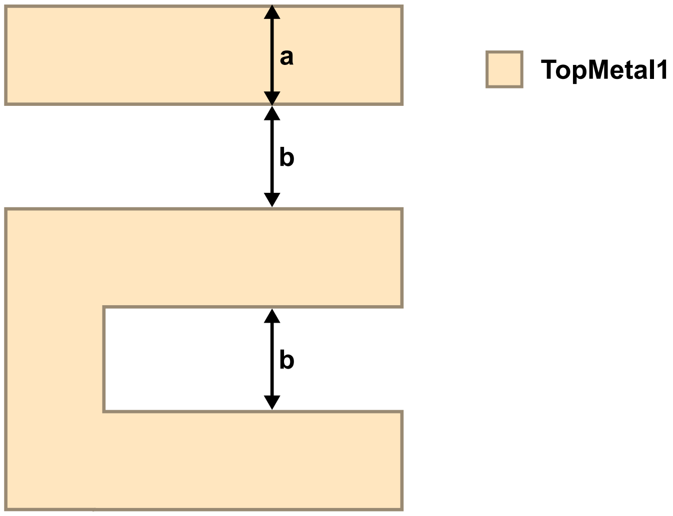

Figure 5.22: TopMetal1 dimensions

5.23 TopMetal1:filler

TopMetal1:filler pattern are required in order to reduce layout sensitivity due to metal etching and CMP process steps.

Rule	Description	Value
TM1Fil.a	Min. **TopMetal1:filler** width	**5.00**
TM1Fil.a1	Max. **TopMetal1:filler** width	**10.00**
TM1Fil.b	Min. **TopMetal1:filler** space	**3.00**
TM1Fil.c	Min. **TopMetal1:filler** space to **TopMetal1**	**3.00**
TM1Fil.d	Min. **TopMetal1:filler** space to **TRANS**	**4.90**

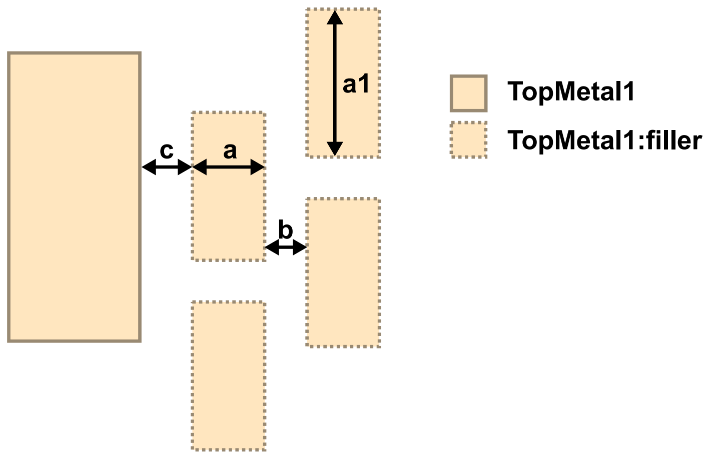

Figure 5.23: TopMetal1:filler dimensions

5.24 TopVia2

Rule	Description	Value
TV2.a	Min. and max. **TopVia2** width	**0.90**
TV2.b	Min. **TopVia2** space	**1.06**
TV2.c	Min. **TopMetal1** enclosure of **TopVia2**	**0.50**
TV2.d	Min. **TopMetal2** enclosure of **TopVia2**	**0.50**

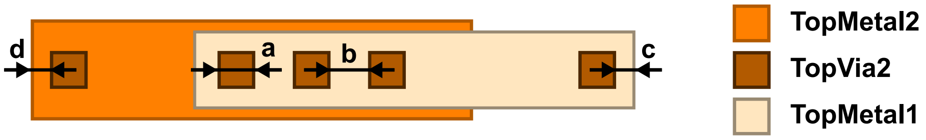

Figure 5.24: TopVia2 dimensions

5.25 TopMetal2

Rule	Description	Value
TM2.a	Min. **TopMetal2** width	**2.00**
TM2.b	Min. **TopMetal2** space or notch	**2.00**
TM2.bR	Min. space of **TopMetal2** lines if, at least one line is wider than 5.0 µm and the parallel run is more than 50.0 µm (Note 1, 2)	**5.00**
TM2.c	Min. global **TopMetal2** density [%]	**25.00**
TM2.d	Max. global **TopMetal2** density [%]	**70.00**

Notes

1. Violations can cause potential issues with TAPEs during backgrinding.
2. Not checked within **IND** regions.

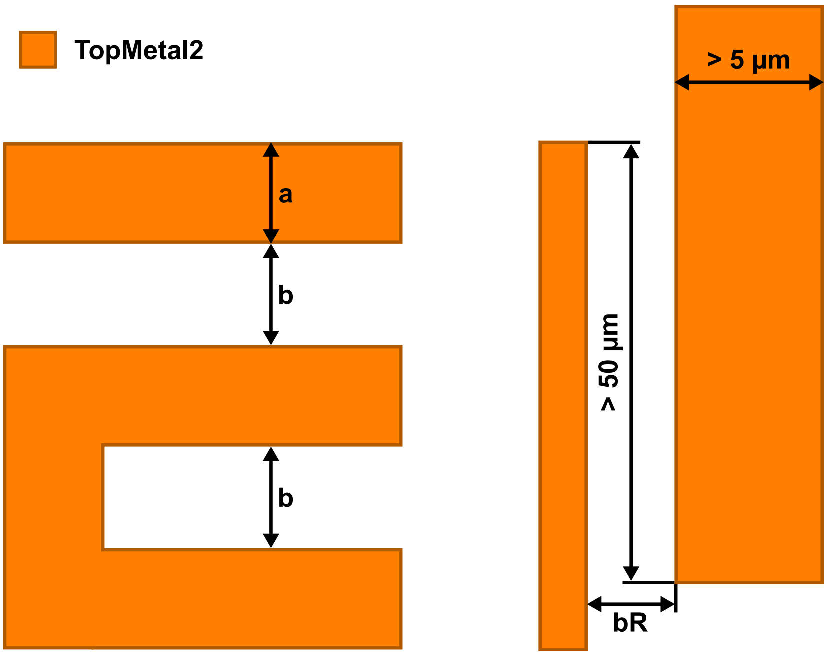

Figure 5.25: TopMetal2 dimensions

5.26 TopMetal2:filler

TopMetal2:filler pattern are required in order to reduce layout sensitivity due to metal etching and CMP process steps.

Rule	Description	Value
TM2Fil.a	Min. **TopMetal2:filler** width	**5.00**
TM2Fil.a1	Max. **TopMetal2:filler** width	**10.00**
TM2Fil.b	Min. **TopMetal2:filler** space	**3.00**
TM2Fil.c	Min. **TopMetal2:filler** space to **TopMetal2**	**3.00**
TM2Fil.d	Min. **TopMetal2:filler** space to **TRANS**	**4.90**

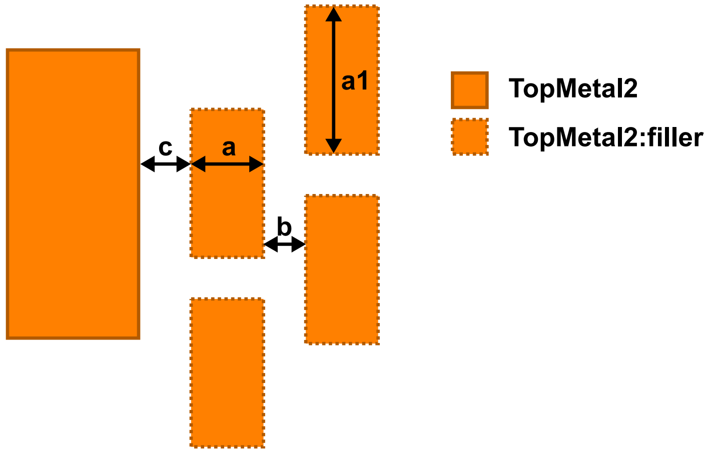

Figure 5.26: TopMetal2:filler dimensions

5.27 Passiv

Rule	Description	Value
Pas.a	Min. **Passiv** width	**2.10**
Pas.b	Min. **Passiv** space or notch	**3.50**
Pas.c	Min. **TopMetal2** enclosure of **Passiv** (Note 1)	**2.10**

Notes

1. Not checked outside of sealring (edge-seal-passive)

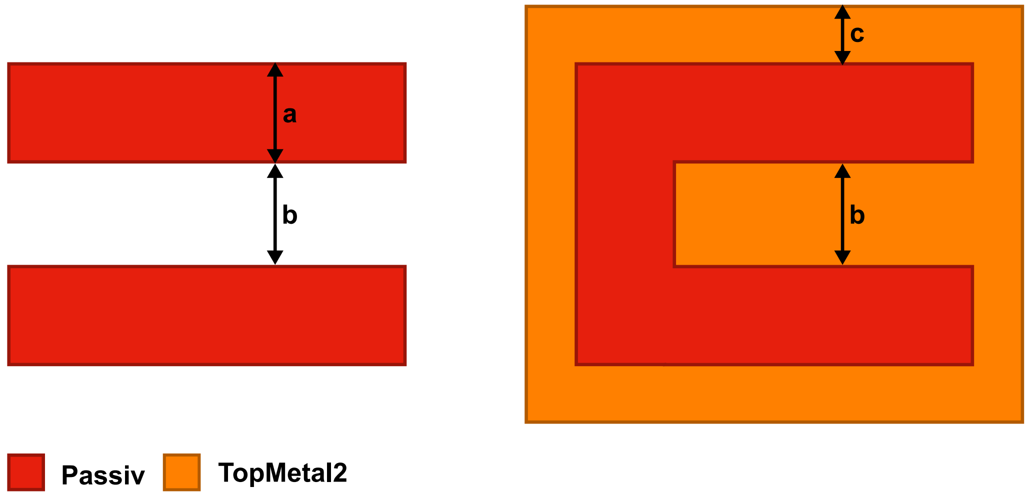

Figure 5.27: Passiv dimensions

6 Device Layout Rules

6.1 Bipolar Design Rules

Bipolar design rules are not disclosed due to IP reasons. Additional layers will be added during the tape out procedure for mask generation. Changing the given layouts may result in catastrophic device malfunction. The IHP library provides a number of predefined devices shown in the follow sections. Do not modify these layouts/abstracts.

Strict design rule: Do not flatten the HBT layout cells and do not place any shapes, except metal for connections, in bipolar **TRANS** regions. Use pins on given metals to connect base, emitter and collector with corresponding metal shapes. Any modification in bipolar transistor results in non-working device.

Device recognition: For device recognition **TRANS** layer in combination with TEXT labels and layer combinations are used for device recognition.

6.1.1 Pre-defined Transistor Layouts

Device	Emitter width	Parameter	Comment
npn13G2	$W_E = 0.07u$	$L_E = 0.9u$, $N_x = 1 \dots 10$, $A_E = N_x\,(0.07u \cdot L_E)$	L_E: emitter length, A_E: emitter area, N_x: number of emitters in a row
npn13G2L	$W_E = 0.07u$	$L_E = 1.0u \dots 2.5u$, $N_x = 1 \dots 4$, $A_E = N_x\,(0.07u \cdot L_E)$	L_E: emitter length, A_E: emitter area, N_x: number of emitters in a row
npn13G2V	$W_E = 0.12u$	$L_E = 1.0u \dots 5.0u$, $N_x = 1 \dots 8$, $A_E = N_x\,(0.12u \cdot L_E)$	L_E: emitter length, A_E: emitter area, N_x: number of emitters in a row

6.1.2 Schematic Cross-section

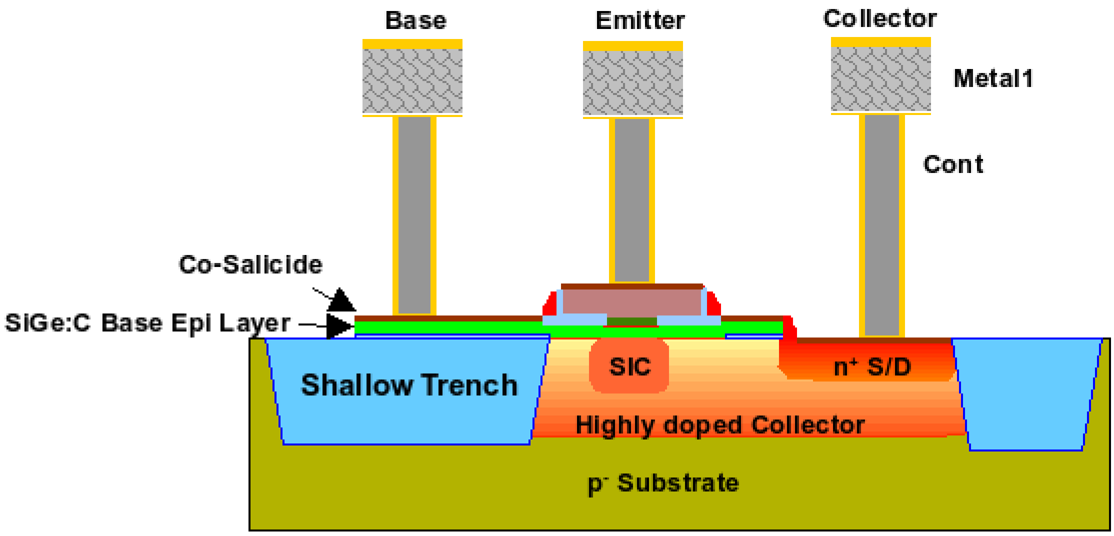

Figure 6.1: Schematic cross-section of the SiGe:C hetero bipolar transistor

6.1.3 Design Rules

The **NPN Substrate-Tie** is formed by **Activ** and **pSD** ring.

The following rules do not apply: nSDB.e

General Design Rules

Rule	Description	Value
npnG2.a	NPN Substrate-Tie = **Activ** AND **pSD**	
npnG2.b	**NPN Substrate-Tie** must enclose **TRANS**	
npnG2.c	**pSD** enclosure of **Activ** inside **NPN Substrate-Tie**	**0.20**
npnG2.d	Min. unrelated **N+Activ**, **NWell**, **PWell:block**, **nBuLay**, **nSD:block** space to **TRANS**	**1.21**
npnG2.d1	Min. unrelated **GatPoly** space to **TRANS**	**0.90**
npnG2.d2	Min. unrelated **SalBlock** space to **TRANS**	**0.90**
npnG2.e	Min. unrelated **Cont** space to **TRANS**	**0.27**
npnG2.f	**NPN Substrate-Ties** are allowed to overlap each other	

Device Related Design Rules

Rule	Description	Value
npn13G2.a	Min. and max. **npn13G2** emitter length	**0.90**
npn13G2.bR	Max. recommended total number of **npn13G2** emitters per chip	**4000**
npn13G2L.a	Min. **npn13G2L** emitter length	**1.00**
npn13G2L.b	Max. **npn13G2L** emitter length	**2.50**
npn13G2L.cR	Max. recommended total number of **npn13G2L** emitters per chip	**800**
npn13G2V.a	Min. **npn13G2V** emitter length	**1.00**
npn13G2V.b	Max. **npn13G2V** emitter length	**5.00**
npn13G2V.cR	Max. recommended total number of **npn13G2V** emitters per chip	**800**

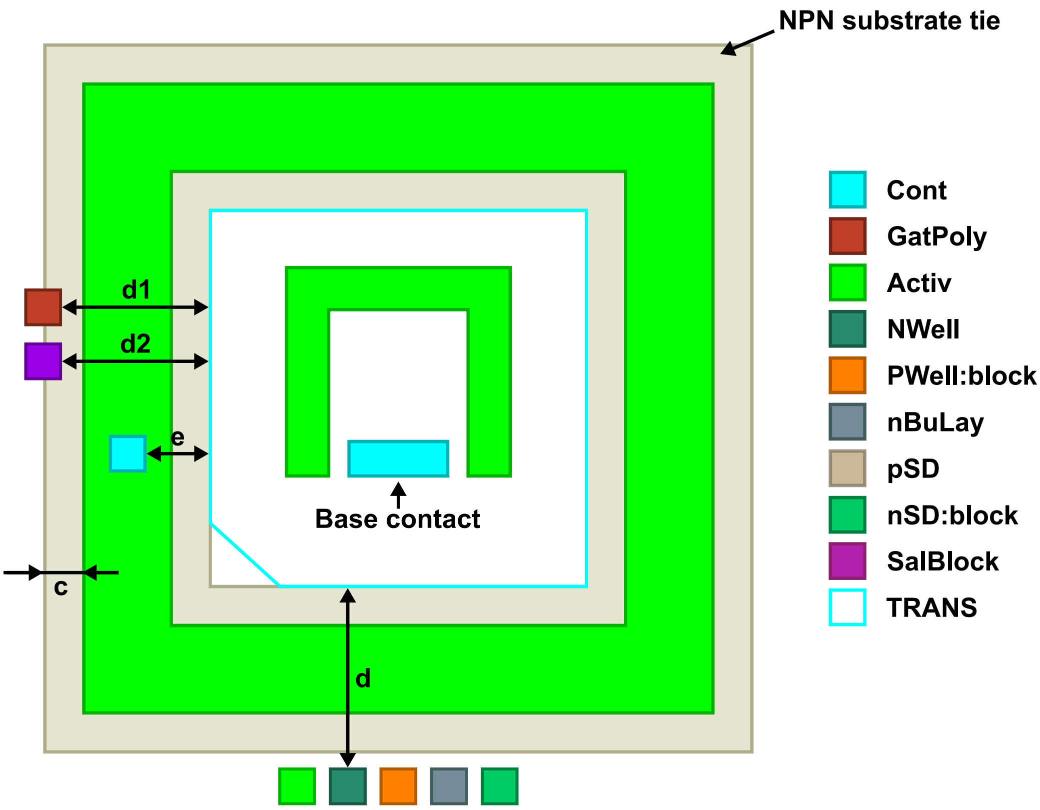

Figure 6.2: HBT dimensions.

6.2 Rsil

Rsil represents the salicided n+ doped **GatPoly** resistor.

Device recognition: Rsil = **RES** + **GatPoly**

Rule	Description	Value
Rsil.a	Min. **GatPoly** width	**0.50**
Rsil.b	Min. **RES** space to **Cont**	**0.12**
Rsil.c	Min. **RES** extension over **GatPoly**	**0.00**
Rsil.d	Min. **pSD** space to **GatPoly**	**0.18**
Rsil.e	Min. **EXTBlock** enclosure of **GatPoly**	**0.18**
Rsil.f	Min. **RES** length	**0.50**

Notes

1. **RES** represents the resistor definition layer and is required for back annotation.

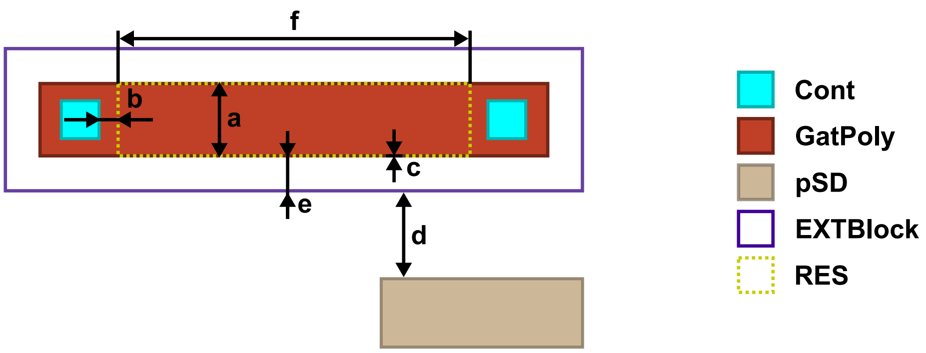

Figure 6.3: Rsil dimensions

6.3 Rppd

Rppd represents the unsalicided p+ doped **GatPoly** resistor.

Device recognition: Rppd = **SalBlock** + **GatPoly** + **pSD**

Rule	Description	Value
Rppd.a	Min. **GatPoly** width	**0.50**
Rppd.b	Min. **pSD** enclosure of **GatPoly**	**0.18**
Rppd.c	Min. and max. **SalBlock** space to **Cont**	**0.20**
Rppd.d	Min. **EXTBlock** enclosure of **GatPoly**	**0.18**
Rppd.e	Min. **SalBlock** length	**0.50**

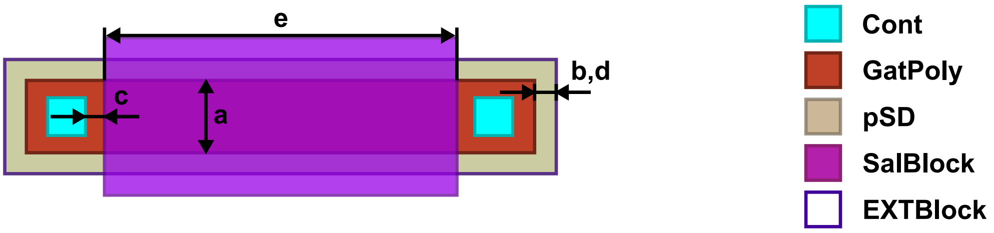

Figure 6.4: Rppd dimensions

6.4 Rhigh

Rhigh represents an unsalicided partial compensated low n-doped **GatPoly** resistor.

Device recognition: Rhigh = **SalBlock** + **GatPoly** + **pSD** + **nSD**

Rule	Description	Value
Rhi.a	Min. **GatPoly** width	**0.50**
Rhi.b	**pSD** and **nSD** are identical (Note 1)	
Rhi.c	Min. **pSD** and **nSD** enclosure of **GatPoly**	**0.18**
Rhi.d	Min. and max. **SalBlock** space to **Cont**	**0.20**
Rhi.e	Min. **EXTBlock** enclosure of **GatPoly**	**0.18**
Rhi.f	Min. **SalBlock** length	**0.50**

Notes

1. **nSD:drawing** is only permitted within **Rhigh** resistors. Apart from that, **nSD** is generated automatically (see section 4.2).

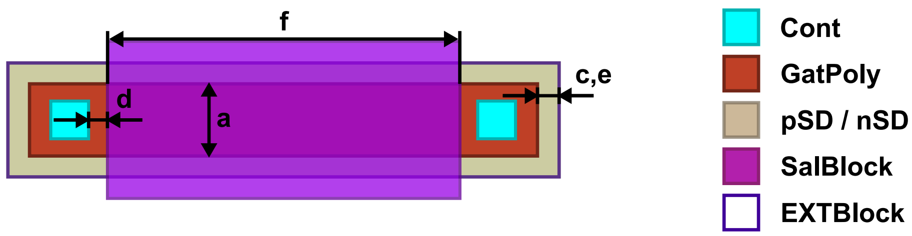

Figure 6.5: Rhigh dimensions

6.5 nmosi and nmosiHV

Device recognition: nmosi is recognized as an nmos device. The difference of nmosi and nmosiHV is given by **ThickGateOx**. There are special device construction rules for this substrate isolated nmos device. These rules will only be tested inside a closed ring of **NWell** AND **nBuLay**.

Rule	Description	Value
nmosi.b	Min. **nBuLay** enclosure of **Iso-PWell-Activ** (Note 1)	**1.24**
nmosi.c	Min. **NWell** space to **Iso-PWell-Activ**	**0.39**
nmosi.d	Min. **NWell-nBuLay** width forming an unbroken ring around any **Iso-PWell-Activ** (Note 2)	**0.62**
nmosi.e1	A separate Iso-PWell contact unabutted to a nmosi device is not allowed	
nmosi.e2	nmosi unabutted to an Iso-PWell-Activ tie is not allowed	
nmosi.f	Min. **nSD:block** width to separate ptap in nmosi	**0.62**
nmosi.g	Min. **SalBlock** overlap of **nSD:block** over **Activ**	**0.15**

Notes

1. Iso-PWell-Activ = **Activ** AND **nBuLay** AND **PWell**
2. NWell-nBuLay = **NWell** AND **nBuLay**
3. NWell which is used as a ring for isolated PWell and carries active p-mos devices has to be carefully layed out in order to prevent latch up.
4. Recommendation: 1 mimimum PWell contact per 50 µm². To calculate voltage drops in PWell consider an average sheet resistance of 3 kΩ.
5. Recommendation: Use ptapsb Pcell to ensure proper isolated PWell connection. An example can be found in Cadence PDK's example library.

6.6 isolbox

The isolbox structure is used to generate PWell regions isolated from the global substrate. This enables the realization of substrate isolated nmos transistors or resistors. We recommend to use only pcell offered via PDK by IHP. The pins "isosub" and "bn" are not part of the layout pcell and have to be placed manually in order to give designer more flexibility.

Device recognition: isolbox = TEXT "isolbox" within (**NWell** enclosed by **Recog:diode**)

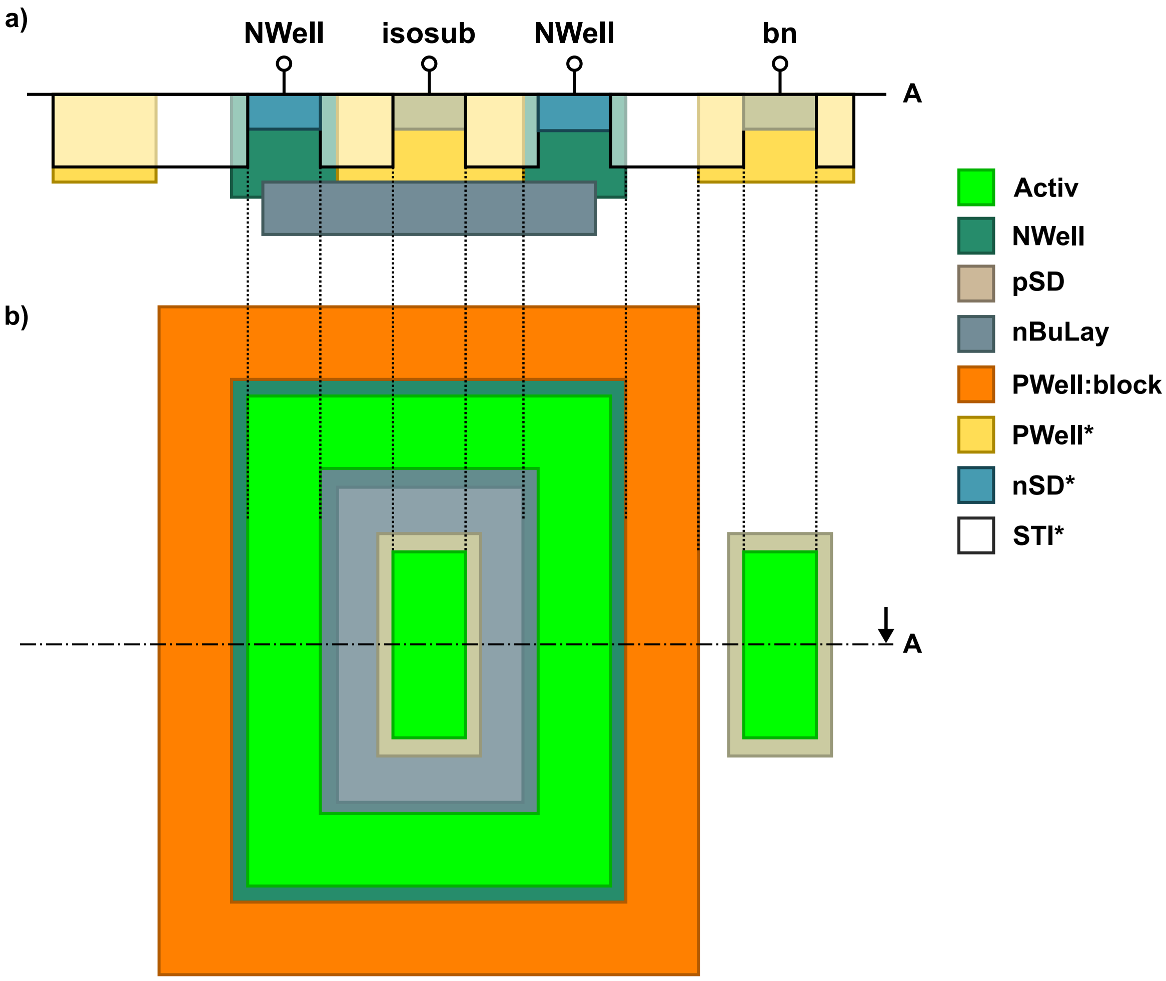

Figure 6.6: a) Cross-section and b) top view of the isolbox device. (* These layers are inherently derived from drawing layers.)

6.7 Schottky diode

Device recognition: schottky_nbl1 = **ContBar** enclosed by (**SalBlock** and **nSD:block** and **PWell:block** and not **nBuLay**)

The following rules do not apply: NW.c1, NW.e1, PWB.f1, CntB.a, LU.d

Rule	Description	Value
Sdiod.a	Min. and max. **PWell:block** enclosure of **ContBar**	**0.25**
Sdiod.b	Min. and max. **nSD:block** enclosure of **ContBar**	**0.40**
Sdiod.c	Min. and max. **SalBlock** enclosure of **ContBar**	**0.45**
Sdiod.d	Min. and max. **ContBar** width inside **nBuLay**	**0.30**
Sdiod.e	Min. and max. **ContBar** length inside **nBuLay**	**1.00**

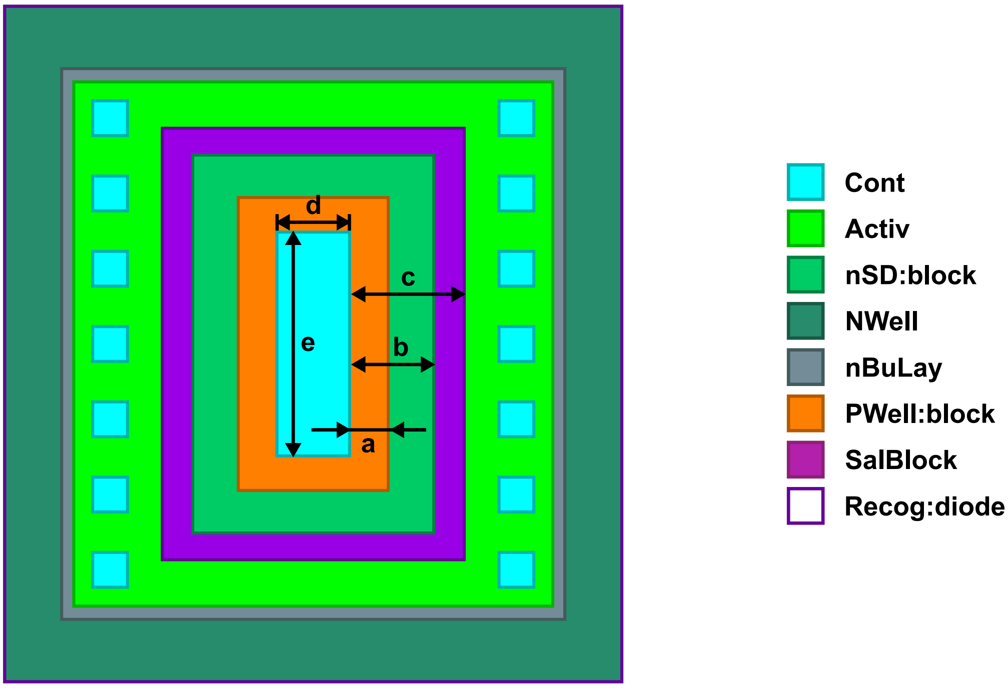

Figure 6.7: schottky_nbl1 dimensions.

6.8 ESD Protection Devices

For ESD protection of the chip, special clamp devices are provided. Please refer to the ESD documents for details about protection level. Also note that it is recommended to have I/O MOS devices with channel length of at least 0.36 µm.

6.8.1 nmoscl_2

Clamp device for limiting supply voltage.

Device recognition: nmoscl_2 = TEXT “nmoscl_2” within **Recog:esd**

Following rules do not apply: nmosi.e, Gat.a3

6.8.2 nmoscl_4

Clamp device for limiting supply voltage.

Device recognition: nmoscl_4 = TEXT “nmoscl_4” within **Recog:esd**

Following rules do not apply: nmosi.e, Gat.a3

6.8.3 scr1

Device recognition: scr1 = TEXT “scr1” within **Recog:esd**

Following rules do not apply: nmosi.c, nmosi.g, LU.d, Gat.a

6.9 Pad Dimensions

Device recognition: Pad = (**Passiv** + **Passiv:sbump** + **Passiv:pillar**) + **dfpad**

Pad rules are tested only within **dfpad** recognition layer. Pad rules are only tested on metal structures which are on same net as **TopMetal2**. The following design rules must be also applied to solder bump pads and Cu pillar pads.

Rule	Description	Value
Pad.aR	Min. recommended **Pad** width	**30.00**
Pad.a1	Max. **Pad** width	**150.00**
Pad.bR	Min. recommended **Pad** space	**8.40**
Pad.d	Min. **Pad** space to **EdgeSeal**	**7.50**
Pad.dR	Min. recommended **Pad** to **EdgeSeal** space (Note 1)	**25.00**
Pad.d1R	Min. recommended **Pad** to **Activ** (inside chip area) space	**11.20**
Pad.eR	Min. recommended **Metal(n)**, **TopMetal1**, **TopMetal2** exit width	**7.00**
Pad.fR	Min. recommended **Metal(n)**, **TopMetal1**, **TopMetal2** exit length	**7.00**
Pad.gR	**TopMetal1** (within **dfpad**) enclosure of **TopVia2**	**1.40**
Pad.i	**dfpad** without **TopMetal2** not allowed	
Pad.jR	No devices under **Pad** allowed (Note 2)	
Pad.kR	**TopVia2** under **Pad** not allowed (Note 3)	

Notes

1. Distance of **Pad** opening to **EdgeSeal** strongly depends on bonding procedure. For flip chip bonding via solder bumps (see section 6.9.1) or copper pillars (see section 6.9.2) or manual bonding a bigger distance may be required. We strongly recommend 25 µm distance for wedge-wedge wire bonding.
2. Components under pads can be damaged by mechanical stress.
3. **TopVia2** may be damaged during packaging process, we recommend not to use them below **Passiv**.

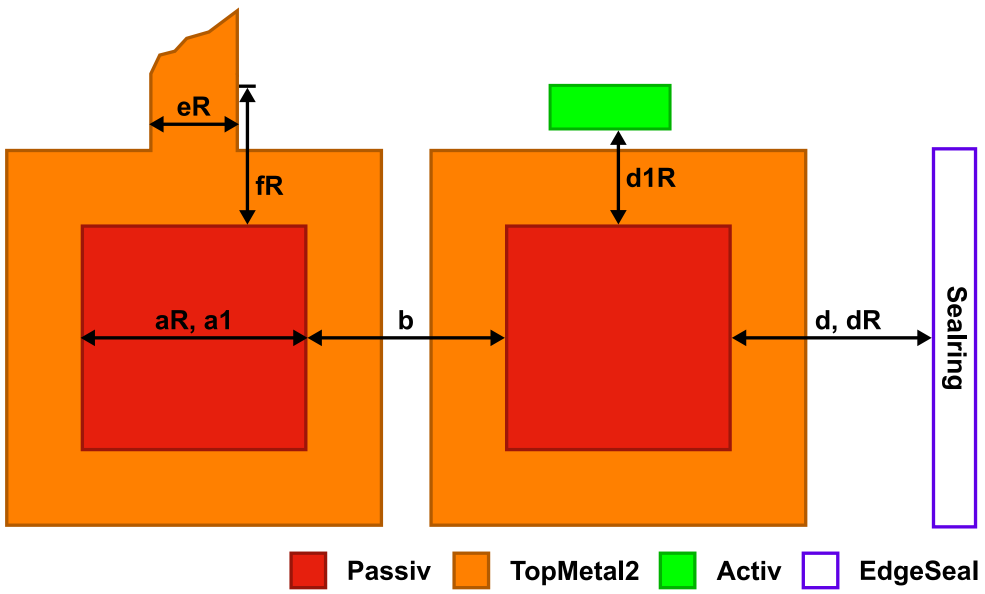

Figure 6.8: Pad dimensions.

6.9.1 Solder Bump Rules

These rules are valid within pads used for solder bumping and flip chip assembling. These pad rules are valid for 60 µm passive opening and 80 µm bump ball size. Bump ball standard is PacTech SAC305 (SnAgCu).

We recommend to use Solder Bump option in Pcell provided in the PDK.

For different geometries refer to design rule manual of our partner PacTech or the design rule manual of your specific bumping provider.

Device recognition: SBumpPad = **Passiv:sbump** + **dfpad**

Rule	Description	Value
Padb.a	**SBumpPad** size	**60.00**
Padb.b	Min. **SBumpPad** space	**70.00**
Padb.c	Min. **TopMetal2** (within **dfpad**) enclosure of **SBumpPad**	**10.00**
Padb.d	Min. **SBumpPad** space to **EdgeSeal**	**50.00**
Padb.e	Min. **SBumpPad** pitch (Note 1)	**130.00**
Padb.f	Allowed passivation opening shape (Note 1)	**Octagon Circle**

Notes

1. Underlying **TopMetal2** may have a different shape. This rule is not checked during DRC.

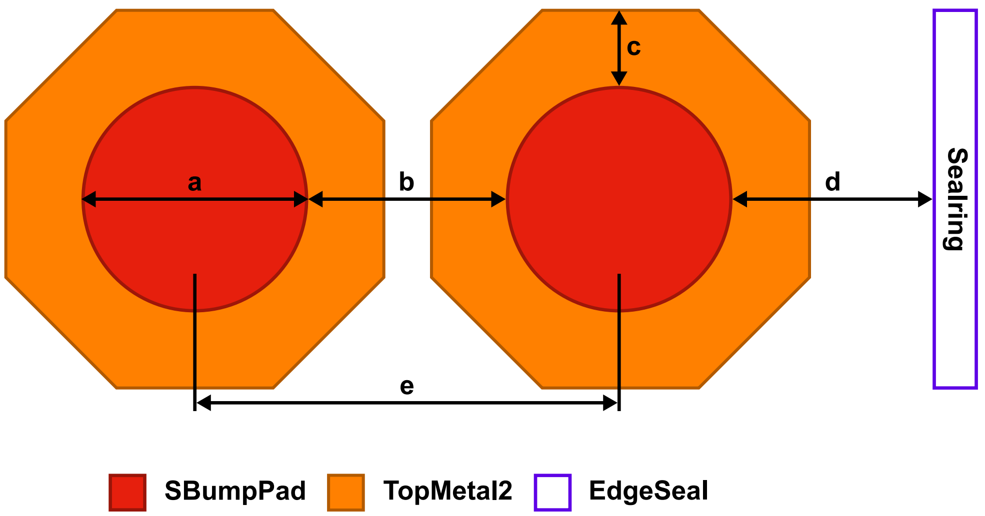

Figure 6.9: Pad dimensions for solder bumping process.

6.9.2 Copper Pillar Rules

These rules are valid within pads used for assembly with copper pillars. The given pad rules are valid for a number of different geometries offered by our partner PacTech given in table 6.1.

Important: Please note that pad opening may have an impact on final testing. If the passivation openings are too small, wafer-level testing may be prevented because the pad metal cannot be sufficiently contacted.

We recommend to use Solder Bump option in Pcell provided in the PDK.

Device recognition: CuPillarPad = **Passiv:pillar** + **dfpad**

* Thickness of optional SnAg cap after reflow at peak temp 260 degree C would be higher than that of after plating/ before reflow in the factor of 1.4 - 1.7, depending on the SnAg height as well.

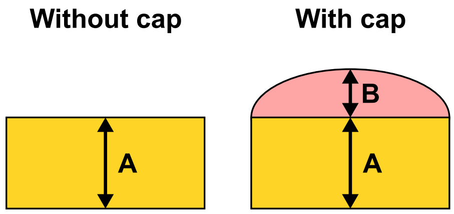

Figure 6.10: Copper pillar layer stack with and without optional SnAg cap.

For different geometries than listed in table 6.1, refer to the design rule manual of our partner PacTech or the design rule manual of your specific bumping provider.

The following table defines design rules for PacTech's copper pillar option with minimum passivation opening, copper pillar height and copper pillar pitch.

Table 6.1: Valid pad geometries and design rules for Cu pillars.

Passiv opening	35	40	45	**Padc.a**
Opening spacing	40	40	50	**Padc.b**
Opening enclosure	7.5	7.5	7.5	**Padc.c**
CuPillarPad pitch	75	80	95	**Padc.e**
Cu pillar height	50 ± 7	55 ± 7	65 ± 7	
Cu pillar diameter	44 ± 3	49 ± 3	54 ± 3	
Cu height (A)	28 ± 2	32 ± 2	42 ± 2	
SnAg height* (B)	16 ± 1	16 ± 1	19 ± 2	

Notes

1. Passivation openings highlighted in **green** are suited for on-wafer measurements
2. Pads with passivation openings of 45 µm and 55 µm are suited for PCB applications. Minimum recommended pitch 250 µm; recommended standard pitch 500 µm.

Rule	Description	Value
Padc.a	**CuPillarPad** size	**Table 6.1**
Padc.b	Min. **CuPillarPad** space	**Table 6.1**
Padc.c	Min. **TopMetal2** (within **dfpad**) enclosure of **CuPillarPad**	**Table 6.1**
Padc.d	Min. **CuPillarPad** space to **EdgeSeal**	**30.00**
Padc.e	Min. **CuPillarPad** pitch (Note 1)	**Table 6.1**
Padc.f	Allowed passivation opening shape (Note 1)	**Circle**

Notes

1. Underlying **TopMetal2** may have a different shape. This rule is not checked during DRC.

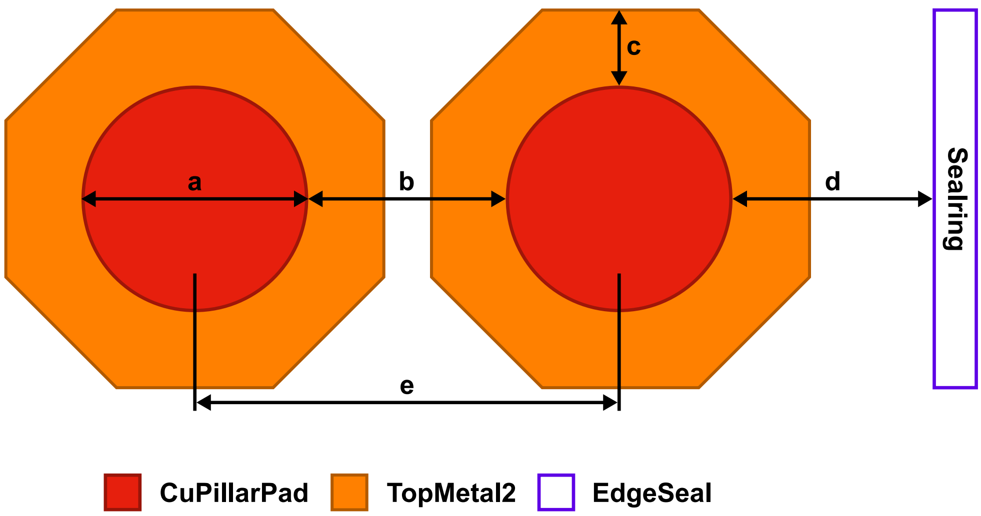

Figure 6.11: Pad dimensions for copper pillar process.

6.10 Sealring

A sealring is an uninterrupted ring of metal and via layers. The purpose of the sealring is to reduce the effects of mechanical stress on the circuit that occurs during dicing of various chips. The sealring must be enclosed by an unbrokend ring of **Passiv**. Figure 6.12 shows distance between **EdgeSeal** and the sealring boundary (30 µm) and the passivation opening. Please be aware that corresponding standard metal and via rules are not checked within **EdgeSeal** regions.

Device recognition: EdgeSeal

Rule	Description	Value
Seal.a	Min. **EdgeSeal-Activ**, **EdgeSeal-pSD**, **EdgeSeal-Metal(n=1-5)**, **EdgeSeal-TopMetal1**, **EdgeSeal-TopMetal2** width	**3.50**
Seal.b	Min. **Activ** space to **EdgeSeal-Activ**, **EdgeSeal-pSD**, **EdgeSeal-Metal(n=1-5)**, **EdgeSeal-TopMetal1**, **EdgeSeal-TopMetal2**	**4.90**
Seal.c	**EdgeSeal-Cont** ring width	**0.16**
Seal.c1	**EdgeSeal-Via(n=1-4)** ring width	**0.19**
Seal.c2	**EdgeSeal-TopVia1** ring width	**0.42**
Seal.c3	**EdgeSeal-TopVia2** ring width	**0.90**
Seal.d	Min. **EdgeSeal-Activ** enclosure of **EdgeSeal-Cont**, **EdgeSeal-Metal(n=1-5)**, **EdgeSeal-TopMetal1**, **EdgeSeal-TopMetal2** ring	**1.30**
Seal.e	Min. **Passiv** ring width outside of sealring	**4.20**
Seal.f	Min. **Passiv** ring outside of sealring space to **EdgeSeal-Activ**, **EdgeSeal-Metal(n=1-5)**, **EdgeSeal-TopMetal1**, **EdgeSeal-TopMetal2**	**1.00**
Seal.k	Min. **EdgeSeal** 45-degree corner length (Note 1)	**21.00**
Seal.l	No structures outside sealring boundary allowed	
Seal.m	Only one sealring per chip allowed (Note 1)	

Notes

1. Not checked during DRC

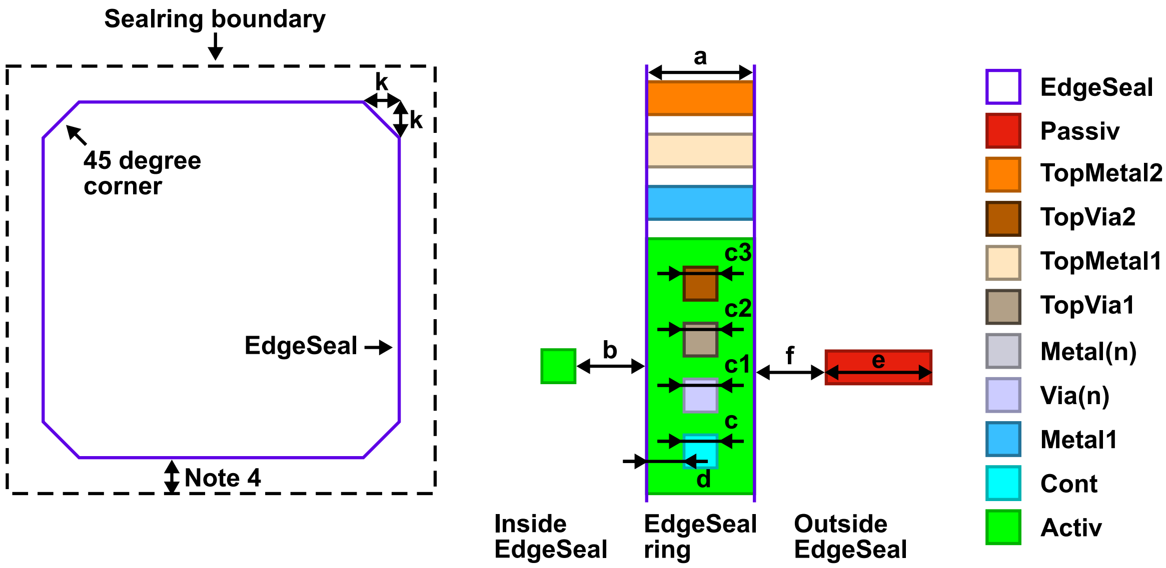

Figure 6.12: EdgeSeal and Sealring dimensions.

6.11 MIM

Metal-Insulator-Metal (MIM) capacitors are formed by a thin dielectric layer and conductor placed between **Metal5**, **TopVia1** and **TopMetal1**.

Within **MIM** capacitor layer **Vmim** can be used instead of **TopVia1**. Some EDA tools cannot distinguish between interconnects and electrical components which are formed by the same conductive layers. Within the MIM device, **TopVia1** can be replaced with **Vmim** to prevent false short circuit detection.

Device recognition: MIM capacitor = **MIM** + **Metal5**

Rule	Description	Value
MIM.a	Min. **MIM** width	**1.14**
MIM.b	Min. **MIM** space	**0.60**
MIM.c	Min. **Metal5** enclosure of **MIM**	**0.60**
MIM.d	Min. **MIM** enclosure of **TopVia1**	**0.36**
MIM.e	Min. **TopMetal1** space to **MIM**	**0.60**
MIM.f	Min. **MIM** area per MIM device (µm²)	**1.30**
MIM.g	Max. **MIM** area per MIM device (µm²)	**5625.00**
MIM.gR	Max. recommended total **MIM** area per chip (µm²)	**174800.00**
MIM.h	**TopVia1** must be over **MIM**	

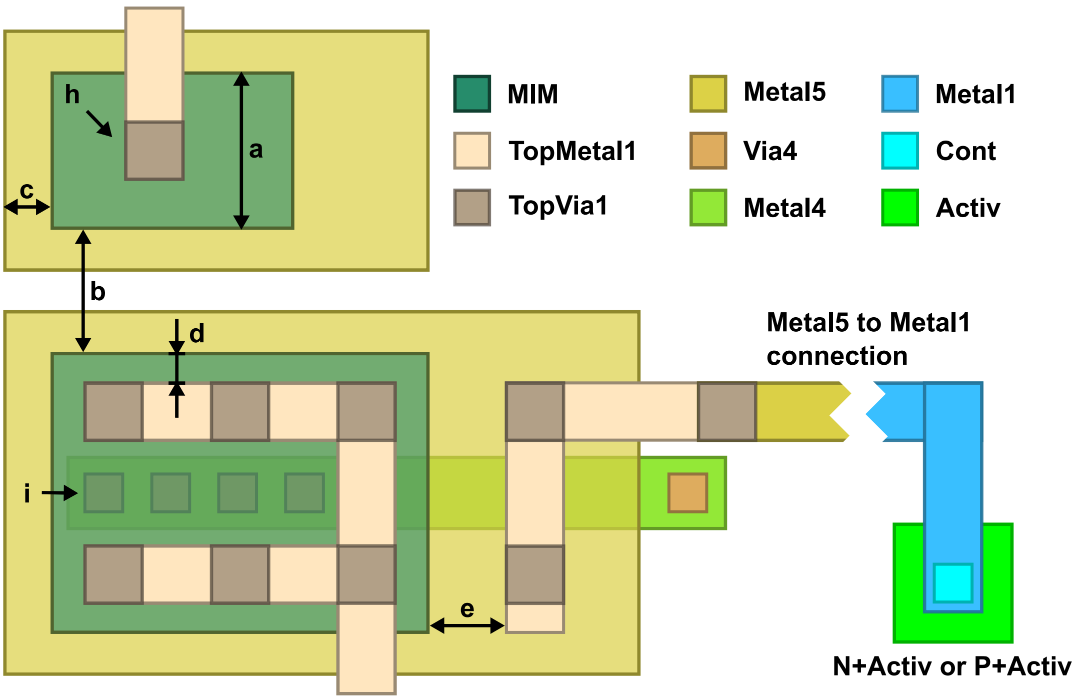

Figure 6.13: MIM dimensions

6.12 Inductors

In order to verify a custom inductor in the LVS check, additional layers must be added to the actual inductor layout (see Fig. 6.14). The inductor must be completely enclosed by the **IND** layer. To define the connection points, rectangles in layer **IND:pin** must be placed on the inductor metal. The connection points must touch the edge of the **IND** layer and contain a pre-defined text label in layer **IND:text**. These text labels are ”LA” and ”LB” for inductors with two connections or ”LA”, ”LB” and ”LC” for inductors with three connections.

Parasitic extraction of metal lines is excluded from inductors defined by this procedure. Within this layer there is by default no filler generation.

Following rules will not be checked within this layer: metal slit rules, AFil.g2, MFil.h, TM2.bR

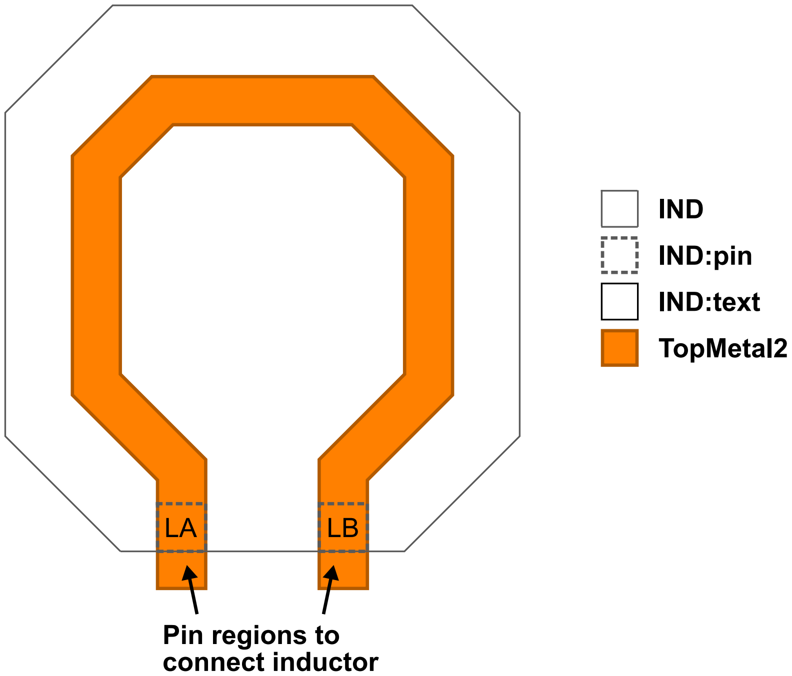

Figure 6.14: Custom inductor connection method.

7 Special Rules

7.1 Antenna Rules

The antenna effect occurs when metal layers on a chip are etched during the semiconductor manufacturing process. As the metal layers are etched, the remaining metal traces collect charge during the etching process. When these metal traces discharge, it can lead to damage or unwanted changes in the properties of the connected devices.

The design rules related to unprotected devices are determined by using gate leakage current (shift of 10 % for nominal devices) as failure criterion.

Antenna Rules are not checked by default. Antenna rule checking must be switched on separately.

Rule	Description	Value
Ant.a	Max. ratio of **GatPoly** over field oxide area to connected **Gate** area	**200.00**
Ant.b	Max. ratio of cumulative metal area (from **Metal1** to **TopMetal2**) to connected **Gate** area (without protection diode)	**200.00**
Ant.c	Max. ratio of **Cont** area to connected **Gate** area	**20.00**
Ant.d	Max. ratio of cumulative via area (from **Via1** to **TopVia2**) to connected **Gate** area (without protection diode)	**20.00**
Ant.e	Max. ratio of cumulative metal area (from **Metal1** to **TopMetal2**) to connected **Gate** area (with protection diode)	**20000.00**
Ant.f	Max. ratio of cumulative via area (from **Via1** to **TopVia2**) to connected **Gate** area (with protection diode)	**500.00**
Ant.g	Size of protection diode (μm²) (Note 4)	**0.16**

Notes

1. The rules apply for both types of oxide.
2. Vn_area = cumulative area Cont, Via1 to TopVia2
3. Via_area = cumulative area Via1 to TopVia2
4. PDarea (μm²) = 0.02 x (Vn_area / (GatPoly over Activ)_area)

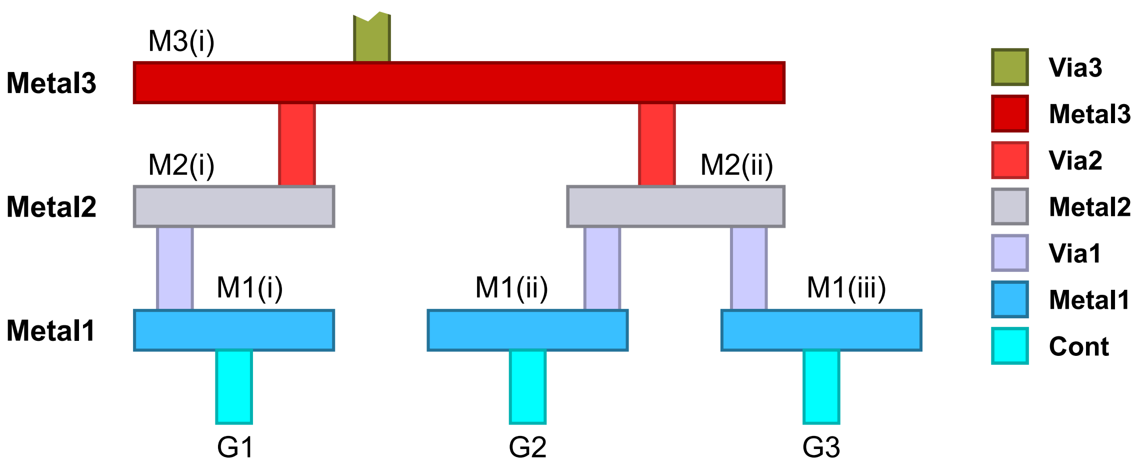

Figure 7.1: Cumulated area ratio calculation example.

$$\text{AreaRatio}\,(\text{G1}) = \frac{\text{Area}\{\text{M1}\,(\text{i})\} + \text{Area}\{\text{M2}\,(\text{i})\}}{\text{Area}\{\text{G1}\}} + \frac{\text{Area}\{\text{M3}\,(\text{i})\}}{\text{Area}\{\text{G1}\} + \text{Area}\{\text{G2}\} + \text{Area}\{\text{G3}\}}$$

$$\text{AreaRatio}\,(\text{G2}) = \frac{\text{Area}\{\text{M1}\,(\text{ii})\}}{\text{Area}\{\text{G2}\}} + \frac{\text{Area}\{\text{M2}\,(\text{ii})\}}{\text{Area}\{\text{G2}\} + \text{Area}\{\text{G3}\}} + \frac{\text{Area}\{\text{M3}\,(\text{i})\}}{\text{Area}\{\text{G1}\} + \text{Area}\{\text{G2}\} + \text{Area}\{\text{G3}\}}$$

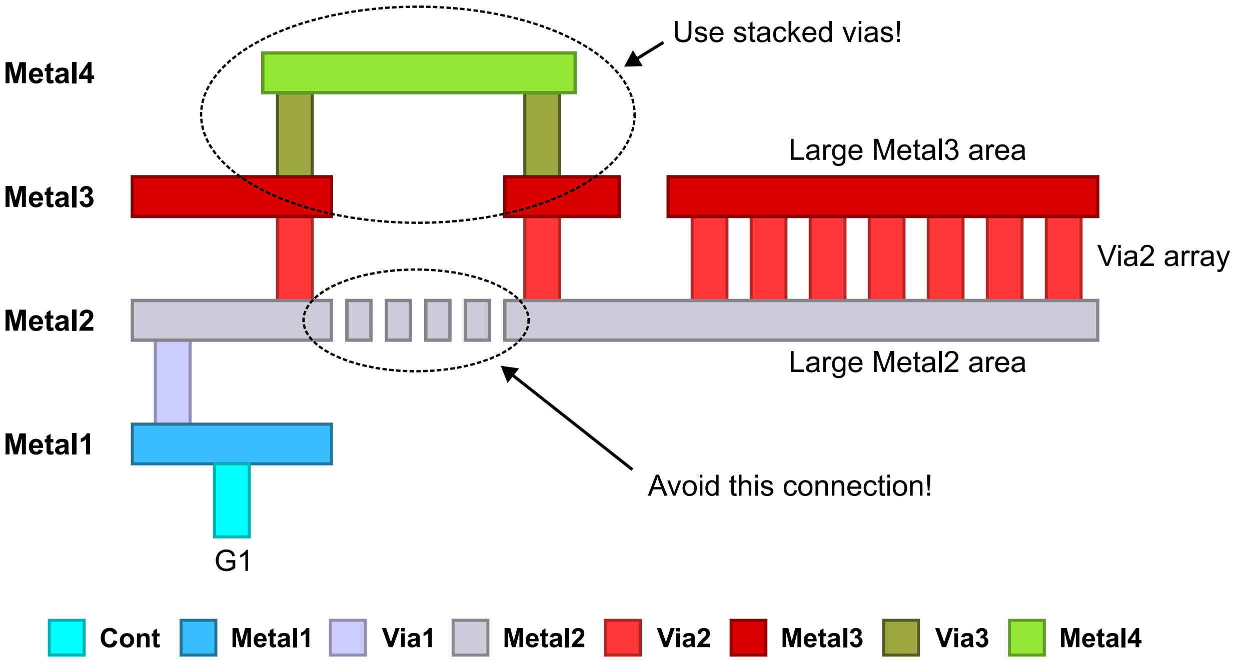

Figure 7.2: Usage of stacked vias to avoid antenna area ratio violations. Please note that this figure is only an example. The stacked via method can be applied up to **TopMetal2**.

Recommendations

- To get DRC clean layouts it is recommended to connect the antenna node to the output of the driver at low metal level to reduce the antenna area or connect the antenna node to a diode.
- To get DRC clean layouts it is recommended to use stacked vias to connect large metal or via areas as shown in Fig. 7.2.
- To protect the gate of an isolated nMOS transistors it is recommended to place the antenna-protection diode in a separate (non isolated) p-body region.
- For applications which are especially sensitive to V_t variation or mismatch (sense amplifers, certain analog circuits, etc.), each gate should be tied directly to an nSD/PWell or pSD/NWell diode in Metal1.

7.2 Latch-up Guidelines

Latch-up is an undesirable phenomenon in integrated circuit (IC) design that can lead to the inadvertent creation of a low-impedance path between the power supply rails or any other regions forming a parasitic thyristor. The effect is trigged by unwated injection of charges into this structure. This can lead to destruction of circuit parts due to overcurrent.

Latch-up rules are not checked by default. Latch-up rule checking must be switched on separately.

7.2.1 Latch-up Protection on Output Buffers

1. Connect source of NMOS and PMOS devices to VSS and VDD, respectively.
2. Connect drain of NMOS and PMOS devices directly to the output pad.
3. Place guard rings (VSS, VDD ties) around any NMOS and PMOS devices, which are directly tied to a pad.
4. Double guard rings (N-Well isolator and P+ isolator) should be inserted between n-channel and p-channel output buffers.
5. Double guard rings (N-Well isolator and P+ isolator) should be inserted between output buffers and internal circuit area.

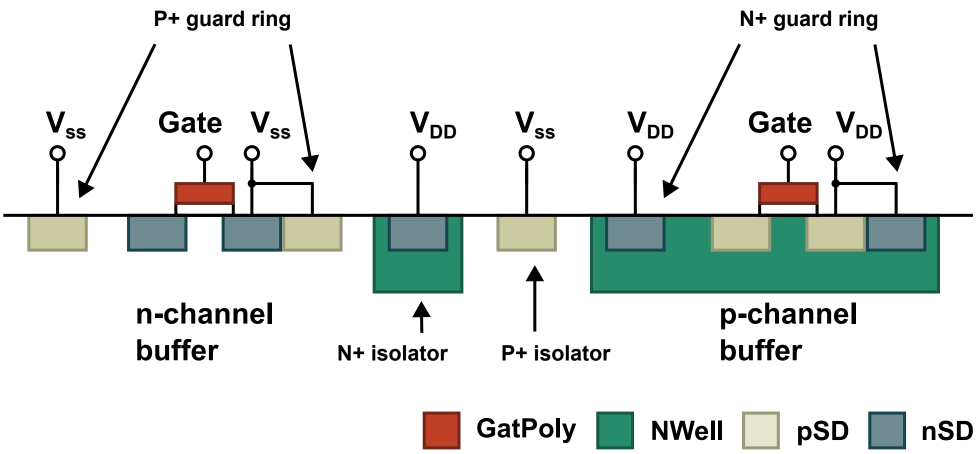

Figure 7.3: I/O latch-up protection scheme.

7.2.2 Additional Rules for Subtrate and NWell Ties

Rule	Description	Value
LU.a	Max. space from any portion of **P+Activ** inside **NWell** to an **nSD-NWell** tie	**20.00**
LU.b	Max. space from any portion of **N+Activ** inside **PWell** to an **pSD-PWell** tie	**20.00**
LU.c	Max. extension of an abutted **NWell** tie beyond **Cont**	**6.00**
LU.c1	Max. extension of an abutted substrate tie beyond **Cont**	**6.00**
LU.d	Max. extension of **NWell** tie **Activ** tie beyond **Cont**	**6.00**
LU.d1	Max. extension of an substrate tie **Activ** beyond **Cont**	**6.00**

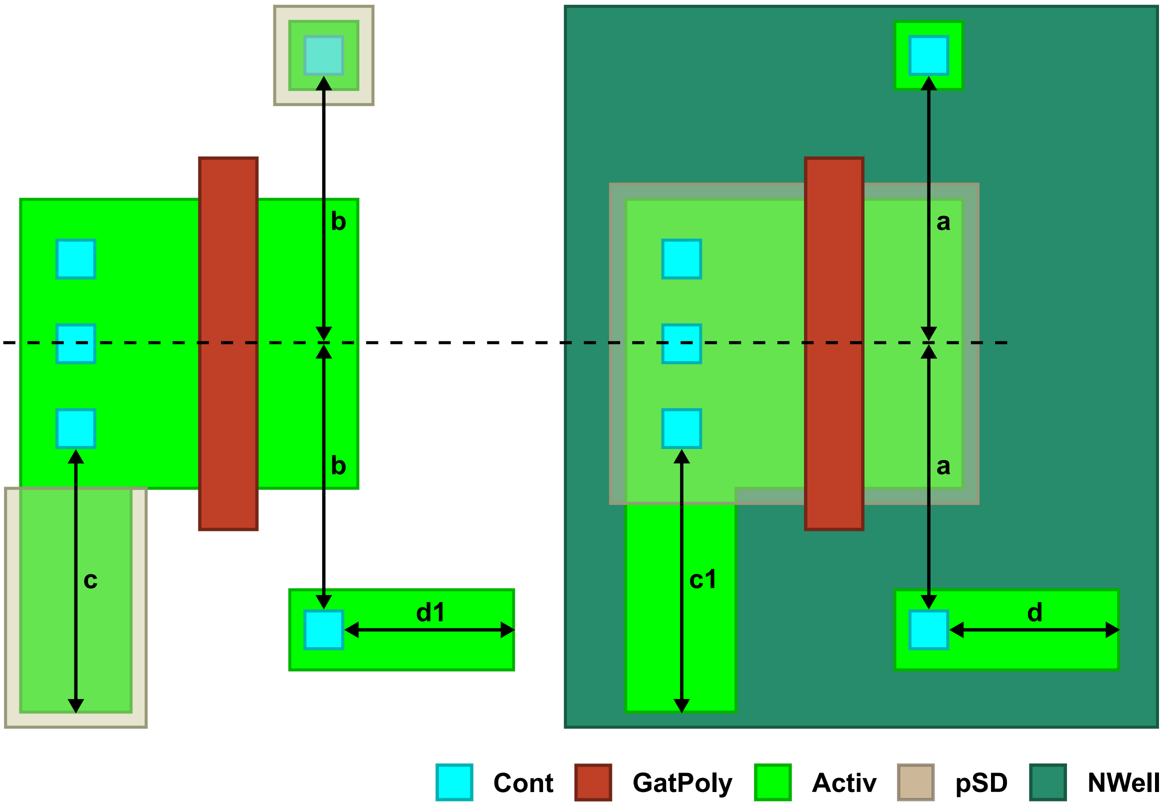

Figure 7.4: Latch-up protection rules.

7.3 Metal Slits

Large areas of metal are subject to mechanical stress during production. This can cause metal detachment from the oxide. The use of metal slits leads to reduction of mechanical stress.

Metal stands for all metal layers (**Metal(n=1-5)**, **TopMetal1** and **TopMetal2**).
Metal = **Metal(n=1-5)** + **TopMetal1** + **TopMetal2**

Rule	Description	Value
Slt.a	Min. **Metal:slit** width	**2.80**
Slt.b	Max. **Metal:slit** width	**20.00**
Slt.c	Max. **Metal** width without requiring a slit	**30.00**
Slt.e	No slits required on bond pads	
Slt.e1	No slits required on **MIM**	
Slt.f	Min. **Metal** enclosure of **Metal:slit**	**1.00**
Slt.g	Min. **Metal5:slit** and **TopMetal1:slit** space to **MIM**	**0.60**
Slt.h1	Min. **Metal1:slit** space to **Cont** and **Via1**	**0.30**
Slt.h2	Min. **Metal(n):slit** space to **Via(n-1)** and **Via(n)**	**0.30**
Slt.h3	Min. **TopMetal1:slit** space to **TopVia1** and **TopVia2**	**1.00**
Slt.h4	Min. **TopMetal2:slit** space to **TopVia2**	**1.00**
Slt.i	Min. **Metal:slit** density for any **Metal** plate bigger than 35 µm x 35 µm [%]	**6.00**

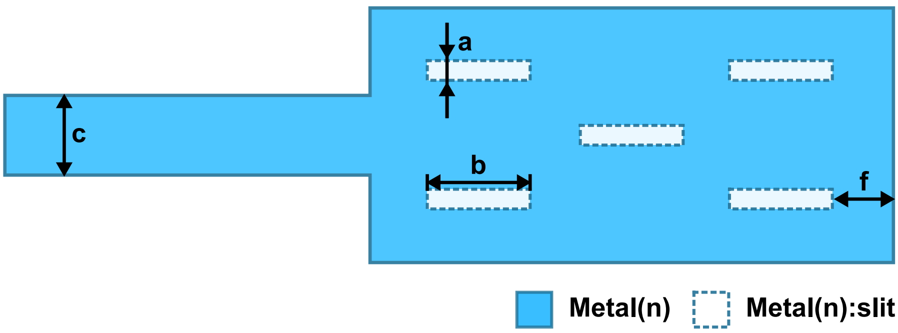

Figure 7.5: Metal slits dimensions.

7.4 Pin Layer Rules

Circuit designers should use only drawing purpose 0 (data types) for layouts. Only exception is pin purpose 2 for symbolic pins. Data type 2 (purpose pin) is used for symbolic connectivity information. Pin areas must be fully covered by drawing. These rules are tested because pin areas are not used for mask generation and a potential issue due to false postive LVS matchs.

Rule	Description	Value
Pin.a	Min. **Activ** enclosure of **Activ:pin**	**0.00**
Pin.b	Min. **GatPoly** enclosure of **GatPoly:pin**	**0.00**
Pin.e	Min. **Metal1** enclosure of **Metal1:pin**	**0.00**
Pin.f	Min. **Metal(n=2-5)** enclosure of **Metal(n=2-5):pin**	**0.00**
Pin.g	Min. **TopMetal1** enclosure of **TopMetal1:pin**	**0.00**
Pin.h	Min. **TopMetal2** enclosure of **TopMetal2:pin**	**0.00**

8 Rules of Digital Design

8.1 DigiBnd Layer

Digital designs can be marked with the **DigiBnd** layer. This layer must be used when using IHP's standard digital libraries. **DigiBnd** must enclose the complete layout of the digital components. Within the **DigiBnd** layer the following design rules are changed compared to the analog flow.

8.1.1 NWell

Refer to section 5.1 for NWell standard rule definitions.

Rule	Description	Value
NW.c1	Min. **NWell** enclosure of **P+Activ** inside **ThickGateOx**	**0.31**
NW.d1	Min. **NWell** space to external **N+Activ** inside **ThickGateOx**	**0.31**
NW.e1	Min. **NWell** enclosure of NWell tie surrounded entirely by **NWell** in **N+Activ** inside **ThickGateOx**	**0.24**
NW.f1	Min. **NWell** space to substrate tie in **P+Activ** inside **ThickGateOx**	**0.24**

8.1.2 Cont

Refer to section 5.14 for Cont standard rule definitions.

Rule	Description	Value
Cnt.c	Min. **Activ** enclosure of **Cont**	**0.05**

8.1.3 nmosi and nmosiHV

Refer to section 6.5 for nmosi and nmosiHV standard rule definitions.

Rule	Description	Value
nmosi.e1	A separate Iso-PWell contact unabutted to a nmosi device is not allowed	**not used**
nmosi.e2	nmosi unabutted to an Iso-PWell-Activ tie is not allowed	**not used**

8.2 DigiSub Layer

The **DigiSub** layer is used to define an area of a layout in which substrate contacts are extracted as a short instead of a resistive component. It is assumed that the substrate in which the components are located has the same potential as the metal connections that are connected to the substrate contact. There is no voltage drop within the substrate.

8.3 SRAM Layer

SRAM cells can be marked with the **SRAM** layer. **SRAM** must enclose the complete layout of the SRAM components. Within the **SRAM** layer the following design rules are changed compared to the analog flow.

8.3.1 NWell

Refer to section 5.1 for NWell standard rule definitions.

Rule	Description	Value
NW.c	Min. **NWell** enclosure of **P+Activ** not inside **ThickGateOx**	**0.149**
NW.d	Min. **NWell** space to external **N+Activ** not inside **ThickGateOx**	**0.24**

8.3.2 Activ

Refer to section 5.5 for Activ standard rule definitions.

Rule	Description	Value
Act.c	Min. **Activ** drain/source extension	**0.189**

8.3.3 GatPoly

Refer to section 5.8 for GatPoly standard rule definitions.

Rule	Description	Value
Gat.a	Min. **GatPoly** width	**0.069**
Gat.b	Min. **GatPoly** space or notch	**0.149**
Gat.c	Min. **GatPoly** extension over **Activ** (end cap)	**0.079**
Gat.d	Min. **GatPoly** space to **Activ**	**0.029**

8.3.4 pSD

Refer to section 5.10 for pSD standard rule definitions.

Rule	Description	Value
pSD.e	Min. **pSD** overlap of **Activ** when forming abutted substrate tie	**0.28**
pSD.g	Min. **N+Activ** or **P+Activ** width when forming abutted tie	**0.15**
pSD.i	Min. **pSD** enclosure of PFET gate not inside **ThickGateOx**	**0.068**
pSD.j	Min. **pSD** space to NFET gate not inside **ThickGateOx**	**0.239**

8.3.5 Cont

Refer to section 5.14 for Cont standard rule definitions.

Rule	Description	Value
Cnt.c	Min. **Activ** enclosure of **Cont**	**0.006**
Cnt.d	Min. **GatPoly** enclosure of **Cont**	**0.009**
Cnt.f	Min. **Cont** on **Activ** space to **GatPoly**	**0.059**
Cnt.g2	Min. **pSD** overlap of **Cont** on **pSD-Activ**	**0.075**

8.3.6 Metal1

Refer to section 5.16 for Metal1 standard rule definitions.

Rule	Description	Value
M1.b	Min. **Metal1** space or notch	**0.159**
M1.c1	Min. **Metal1** endcap enclosure of **Cont**	**0.005**
M1.i	Min. space of **Metal1** lines of which at least one is bent by 45-degree	**0.18**

8.4 Metal(n=2-5)

Refer to section 5.17 for Metal(n=2-5) standard rule definitions.

Rule	Description	Value
M1.b	Min. **Metal(n)** space or notch	**0.169**
M1.c1	Min. **Metal(n)** endcap enclosure of **Via(n-1)**	**0.02**

8.5 Via1

Refer to section 5.19 for Via1 standard rule definitions.

Rule	Description	Value
V1.c1	Min. **Metal1** endcap enclosure of **Via1**	**0.005**

8.6 Via(n=2-4)

Refer to section 5.20 for Via(n=2-4) standard rule definitions.

Rule	Description	Value
Vn.c1	Min. **Metal(n)** endcap enclosure of **Via(n)**	**0.005**

9 Localized Backside Etching (LBE)

The backside etching module is not qualified and not yet tested under all conditions. The module is not available for SG13RH.

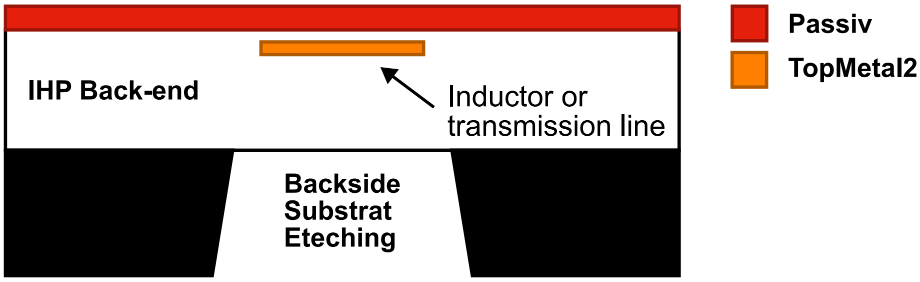

Figure 9.1: **LBE** cross-section.

Rule	Description	Value
LBE.a	Min. **LBE** width	**100.00**
LBE.b	Max. **LBE** width	**1500.00**
LBE.b1	Max. **LBE** area (μm²)	**250000.00**
LBE.b2	Min. **LBE** area (μm²)	**30000.00**
LBE.c	Min. **LBE** space or notch	**100.00**
LBE.d	Min. **LBE** space to inner edge of **EdgeSeal**	**150.00**
LBE.e	Min. **LBE** space to **dfpad** and **Passiv**	**50.00**
LBE.f	Min. **LBE** space to **Activ**	**30.00**
LBE.h	No **LBE** ring allowed	
LBE.i	Max. global **LBE** density [%]	**20.00**

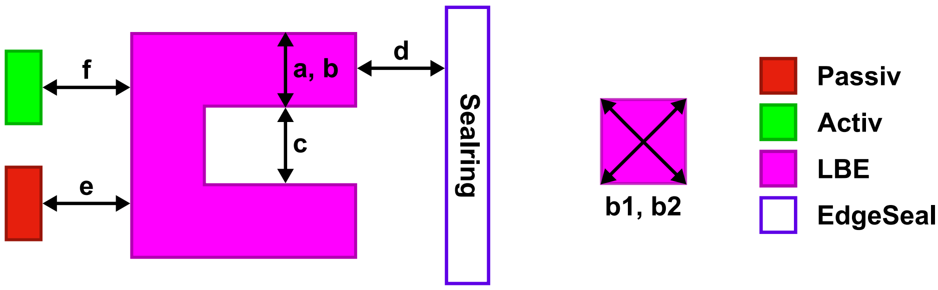

Figure 9.2: **LBE** dimensions.

10 Through-Silicon Via for Grounding (TSV_G)

The TSV_G module is not qualified and not yet tested under all conditions. Please note that wafers processed at IHP have full backside metallization.

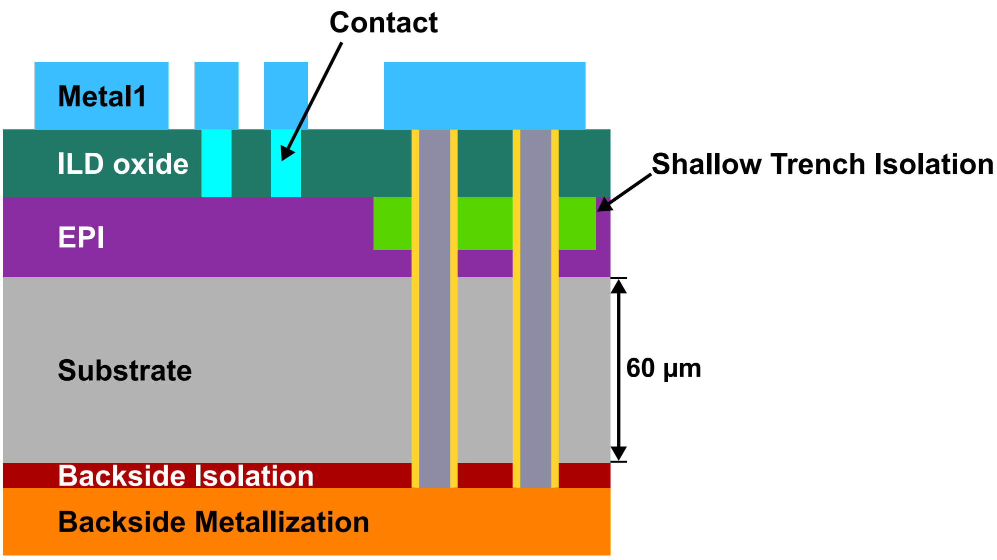

Figure 10.1: TSV module cross-section.

Areas with etched TSV ring are recognized by the **DeepVia** layer. No grid check is performed on layer **DeepVia**.

Rule	Description	Value
TSV_G.a	**DeepVia** has to be a ring structure	
TSV_G.b	Min. and max. **DeepVia** width	**3.00**
TSV_G.c	**DeepVia** ring diameter	**25.00**
TSV_G.d	Min. **DeepVia** space	**25.00**
TSV_G.e	Min. **DeepVia** space to **Activ**, **Activ:filler**, **GatPoly**, **GatPoly:filler** and **Cont**	**5.00**
TSV_G.f	Min. **PWell:block** enclosure of **DeepVia**	**2.50**
TSV_G.g	Min. **Metal1** enclosure of **DeepVia** ring structure	**1.50**
TSV_G.i	Max. global **DeepVia** density [%]	**1.00**
TSV_G.j	Max. **DeepVia** coverage ratio for any 500.0 x 500.0 µm² chip area [%]	**10.00**

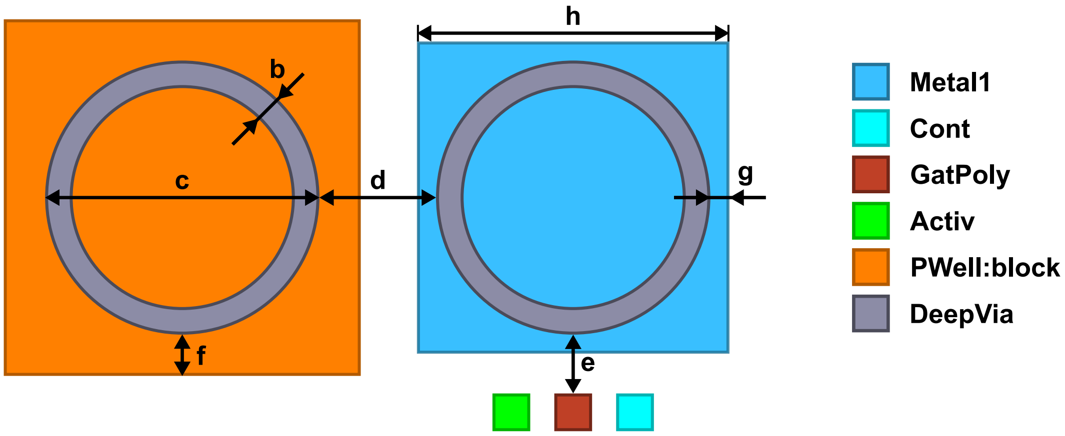

Figure 10.2: TSV dimensions.

11 Change history

Revision	Date	Changes
Rev. 0.1	2023-04-20	Initial revision
Rev. 0.2	2024-03-08	Document structure completely revised Add missing figures to rule sections Chapter 2: Add layer isoNWell to 257:0 Chapter 3: Add chapter "General Requirements" Chapter 3.2: Add NoDRC Chapter 4: Add chapter "Terminology" Chapter 4.2: Add introduction text, add PWell, nBuLay and Gate descriptions Chapter 5.1: Update NW.c, NW.c1, NW.d, NW.d1, NW.e, NW.e1, NW.f, NW.f1 rule descriptions, remove (old) note 3, update (old) note 4 Chapter 5.2: Update PWB.e, PWB.e1, PWB.f, PWB.f1 rule descriptions Chapter 5.3: Update introduction text, update note 1, remove note 2 Chapter 5.4: Remove note 1, move note 2 into introduction text Chapter 5.6: Remove note 2, change AFil.b to 0.42 Chapter 5.8: Move GatPoly:filler part of Gat.c to (new) GFil.j, update Gat.g description Chapter 5.9: Remove (old) Gat.j, move GatPoly:filler part of Gat.c to (new) GFil.j, remove note 2 Chapter 5.10: Add introduction text Chapter 5.14: Add introduction text Chapter 5.15: Update introduction text Chapter 5.18: Remove note 3, update note 2 text, change MFil.b to 0.42 Chapter 5.23: Add introduction text, remove note 1 Chapter 5.26: Add introduction text, remove note 1 Chapter 6.4: Update note 1 Chapter 6.6: Update introduction text, remove table containing pcell parameters Chapter 6.9: Update introduction text, update note 1 Chapter 6.9.1: Merge note 1 und note 3, move note 1 to introduction text Chapter 6.9.2: Merge note 1 und note 3, move note 1 to introduction text Chapter 6.10: Section renamed to "Sealring", update introduction text, remove note 2 and note 4, move note 1 to introduction text, add Seal.m, update Seal.e and Seal.f descriptions Chapter 6.11: Remove MIM.i, remove "Yield Enhancement Guideline" Chapter 6.12: Rename section to "Inductors", add explanation of the connection method, add Fig. 6.14, fix waived design rules Chapter 7: Remove section "Layer generation" (overview of generated layers can be found in section 4.2), remove section "NoDRC", move sections "Grid Rules" and "Forbidden Layers" to chapter 3 Chapter 7.1: Move note 1 to introduction text Chapter 7.2: Add introduction text, change LU.c1 description to "Max. extention of an abutted substrate tie beyond Cont" Chapter 7.3: Update introduction text

		Chapter 8.1: Update introduction text Chapter 8.1.1: Change to subsection of section 8.1, align description to original descriptions in section 5.1 Chapter 8.1.2: Change to subsection of section 8.1 Chapter 8.1.3: Change to subsection of section 8.1 Chapter 8.2: Update introduction text Chapter 8.3: Update introduction text Chapter 10: Remove TSV_G.h, update TSV_G.g description, update Fig. 10.1

12 Known issues