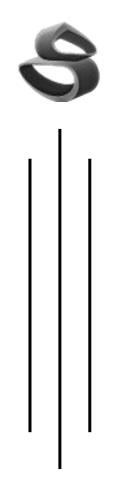
SAGARMATHA ENGINEERING COLLEGE

(TU Affiliated)

Sanepa, Lalitpur



LAB NO: 4

A LAB REPORT ON

SIMULATION OF 8085 PROGRAM USING VIRTUAL SIMULATOR KIT WITH TIMING WAVEFORM GENERATOR.

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Faculty/Year:	Department of Electronics and Computer Engineering
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Date:	

MICROPROCESSOR LAB-04

TITLE

SIMULATION OF 8085 PROGRAM USING VIRTUAL SIMULATOR KIT WITH TIMING WAVEFORM GENERATOR

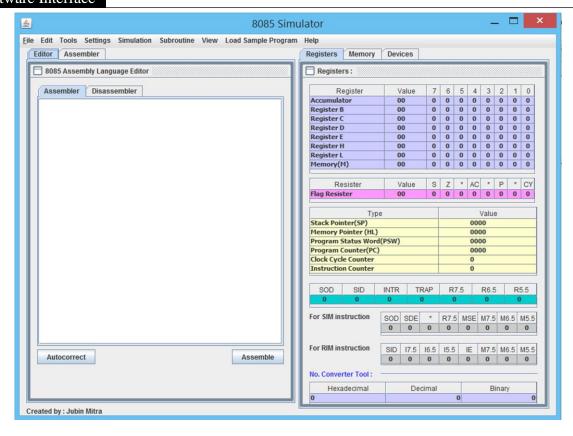
Objective

- ✓ To be able to simulate simple programs in 8085 virtual simulator kit.
- ✓ To be able to generate timing diagrams using the virtual simulator software.

Hardware/Software Required

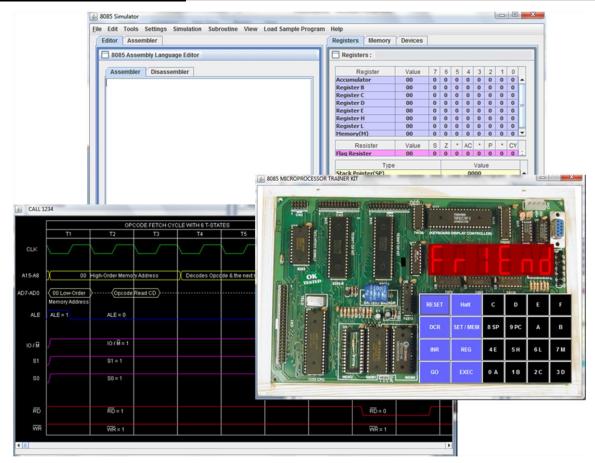
- Computer with internet
- 8085 virtual simulator

Software Interface



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Hardware/Software Required



Simulation using Kit

;Assume [C050H]=96H	PC
LDA C050H	
CMA	
STA C051H	
HLT	

Address	Value	Remarks
C050H		Manually loaded content
C000H		Op-code of LDA instruction
C001H		
C002H		
C003H		
C004H		
C005H		
C006H		
C007H		
C051H		

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Procedure

Table 7.1: Showing the buttons to be pressed sequentially to load the program in the memory

To load the Program			
STEP	1:	RESET	
STEP	2:	SET/MEM	
STEP	3:	C 0 0 0	
STEP	4:	INR	
STEP	5:	3 A	
STEP	6:	INR	
STEP	7:	$\begin{bmatrix} 5 \end{bmatrix} \begin{bmatrix} 0 \end{bmatrix}$	
STEP	8:	INR	
STEP	9:	C 0	
STEP	10:	\overline{INR}	
STEP	11:	2 F	
STEP	12:	INR	
STEP	13:	3 2	
STEP	14:	INR	
STEP	15:	5 1	
STEP	16:	INR	
STEP	17:	C 0	
STEP	18:	INR	
STEP	19:	7 6	
To l	oad a	value in C050	
STEP	20:	SET/MEM	
STEP	21:	C050	
STEP	22:	INR	
STEP	23:	96	

Table 7.2: Showing the buttons to be pressed for proper execution of the code

To begin execution			
STEP	1:	RESET	
STEP	2:	GO	
STEP	3:	$\begin{bmatrix} C & 0 & 0 & 0 \end{bmatrix}$	
STEP	4:	EXEC	

Dynamic Timing Diagram Generation

You need to click on the column named "T-states" of the currently highlighted row to generate timing diagram of that operation code (instruction).

Sanepa, Lalitpur

MICROPROCESSOR LAB-04

Problems

L1:

Q1. Assemble the following program and observe the output.

```
LXI SP,08FFH

CALL L1

MOV B, A

HLT

INR A
```

RET

Address	Value	Remarks
08FEH		
08FDH		
A		
В		

Also, generate the timing diagram of instruction **LXI SP**, 08FFH and attach the freehand drawing of the timing diagram along with the sheet.

- **Q2.** There are 12 bytes of data starting from 9000H. Transfer by complementing those data to location starting from 9010H.
- **Q3.** WAP to add upper and lower nibble of a data stored at 9000H, and store the final result at 9010H.
- **Q4.** WAP to transfer 8-bit data from one table to another by setting bit D_5 and resetting D_6 .
- **Q5.** Write a program to transfer 8-bit data from one table to another if there is even number of one else store zero.
- **Q6.** Sixteen-bit data are stored in two tables starting at 9000H and 9020H having ten data each. WAP to store the sum in the corresponding index of the third table starting at 9040H. Assume the sum will not exceed 16 bits.

Result

Hence, all the given programs are executed and the results are verified.