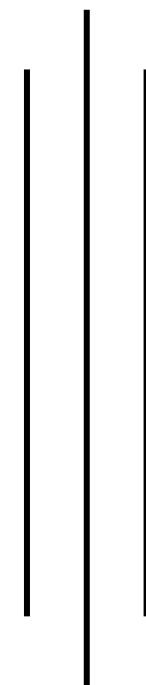


SAGARMATHA ENGINEERING COLLEGE

(TU Affiliated)

Sanepa, Lalitpur



LAB NO: 2

A LAB REPORT ON

OBSERVATION OF FLAGS & USE OF BRANCHING INSTRUCTIONS

Submitted By

Name:

Faculty/Year:

Roll No.:

Date:

Submitted To

Department of Electronics and Computer Engineering

Signature:

Date:

MICROPROCESSOR LAB-02

TITLE

OBSERVATION OF FLAGS & USE OF BRANCHING INSTRUCTIONS

Objective

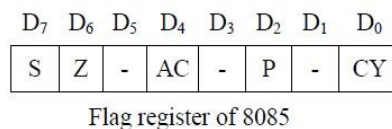
- ✓ To be familiar with the use of flag bits and branching instructions in 8085.
- ✓ To be able to implement loop in assembly for array and table processing.

Hardware/Software Required

- Computer with internet
- Sim8085 online simulator

Related Theory

Flags in 8085: Flag is a flip flop which indicates some condition produced by the execution of an instruction. The flag register of 8085 microprocessor consists of 5 flags. The flag register is connected to ALU. When an operation is performed by ALU the result is transferred to the accumulator and status of result will be stored in flip flops.



Branching Group Instructions: This instruction group branches the normal flow of execution and continues executing machine codes from new location.

- **Conditional Branching:** Program sequence branches only if some condition (*generally flag status*) is satisfied.
- **Unconditional Branching:** Program sequence branches to subroutine unconditionally (without checking any condition/flag status)

Machine Control Instructions: This instruction group controls machine functions such as halt.

**MICROPROCESSOR LAB-02****Code and Observations****Effect on Flags by Various Instructions**

Please fill up the result (*value of accumulator*) and flags after executing the following code line by line and give your reason why the flags are getting affected.

Please clear all flags before executing the instructions.

Mnemonics	A	Flag (Binary)	Reason
MVI C, FFH INR C			
LXI H, FFFFH INX H			
MVI A, FFH ANA 00H			
MVI A, 00H ANI AAH			
MVI A, F0H XRA A			
MVI A, FFH CMA			
MVI A, 01H CPI 02H			
MVI A, 01H CPI 01H			
MVI A, 80H			
RAL			
RAR			
RLC			
RRC			

Rough



MICROPROCESSOR LAB-02

Code and Observations

How Microprocessor Stores Instruction and How Branching Occurs?

<pre> ;Assume [9000H]=01H LDA 9000H JMP L1 MVI A, 55H NOP NOP L1: INR A STA 9000H HLT </pre>	PC	Address	Value	Remarks
		9000H		Manually loaded content
		0800H		Op-code of LDA instruction
		0801H		
		0802H		
		0803H		
		0804H		
		0805H		
		0806H		
		0807H		
		0808H		
		0809H		
		080AH		
		080BH		
		080CH		
		080DH		
		080EH		
		9000H		

JMP Vs CALL

<pre> LXI SP, 08FFH CALL L1 MVI A, FFH HLT L1: INR A RET </pre>	A	PC	Address	Value	Remarks
			08FEH		Initial Stack Value (Higher)
			08FDH		
			0800H		Op-code of LXI instruction
			0801H		
			0802H		
			0803H		
			0804H		
			0805H		
			0806H		
			0807H		
			0808H		
			0809H		
			080AH		
			080BH		
			A		

MICROPROCESSOR LAB-02

Code and Observations

LOOP Examples

	Itr.	A	Z	C
MVI C, 05H	1			
L1: INR A	2			
<i>;Looped Block</i>	3			
DCR C	4			
JNZ L1	5			
HLT	6			

Explanation

Observe and write the output for the following code.

[illegible]



MICROPROCESSOR LAB-02

Practice Questions

Q1. Write a program to multiply 05H and 03H and store result at 9000H.

Q2. Add numbers from one to fifty and store the 16 bit result at 9000H and 9001H.

Q3. Transfer 10 bytes of data from 9020 to 9030 if the data is greater than 7FH.

Result

Hence, All the given instructions are executed and the result is verified.