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TI Designs – Precision: Verified Design

High-Resolution, Low-Drift, Precision Weigh-Scale Reference Design with AC Bridge Excitation

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Circuit Description

This precision weigh-scale reference design achieves greater than 50,000 noise-free counts of resolution over a wide temperature range. Offset and offset drift errors are nearly eliminated by an ac-excited, ratiometrically measured resistor bridge. This design takes advantage of the high-resolution ADS1262 delta-sigma ADC.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
ADS1262	Product Folder
TS5A21366	Product Folder
MSP-EXP430F5529LP	Tool Folder

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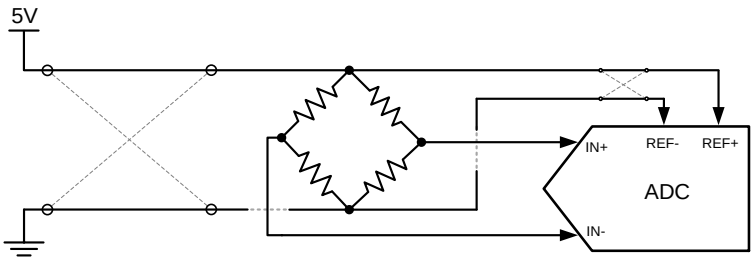

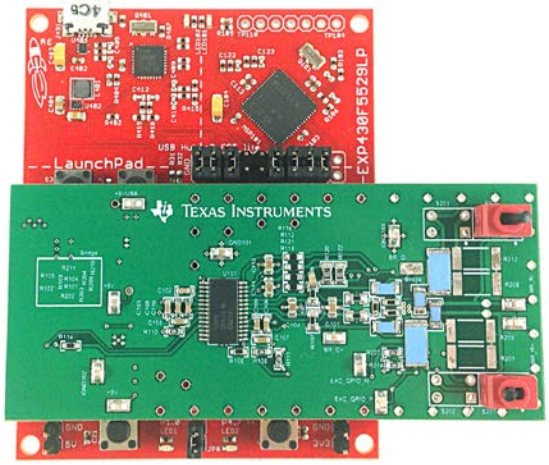

1 Design Summary

The design requirements are as follows:

- Bridge Sensitivity: 2 mV/V
- Bridge Excitation/Reference Voltage: 5 V
- Bridge Output Voltage: 0 - 10 mV
- Bridge Impedance: 350 Ω
- ADC Supply Voltage (AVDD): 5 V
- Temperature Range: -40°C to 125°C

The design goals and performance are summarized in Table 1.

Table 1. Comparison of Design Goals, and Measured Performance

AC Excitation Performance Parameters	Goal	Calculated	Measured
Temperature Dependent Error (@ Full-scale)	≤ 25 nV/ºC	10 nV/ºC	9.2 nV/ºC
Noise-Free Counts (@ 25ºC)	≥ 50,000	71,425	86,785

Figure 1 and Figure 2 show the total error over temperature and the achieved noise performance, for both dc- and ac-excited bridge implementations.

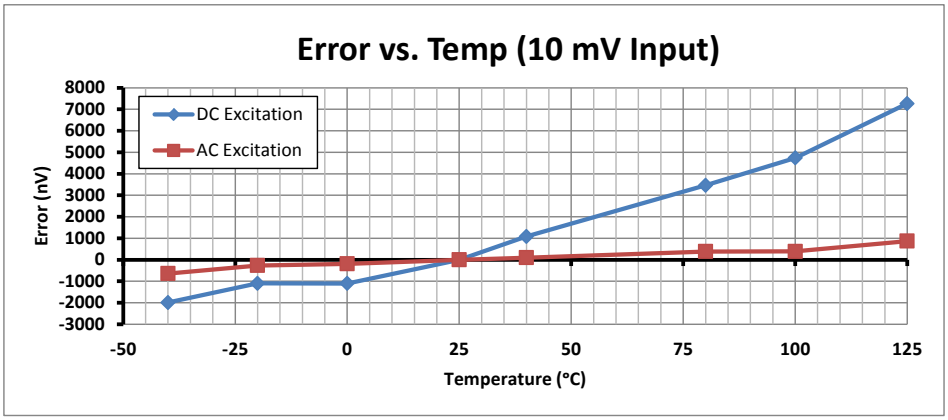

Figure 1: Measured Error across Temperature with Full-Scale Input

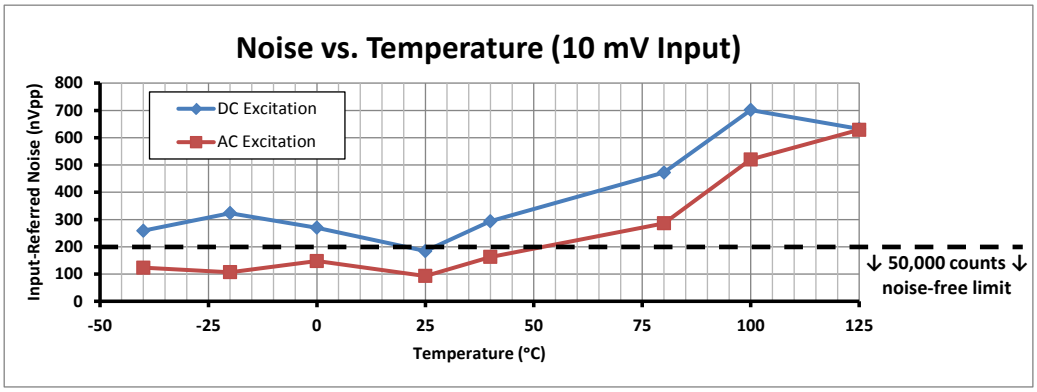

Figure 2: Measured Noise across Temperature with Full-Scale Input

2 Theory of Operation

2.1 Overview of Bridge Measurements

The most common technique to convert weight into an electrical signal is to use a resistive load cell configured as a Wheatstone bridge. In this configuration, one or more of the resistors change value in proportion to the load (weight) applied. To measure this effect, an excitation voltage (or current) source is applied across the top and bottom of the bridge and the output signal is measured as the differential voltage across the middle nodes, as shown in Figure 3.

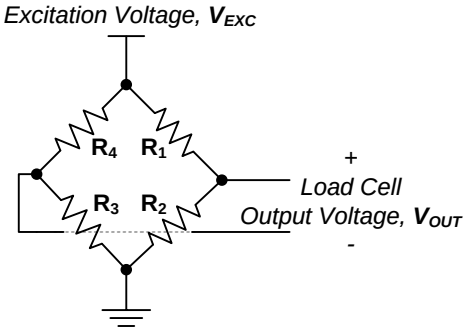

Figure 3: Wheatstone Bridge

In practice, load cells are specified with a known sensitivity (or rated output) and a rated capacity (maximum load). The sensitivity is specified by the ratio of the output voltage produced per 1-V excitation voltage (given in units of mV/V) with the rated capacity load applied. The full-scale output voltage of the load cell is then calculated by Equation 1.

$$V_{Bridge\_FS}(mV) = Sensitivity\ \left(\frac{mV}{V}\right) \cdot V_{EXC}(V) \quad (1)$$

For example, a 2 mV/V load cell excited with 5 V will have a full-scale output voltage of 10 mV. It is important to note that the magnitude of the output signal is directly proportional to the magnitude of the excitation voltage and applied load. In general, the output voltage for any other applied load will scale linearly from no load to the maximum load. (Bridge linearization techniques may be used increase the bridge linearity, but this topic is outside the scope of this TI Design).

2.1.1 Ratiometric Bridge Measurements

The voltage-excited bridge is connected to the ADC using a ratiometric connection, as shown in Figure 4.

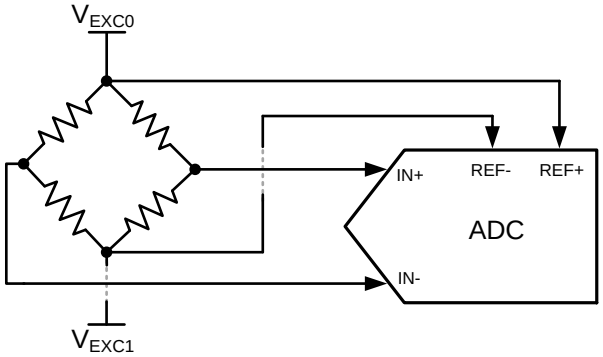

Figure 4: Ratiometric Bridge Configuration

NOTE: The excitation voltage ($V_{EXC} = V_{EXC0} – V_{EXC1}$) does not necessarily need to be referenced to ground. This allows for level-shifting of the bridge common-mode voltage.

In this configuration, the bridge excitation voltage is shared with the ADC's reference voltage. Any changes in the bridge excitation voltage, due to temperature drift or noise, will affect both the input signal and reference proportionately. Therefore, the ADC conversion results (codes) remain unaffected by changes in the excitation/reference voltage, as shown by Equation 2.

$$Code \propto \frac{V_{Bridge}}{V_{REF}} = \frac{(\%\ Rated\ Load) \cdot (Sensitivity) \cdot V_{REF}}{V_{REF}} = (\%\ Rated\ Load) \cdot (Sensitivity) \quad (2)$$

Another benefit of ratiometric bridge measurements is that reference noise is reduced because the reference noise is common to both the ADC and reference inputs. To the degree that the reference noise seen by the ADC input and reference terminals match, reference noise is ratiometrically removed from the ADC conversion results, as Equation 2 shows. Therefore, input and reference filters ought to be matched to provide the best reference noise rejection (discussed in SBAA201).

2.2 Input Chopping Overview

Chopping is a form of averaging that samples a differential input from both directions and averages the conversion results. Figure 5 shows the two phases of an ADC sampling a chopped input, with system offset voltages modelled as V_{OS1} and V_{OS2}.

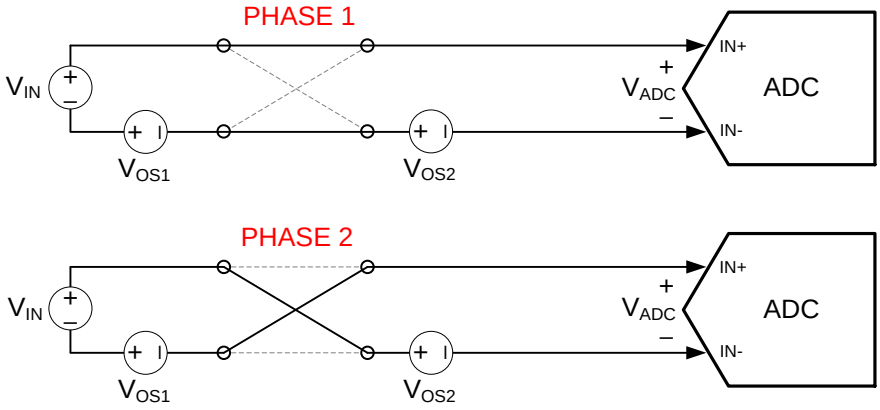

Figure 5: Input Chopping Concept

Many high-resolution ADCs, such as the ADS1262, integrate input chopping into the device to reduce the offset and offset drift of the ADC. By performing the chopping operation, any systematic offsets that occur *after* the chopping circuitry (primarily the ADC's offset) are removed, as shown by equation 3.

$$V_{ADC} = \frac{V_{ADC}(PHASE1) - V_{ADC}(PHASE2)}{2} = \frac{(V_{IN} + V_{OS1} + V_{OS2}) - (-V_{IN} - V_{OS1} + V_{OS2})}{2} = V_{IN} + V_{OS1} \quad (3)$$

Systematic offsets that occur *before* the input chopping circuitry (represented by V_{OS1}) are not removed by chopping. These offsets are seen as part of the differential input signal and are only removed by offset calibration. However, slowly changing offsets that occur *after* the chopping (represented by V_{OS2}) are dynamically removed.

NOTE: This design does not use the ADC's input chopping feature. This discussion is provided only to introduce the input chopping concept and how it works, as a prerequisite for understanding ac bridge excitation.

2.2.1 Overview of AC Bridge Excitation

AC bridge excitation is an extension of input chopping. While input chopping only reduces the offset and offset drift of the ADC; ac bridge excitation reduces the offset and offset drift of the whole measurement system. AC bridge excitation performs the same operation as ADC input chopping, but performs the chopping directly on the bridge sensor. Recalling the observation from Section 2.2 that offsets *after* the chopping stage are removed, it is then most beneficial to place the chopping circuitry as close to the sensor output as possible. By doing so, the measurement system's offset is almost completely removed from the measurement results.

AC bridge excitation does *not* excite the bridge with an actual ac signal (as the name would seem to imply). AC bridge excitation is performed by applying a *dc excitation* voltage to the bridge and *alternating* the polarity of the excitation voltage, as seen in Figure 6.

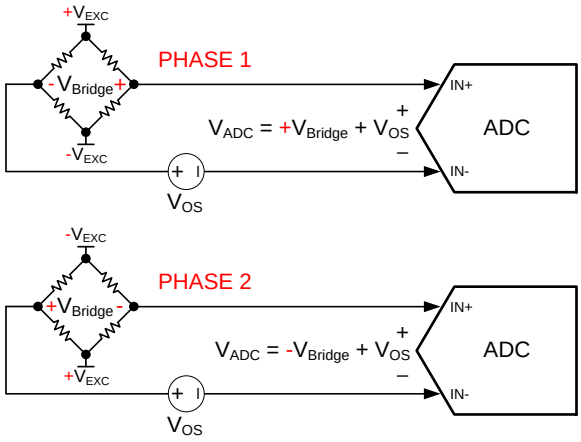

Figure 6: AC Bridge Excitation Concept

Equation 4 shows that ac bridge excitation removes offsets in the same way that input chopping removes offsets. The only difference between these two methods is the location of the chopping/switching.

$$V_{ADC} = \frac{V_{ADC}(PHASE\ 1) - V_{ADC}(PHASE\ 2)}{2} = \frac{\left(V_{Bridge} + V_{OS}\right) - \left(-V_{Bridge} + V_{OS}\right)}{2} = V_{Bridge} \quad (4)$$

The offset voltage, $\mathbf{V_{OS}}$, of Figure 6 comprises all offset voltages in the measurement system. These may include the ADC's offset, parasitic thermocouples (to be discussed in Section 2.3), or any offsets added by signal conditioning circuitry. Therefore, as long as $\mathbf{V_{OS}}$ changes slowly (with respect to the chopping frequency) the system's offset and offset drift are dynamically removed.

The effect of ac bridge excitation is much like continuously measuring and applying a *system* offset calibration (removing the overall offset of the measurement system, as opposed to input chopping, which only removes the ADC's contribution to the system offset).

Note that applying the AC bridge excitation technique will require the reference connections to be switched to keep the reference voltage (as seen by the ADC) positive.

2.3 Overview of Parasitic Thermocouples

Thermocouples are a very useful and common type of temperature sensor. They are formed by junctions of dissimilar metals. When these junctions are exposed to temperature gradients, a thermal electromotive force (EMF), or Seebeck voltage, is produced as a function of the temperature gradient and the metals involved. When thermocouples are used intentionally, they can provide accurate temperature sensing over a wide temperature range and at a low cost. However, unintentional thermocouples are just as common (if not more) and can greatly reduce the accuracy of precision sensing applications. When used unintentionally, we refer to these thermocouples as *parasitic thermocouples*.

> *Refer to previous TI Design documents (SLAU509 or TIDU574) for more detailed descriptions and overviews of thermocouple theory.*

Parasitic thermocouples exist in many locations within a circuit. Most connections to the printed circuit board (PCB) will involve multiple dissimilar metals such as copper, tin, lead, nickel, gold, silver, aluminum, etc... The larger the Seebeck coefficient (or sensitivity, expressed in µV/°C) between these junctions, the larger the offset voltage that can be introduced into the circuit as a temperature gradient is formed. The typical thermocouple sensitivity of most dissimilar metals will have a Seebeck coefficient in the range of a few microvolts per degree Celsius (µV/°C). However, thermocouples with sensitivities >500 µV/°C are possible with Copper-Copper Oxide junctions (caused by oxidation).

Parasitic thermocouples add to the offset and offset drift of the measurement system and may significantly degrade the overall system accuracy.

2.3.1 Reducing the Effects of Parasitic Thermocouples

PCB layout can reduce the effects of parasitic thermocouples. Symmetrical PCB layouts and differential measurements may help to match parasitic thermocouples and cancel any common-mode offsets. The use of a large (solid) ground plane can also act as a heat sink to remove thermal gradients. By keeping dissimilar metal junctions at a constant temperature, the parasitic thermocouple will not induce any additional Seebeck (offset) voltage because of the law of intermediate metals.

Calibration may also be performed to correct for these offsets under certain conditions; however, dynamically changing environments may result in dynamic offsets, which are difficult to correct for by calibration alone. Even when calibrations are performed at multiple operating temperatures, the effect of parasitic thermocouples may still be observed as an offset drift over temperature.

AC bridge excitation is one of the best methods to remove the effects of parasitic thermocouples. Parasitic thermocouples appear *after* the chopping stage; therefore, their offset is continuously removed. This is the advantage of ac bridge excitation, as compared to offset calibration, which can only remove the initial offset.

2.3.2 Other Causes of Offset and Offset Drift

Parasitic thermocouples are just one example of an offset voltage source with temperature dependence. Another common source of offset voltage and offset drift results from input bias currents, namely *input offset currents* or *differential input currents*, when the input bias currents of a differential input pair are mismatched. An offset voltage forms when the differential bias current flows through any input-attached impedance, such as an input filter. The offset voltage will be proportional to the current and impedance, and both of these parameters (current and impedance) will typically have temperature dependence.

Additionally, offset and offset drift-like behaviors have been shown (reference) to result from solder flux residues remaining from the PCB assembly process. There residues create parasitic conduction paths within the circuit and result in unpredictable behavior.

3 Component Selection and Configuration

3.1 ADC Selection – ADS1262 (or ADS1263)

The ADC is the critical component in most measurement systems. While all components may affect the overall measurement system performance, the system accuracy is unlikely to exceed the performance of the ADC. Hence, the ADC is typically selected first.

To determine the resolution required by the measurement system, the full-scale output voltage of the bridge is divided by the desired scale resolution specified in counts, as shown in Equation 5. (The scale requirement is 50,000 counts in this example).

$$Required\ Resolution = \frac{10\ mV}{50{,}000} = 200\ nV \rightarrow \log_2(50{,}000) = 15.6\ bits \quad (5)$$

The measurement system must be able to accurately resolve signals of at least 200 nV, or approximately15.6 bits. However, in practice, an ADC of much higher resolution must be used to account for the loss of dynamic range that occurs when the input signal is not scaled (level shifted and amplified) to match the ADC's input range. A 24-bit delta-sigma ADC is usually selected for this type of application.

The ADS1262, a 32-bit delta-sigma ADC, was chosen for this design for its low-noise performance and integrated Programmable Gain Amplifier (PGA). The ADS1262 achieves the resolution required for high-end weigh-scale applications. Additionally, the ADS1262 provides General Purpose Input/Outputs (GPIOs) which may be used to control the switches for ac bridge excitation, a programmable settling delay time that allows large input step changes to settle prior to beginning conversions, and a reference polarity switch that makes it easier to implement ac bridge excitation.

3.1.1 Programmable Gain Amplifier (PGA) Configuration

The ADS1262's integrated low-noise PGA provides gains up to 32 V/V. The highest gain setting, that does not exceed the input voltage range requirements, will typically provide the best noise performance. In this design, the full-scale bridge output voltage is 10 mV; therefore, a gain of 32 V/V may be used. (See Table 4 in the ADS1262 data sheet (SBAS661).

NOTE: The ADC's full-scale range scales with both reference voltage and gain. The full-scale range of the ADS1262 (as used in this design), is shown in Equation 6.

$$FSR = \frac{\pm V_{REF}}{PGA} = \frac{\pm(5\ V)}{32\ V/V} = \pm 156\ mV\ (or\ 312\ mV) \quad (6)$$

NOTE: Many weigh-scale designs typically use gains higher than 32 V/V. However, it is important to note that increasing gain amplifies both the input signal *and* the amplifier's noise. The low-noise PGA of the ADS1262 is capable of resolving much smaller signals than most other amplifier or PGA configured with higher gain.

3.1.2 Digital Filter Configuration

The default filter configuration for the ADS1262 is an FIR filter with a data rate of 20 SPS. This filter setting was used in this design because it provides simultaneous 50/60Hz line cycle rejection and single-cycle settling behavior. This configuration provides ADC resolutions down to 0.167 nV_{PP}, as shown by Table 1 in the ADS1262 data sheet (SBAS661).

3.2 Switch Selection – TS5A21366

The TS5A21366 is a dual single pole single throw (SPST) 0.75Ω analog switch used to control the bridge's excitation voltage polarity (for ac bridge excitation). This switch was chosen for its voltage compatibility and low on-resistance. The digital logic level of the switch is compatible with the 5-V GPIO logic of the ADS1262, and the input allows for the 5-V bridge excitation voltage. The on-resistance of the bridge switch is important to consider in this application because a significant current flows through the bridge (approximately 15mA. The power dissipation of the bridge switch can cause device heating, as well as reduce the excitation voltage and signal magnitude of the bridge output The TS5A21366 is rated for currents up to 200 mA, making it well suited for this application.

NOTE: The TS5A21366 is only specified to operate from -40ºC to 85ºC and was not directly subjected to the forced ambient air temperatures during testing.

3.3 Passive Component Selection

3.3.1 Input and Reference Low-Pass Filters

The input and reference filters are first-order RC circuits. The main purpose of the input filter is for anti-aliasing. While this filter can also assist in reducing signal noise, the low-bandwidth digital filter provides the majority of the signal noise rejection; therefore, we are only concerned about using this filter for anti-aliasing.

The aliasing frequencies of concern are frequencies around the modulator sampling frequency, f_{MOD} (for the ADS1262 f_{MOD} = 921.6 kHz when using the internal oscillator). Note that the sampling frequency inside a delta-sigma ADC is much higher than the output data rate. The input signal is oversampled by the delta-sigma modulator and the output data rate is decimated by the digital filter.

The delta-sigma ADC's digital filter does not provide much noise attenuation around the sampling frequency. Signals in this region are aliased back into the filter's low-frequency passband. Typically, a single-pole RC filter is adequate to attenuate signals in this region. Figure 7 shows an example of an RC filter with a cutoff frequency of 33.8 kHz and ~29 dB of attenuation near the ADC's sampling frequency.

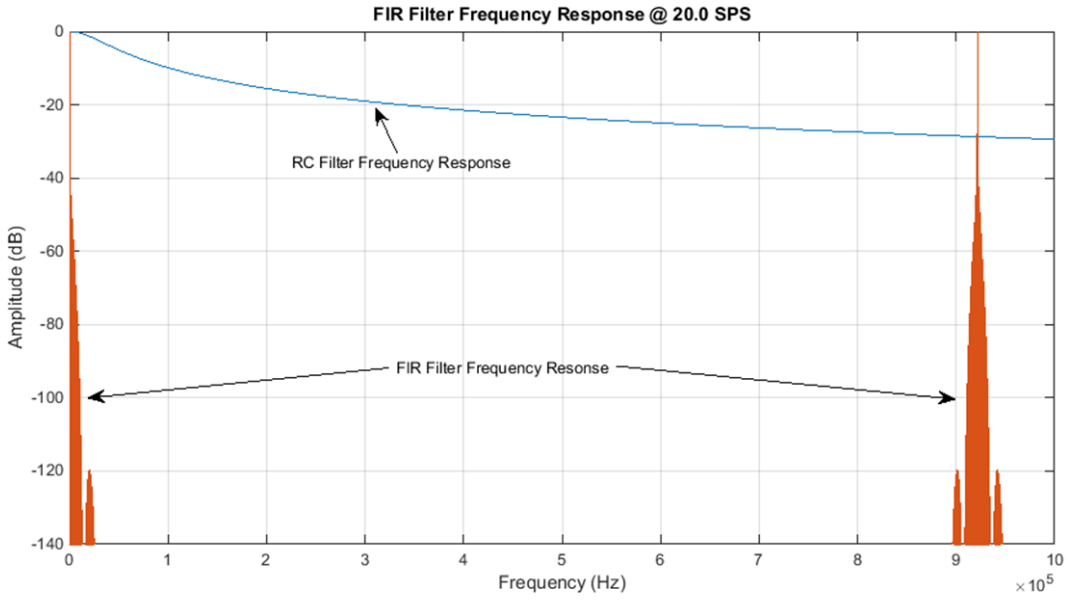

Figure 7: 20 SPS FIR Filter Frequency Response

Refer to Section 10.1.5.1 in the ADS1262 Data Sheet (SBAS661) for additional information on aliasing.

3.3.2 X2Y™ Capacitors

X2Y™ capacitors were used for the RC low-pass filters. A single X2Y™ capacitor can replace multiple capacitors required for common-mode and differential filtering. In addition to saving board space, these capacitors have low equivalent series inductance (ESL) and excellent common-mode capacitor matching, required to prevent the conversion of common-mode signals to differential signals.

NOTE: Typically common-mode filters become mismatched because of high capacitor tolerances. Higher common-mode signal frequencies are then filtered differently and result in a differential signal seen by the ADC inputs. This effect can also be reduced by ensuring that the differential filter has a lower cutoff frequency (~1/10th) than the common-mode filter's cutoff frequency.

4 Simulations and Calculations

4.1 Load Cell Bridge Simulator Circuit

Figure 8 shows the TINA-TI™ circuit used to simulate the behavior of the load cell bridge.

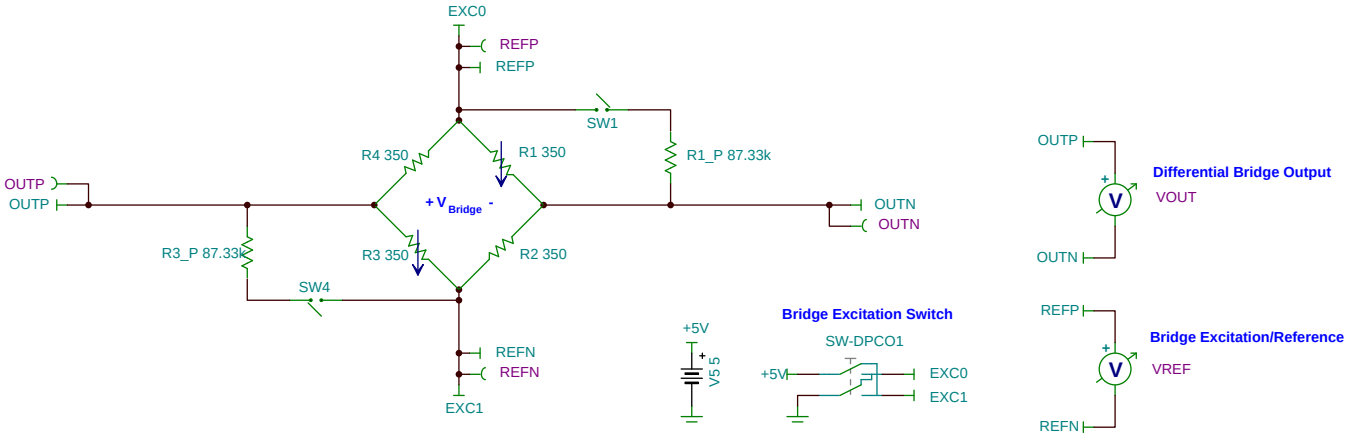

Figure 8: Load Cell Bridge Simulator

The load cell bridge simulator was designed to model the behavior of a load cell at “no load” and “max load” conditions. When SW1 and SW4 are open, the resistor bridge is balanced and the output voltage should be 0 V (no load condition). When SW1 and SW4 are closed, the resistor bridge is unbalanced and the output voltage should be 10 mV (max load condition with 2 mV/V sensitivity and 5-V excitation).

Normally, the resistor changes resistance as a function of the load, but in this simulator circuit, a resistor is switched in to be parallel with the active bridge elements to model the changing resistance. The output voltage of the bridge in Figure 9 can be calculated using Equation 7.

$$V_{Bridge} = -\frac{V_{EXC}}{2} \cdot \frac{\Delta R}{R + \frac{\Delta R}{2}} \quad (7)$$

Where

- “V_{EXC}” is the bridge excitation voltage (5 V)
- “ΔR” is the change in resistance of R1 and R3 when SW1 and SW4 are closed.

Solving Equation 7 with V_{Bridge} = 10 mV, we find that $\Delta R \approx$ -1.3972 Ω. Next we find the value of the parallel resistors (R_{1P} and R_{3P}) that produce an equivalent resistance of $R + \Delta R$ and find that parallel resistors of approximately 87.325 kΩ produce the desired outcome. The simulation confirms this result, with a full-scale bridge voltage of 9.97 mV. The 0.3% full-scale error is tolerable because most load cells will have a similar error (which is removed by performing full-scale calibration).

4.2 Load Cell Simulator Settling Time

Figure 9 shows the TINA-TI™ circuit used to simulate the settling time of the load cell.

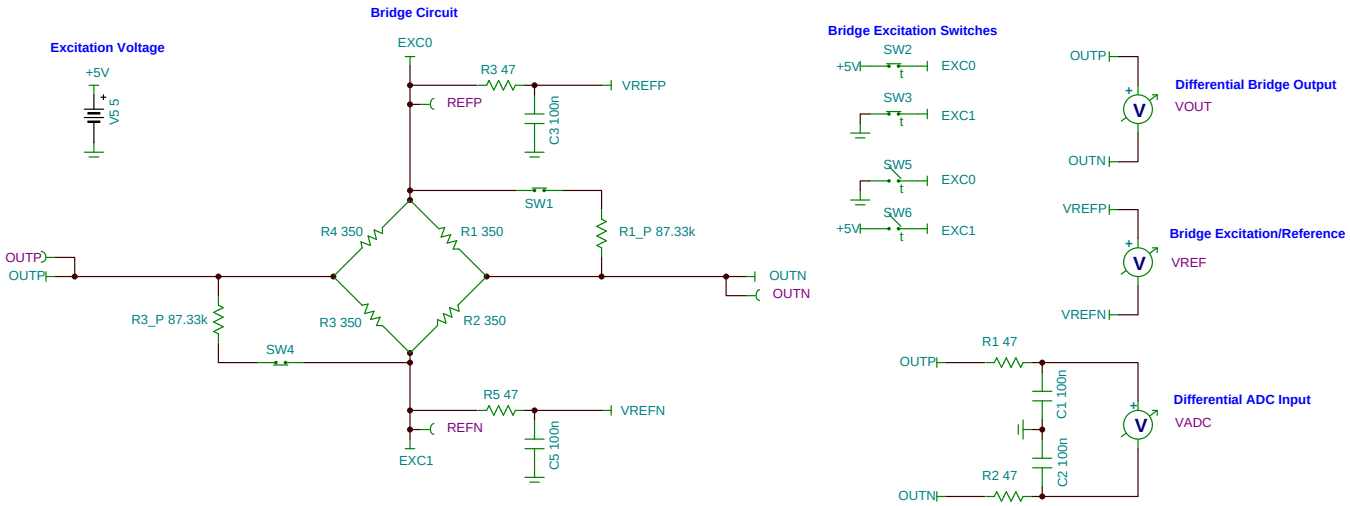

Figure 9: Load Cell Bridge Simulator with Low-Pass Filters

The circuit in Figure 9 has been slightly modified from Figure 8. Switches SW1 and SW4 are closed to set the bridge to full-scale, time-controlled switches are added to control the bridge excitation polarity, and the RC low-pass filters are included on the reference and bridge outputs.

At a certain time, the bridge excitation polarity is switched in a break-before-make scheme and the bridge output is monitored to observe the required settling time of the RC filter. Note that this settling time needs to be provided each time the ac bridge excitation switches polarity, prior to beginning the ADC conversion, which reduces the effective throughput of the ADC. The transient simulation, shown in Figure 10, shows the combined bridge and filter settling time (observed from the ADC's input) to be approximately 250 µs.

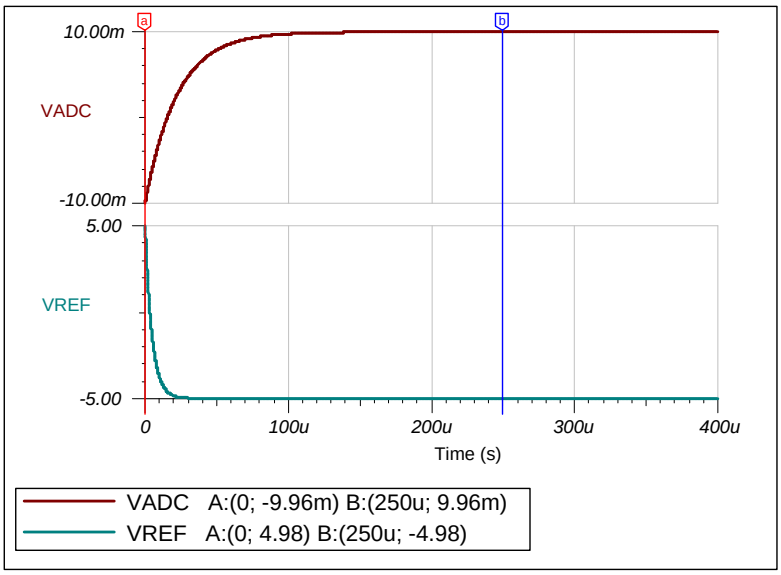

Figure 10: Bridge Settling Time Transient Analysis

Knowing the settling time of the bridge and input circuitry allows us to delay ADC conversions until the ADC's input signal is settled. The ADS1262 allows for a programmable settling delay. Writing "0110b" to the DELAY[3:0] bits in the MODE0 register configures a 278 µs conversion start delay. See Section 9.4.3 (Programmable Time Delay) in the ADS1262 data sheet (SBAS661).

4.3 Effective System Data Rate

The effective system data rate, or throughput, is the rate at which ADC data can be read and processed. This data rate may be less than the programmed data rate of the ADC due to certain measurement delays. These delays are discussed for both the dc- and ac-excited bridge measurements.

4.3.1 Effective System Data Rate for DC-excited Bridge Measurements

In general, measurements in a dc-excited bridge are taken continuously. Therefore, the effective data rate is the same as the ADC's configured data rate. Except, the first ADC conversion result includes some conversion latency to allow for the input circuitry to settle and to allow for the conversion results to propagate through the multiple digital filter stages. See Section 9.4.2 in the ADS1262 data sheet (SBAS661).

Additionally, post-processing may request multiple ADC samples to calculate an averaged result, further reducing the effective data rate. Once all of these delays are combined, the resulting effective data rate is given by Equation 8.

$$DR_{DC\_Eff} = \frac{1}{\left(DELAY + t_{d(STDR)} + \frac{(N-1)}{DR_{Nom}}\right)} \quad (8)$$

- "$DELAY$" is the programmed settling delay of the ADS1262 from the START signal (or command) to the beginning of ADC conversions. This settling delay should be long enough to account for the analog RC filter settling time as simulated in Section 4.2.
- "$t_{d(STDR)}$" is the ADC's conversion latency for the first conversion period. This period is slightly longer than a normal data rate period to allow for digital delays required to start the conversion, calculate the calibrated results, and output the result. These delays are masked by pipelined operations when continuously converting.
- "DR_{Nom}" is the nominal output data rate of the ADC when continuously converting.
- "N" is the number of samples averaged in post-processing.

In this design, the ADS1262 was configured with the 20 SPS, FIR digital filter, and additional 278 µs delay. The time required to collect 16 samples is 802.5 ms, as shown by Equation 9.

$$\frac{1}{DR_{DC\_Eff}} = \left(DELAY + t_{d(STDR)} + \frac{(N-1)}{DR_{Nom}}\right) = 278\ \mu s + 52.22\ ms + \frac{(16-1)}{(20\ SPS)} = 802.5\ ms \quad (9)$$

4.3.2 Effective System Data Rate for AC-excited Bridge Measurements

The effective data rate for ac-excited bridge measurements is similar to the dc-excited case; however, the ADC conversion must be restarted every time the excitation voltage is reversed, resulting in additional conversion latency, as shown by Equation 10.

$$DR_{AC\_Eff} = \frac{1}{2 \cdot \left(DELAY + t_{d(STDR)} + \frac{(N-1)}{DR_{Nom}}\right)} \quad (10)$$

- "N", in this equation, is the number of samples taken each time the excitation voltage polarity is switched.

In this design, the ac-excited bridge was measured with a total of 32 samples (16 samples each time the bridge excitation voltage was switched), resulting in a total collection time of 1605 ms (twice the time calculated in Equation 10).

NOTE: Software delays are assumed to be insignificant and neglected from Equations 8-10.

4.4 Total Error Analysis

The performance of this system depends mostly on the ADC's performance. The ADS1262 error specifications can be taken from the data sheet (SBAS661) and used to estimate the typical performance of this design. The main errors of interest are the noise, offset, offset drift, gain error, gain error drift, and integral nonlinearity (INL). The typical values for these errors were converted to parts per million (ppm) ratios, referenced to the ADC's full-scale range, as shown in Table 2.

Table 2. Total ADC Error Calculations (Typical)

Typical ADC Errors			Error Before Calibration		Error After Calibration	
Noise	198.00	(nVpp)	0.63	(ppm)	0.63	(ppm)
Offset *(removed by ac excitation)*	10.9375	(µV)	35.00	(ppm)	0.16	(ppm)
Offset Drift *(removed by ac excitation)*	10.94	(nV/ºC)	5.78	(ppm)	5.78	(ppm)
Gain Error	0.005%	(%)	1.00	(ppm)	0.01	(ppm)
Gain Error Drift	0.5	(ppm/ºC)	5.28	(ppm)	5.28	(ppm)
INL	3	(ppm)	3	(ppm)	3	(ppm)
TOTAL DC Excitation Error Estimate (@ 10 mV)			**36.01**	**(ppm)**	**8.41**	**(ppm)**
			11253	**nV**	**2627**	**nV**
			14.8	**(nV/ºC)**	**14.8**	**(nV/ºC)**
TOTAL AC Excitation Error Estimate (@ 10 mV)			**6.17**	**(ppm)**	**6.09**	**(ppm)**
			1928	**nV**	**1903**	**nV**
			10	**(nV/ºC)**	**10**	**(nV/ºC)**

For each error calculation, the error was converted to an absolute voltage and then divided by 0.312 mV (the ADC's full-scale range, as calculated in Equation 6). To estimate the absolute voltage error of a temperature-dependent error (offset drift and gain drift), the error must be multiplied by the temperature range (165ºC in this design). To estimate the absolute voltage error of a gain-related error (gain error and gain error drift), the error is multiplied by the ADC's full-scale utilization factor (6.4%, or 10 mV divided by 0.312 mV). All errors were added together using the root sum of squares method to calculate the total error. The root sum of squares method assumes all errors are uncorrelated. When calculating the total error for the ac-excited bridge, the offset and offset drift errors were disregarded because they are removed by chopping.

The full Excel spreadsheet with additional error calculations can be found in the TIPD188 design file (TIDCAM8). ADC error calculations are also explained in a TI Precision Hub Blog (reference).

NOTE: These calculations only take into account the ADC error. The error contributions of the bridge sensor are not observed in this design. In the end-application, the load cell's linearity and other error contributions should also be considered.

It is apparent from these calculations that the initial offset is the largest source of error. To reduce the offset error, either calibration or ac-excited bridge measurements must be implemented. The next largest sources of error are the offset drift and gain error drift. These errors can only be removed by re-calibrating, limiting the system's temperature range, or performing ac bridge excitation to remove the offset drift. When ac bridge excitation is used, the ADC may not require calibration (or may not require re-calibration as often). However, in practical use, the load cell introduced errors may still require calibration.

From these calculations, the total measurement error of the ac-excited is estimated to be within 6 ppm (or about 2 µV) across the temperature range. Additionally, the error's slope across temperature is linearly approximated to be about 15 nV/ºC (for the dc-excited bridge), and 10 nV/ºC (for the ac-excited bridge).

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

The PCB is designed in a BoosterPack form factor to connect to TI's LaunchPads. This particular BoosterPack was specifically designed to pair with the MSP430F5529 USB LaunchPad Evaluation Kit (MSP-EXP430F5529LP). The LaunchPad provides the SPI interface to the ADS1262 and USB interface to the PC. For LaunchPad Hardware, refer to the MSP-EXP430F5529LP hardware design files (SLAR090).

5.1 PCB Layout

For optimal performance in any design, follow standard precision PCB layout guidelines including proper power supply decoupling close to all integrated circuits and adequate power and GND connections with large copper pours.

The top and bottom side PCB layout for this design are shown in Figure 11 (inner ground and power layers are not shown). This layout provides proper power supply decoupling and large ground pours on multiple layers. However, this PCB does not provide a symmetrical layout (as discussed in Section 2.3.1) to purposely allow for some parasitic thermocouples effects.

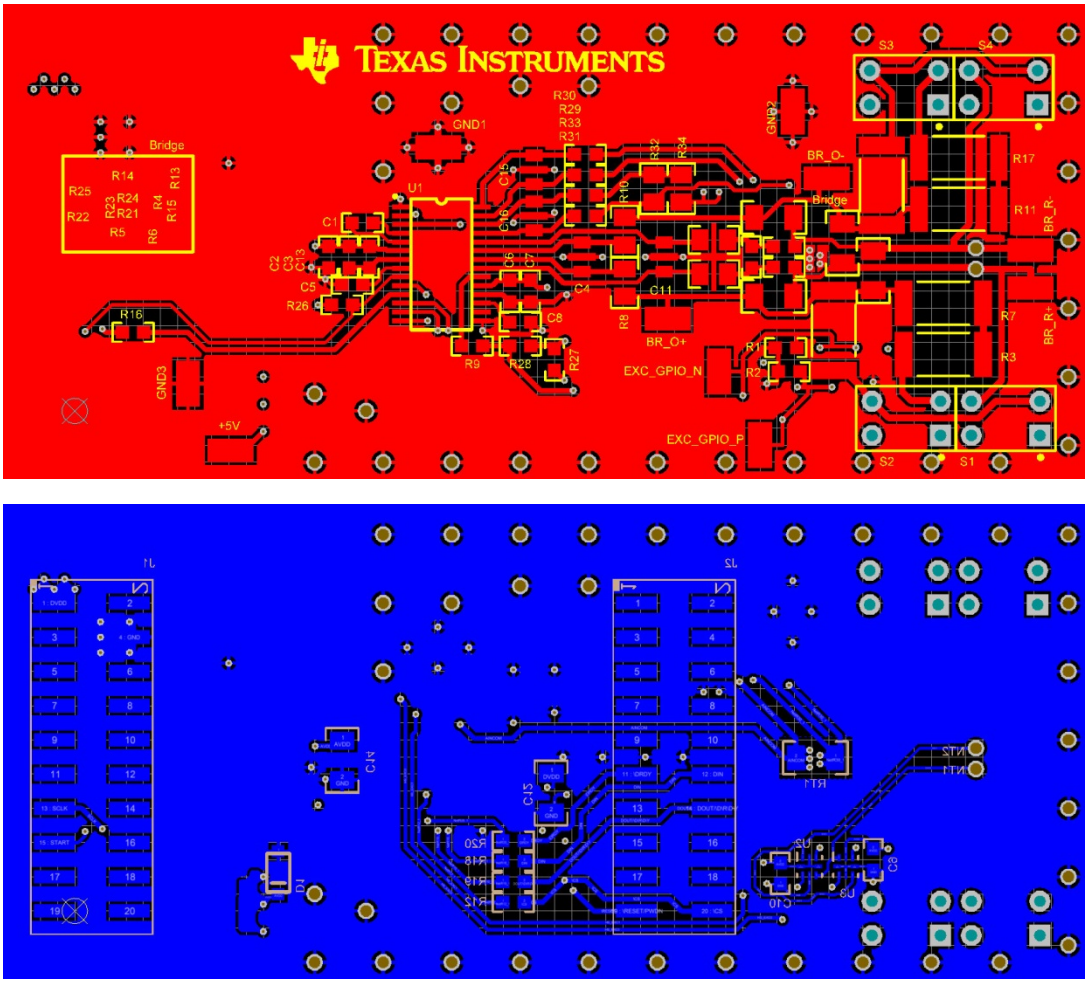

Figure 11: Altium PCB Layout (Top and Bottom Sides)

6 Verification & Measured Performance

The full data collection procedure is outlined in Appendix C. Measurement data was collected for the 0V input and 10mV input cases. These two cases correspond to the 0% full-scale and 100% full-scale bridge outputs (or 0% and 6.4% full-scale range, with respect to the ADC input range, respectively). These cases typically showcase two extremes of the system performance:

1. Near 0% full-scale, measurement error is dominated by offset and INL errors.
2. Near 100% full-scale, measurement error is dominated by gain errors.

6.1 System Measurement Error

The dc and ac bridge excitation measurements were compared to the DMM measurement results to determine the measurement error. The difference between these results removes the offset drift of the resistor bridge circuit from the observed system error. Figure 12 shows the error of the dc- and ac-excited bridge measurements for a 0 V input signal.

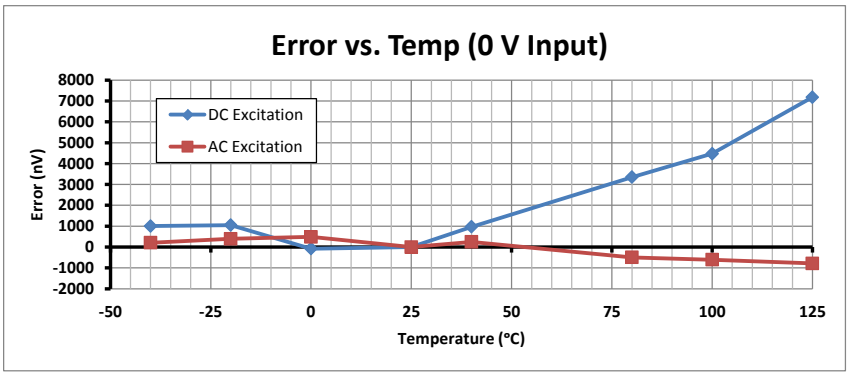

Figure 12: Error vs. Temperature (0 V Input)

Similarly, Figure 13 shows the offset drift of the dc and ac-excited bridge measurements for a 10 mV input signal.

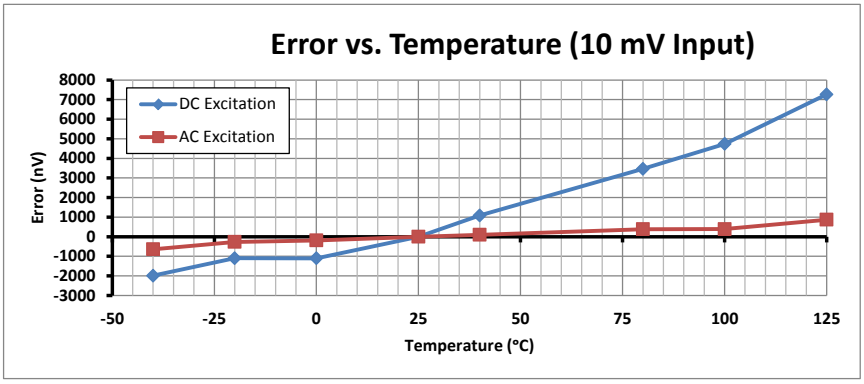

Figure 13: Error vs. Temperature (10 mV Input)

The measurement error is much improved for the ac-excited bridge. Notice how the absolute values and temperature slope are both reduced. Also, notice that the measurement errors for both the 0V and 10mV inputs signal are very similar. In both of these cases, the offset and offset drift errors dominated the overall measurement error, which is what ac bridge excitation is able to remove.

The total system error for the ac-excited bridge (for a 10 mV input) is within ±1 µV. In Section 4.4, the total error calculated was 2 µV. These correlate well since the measurement error was centered around 25ºC.

6.2 Noise Performance

The noise performance of the measurement system was observed across temperature and for both load conditions, as shown in Figures 14 and 15. The noise was measured as the maximum peak-to-peak voltage variation observed within 16 samples.

NOTE: For the ac-excited bridge measurements, two samples from opposite excitation polarities were first averaged to reduce the data from 32 samples to 16 (averaged) samples. The noise was then measured as the peak-to-peak voltage variation within the 16 (averaged) samples.

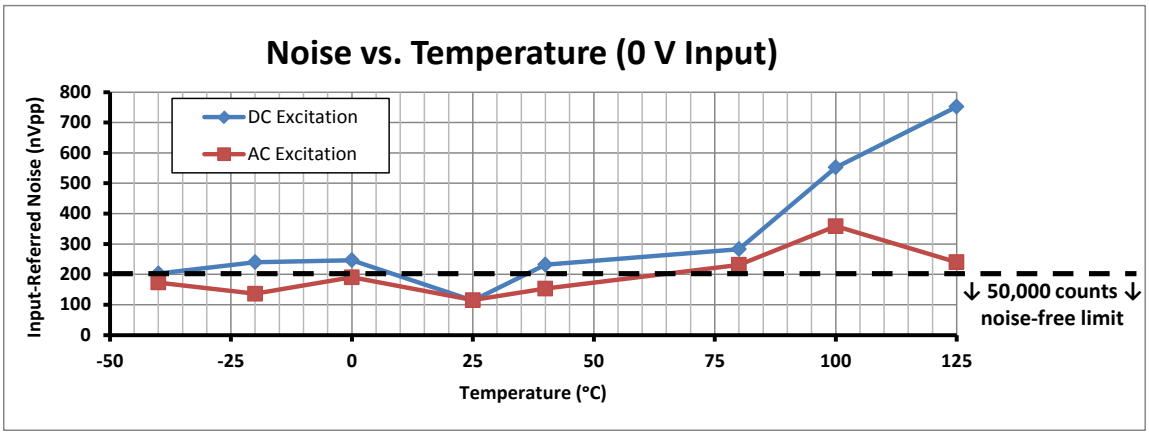

Figure 14: Noise vs. Temperature (0 V Input)

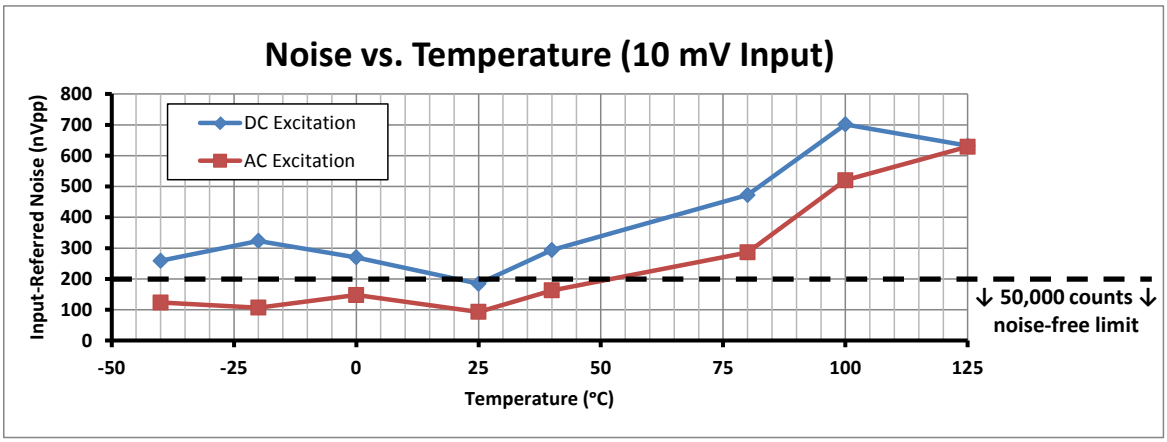

Figure 15: Noise vs. Temperature (10 mV Input)

The averaged ac-excited bridge measurements show improved noise performance over the dc-excited bridge measurements and achieved 50,000 noise-free counts of resolution up to about 50 ºC. Noise performance did not degrade significantly from the 0 V to 10 mV input conditions because of the ratiometric measurement configuration, which provides reference noise cancellation.

The number of noise-free counts is calculated using Equation 11.

$$Noise\text{-}free\ counts = \frac{10\ mV}{Noise\ (nVpp)} = \frac{10\ mV}{200\ nVpp} = 50{,}000 \quad (11)$$

For higher temperatures, increased thermal noise and higher component drift degrade the noise performance. However, weigh-scales are typically not operated up to such high temperatures.

7 Modifications

Many times analog circuit design involves trade-offs between various specifications. This section describes some of the trade-off decisions and possible modifications to this TI Design.

7.1 Effective Data Rate vs. Noise Performance

It is desirable to operate the measurement system at the fastest (effective) data rate that achieves the required noise performance of the measurement system. Noise performance degrades as the data rate is increased, because at higher data rates, the digital filter bandwidth increases and additional noise is observed in the ADC's output codes. However, it is not just the programmed data rate that must be considered in this trade-off, but the *effective data rate* of the system. As seen by Equation 10, the effective data rate is a function of the ADC's configured output data rate, the total settling and conversion delays, and the number of averages taken for each conversion result.

The portion of time which the ADC is converting must first be maximized to improve both the effective data rate and noise performance of the ADC. Therefore, it is important to keep settling times and conversion delays as small as possible, because the ADC is not converting during these delays. To reduce these delays, the cutoff frequencies of the analog input and reference filters can be relaxed. Even though increasing the cutoff frequencies would seem to degrade the noise performance, it does not have a significant impact at these low data rates, where the digital filter provides the bulk of the noise filtering. The cutoff frequencies of these filters can be increased to provide just enough anti-aliasing, and reducing the required settling time.

NOTE: The analog switch's settling time may also be reduced by choosing a switch with a higher on-resistance (R_{ON}), but lower gate capacitance (C_g). However, the settling time of the switch is usually much smaller than the settling time of the input and reference filters.

Once the ADC conversion time has been maximized, the next option is to determine the number of additional samples to average during post-processing to further reduce the measurement system noise. Averaging reduces the standard deviation of the noise by a factor of "$\sqrt{N}$" ("N" is defined in Section 4.3). Note that the square-root factor provides diminishing returns on noise reduction as the number of averages is increased.

Instead of averaging additional samples ("N") in post-processing, a better option may be to reduce the ADC's data rate. This has a similar effect to averaging multiple samples; however, it also benefits from the delta-sigma ADC's noise shaping characteristic, resulting in lower noise than averaging in post-processing. For example, reducing the ADC's data rate from 20 SPS to 2.5 SPS is essentially allowing the ADC to internally average an additional 4 samples per conversion. This typically provides better noise performance than averaging 4 samples taken at the faster (20 SPS) data rate.

7.2 Alternate Reference Filtering Scheme

The schematic for this design provided an optional resistor divider for the ADC's external reference input. This divider was not used, and all reference filter series resistors (R21, R22, R24, and R25) were populated with 0-Ω resistors, as seen in Figure 16.

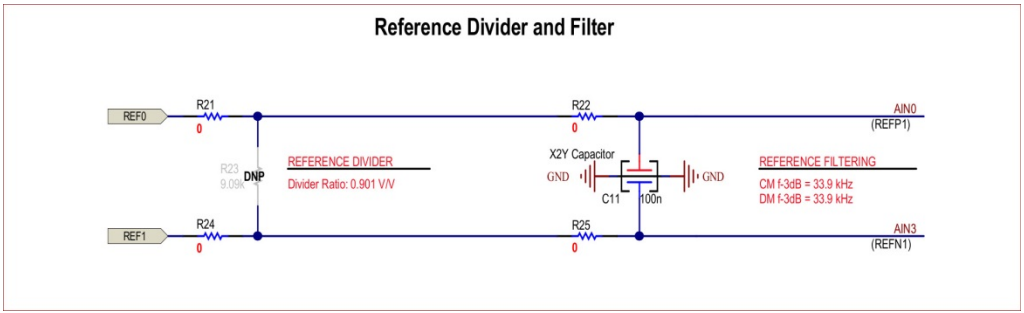

Figure 16: Reference Filter

When the bridge is excited, the positive reference input is approximately 5 V (AVDD) and the negative reference input is approximately 0 V (AVSS). This leads to an average increase in the reference input bias current of about 50 nA (see the reference in the note below). This input current is also more sensitive to temperature variations. Therefore, any voltage drop across the reference resistors would reduce the reference voltage seen by the ADC, creating an additional gain error and gain error over temperature. This error was avoided by using 0-Ω resistors for the reference filter.

An alternate design option is to populate R21 and R24 with 91-Ω resistors and R23 with a 9.09-kΩ resistor to reduce the ADC's reference voltage to 4.9 V. This small decrease in reference voltage is enough to avoid the higher reference input bias currents.

NOTE: Figure 33 in the ADS1262 data sheet (SBAS661) shows the "Reference Input Current vs Reference Input Voltage". The input bias current of the positive reference input increases when a 5 V reference is applied. Note that the x-axis step size in this plot is large and that that positive reference input current is well behaved until the reference is very close to 5 V.

7.3 Alternate ADC Design Options

The ADS1262 was chosen for this design because of its high performance and features that are well suited for implementing an ac-excited bridge measurement. The ADS1263 is a pin-for-pin and software compatible replacement that adds a secondary 24-bit delta-sigma ADC useful for redundant bridge measurements or other supporting functions within weigh-scale applications.

The ADS1232 and ADS1234 are part of another recommended family of 24-bit delta-sigma ADCs, well suited for bridge measurements. These devices are a lower cost alternative to the ADS126x devices, and are also capable of achieving high repeatability. These ADCs also allow for external references voltages up to AVDD + 0.1 V, which is very useful for implementing ratiometric 5-V excited bridge measurements.

For low-power weigh-scale applications, the ADS1220 or ADS1231 24-bit delta-sigma ADCs are recommended. The ADS1220 is capable of fast power-up and duty-cycled operation. Both the ADS1220 and ADS1231provide a low-side bridge switch to power-down the bridge between conversions.

8 About the Author

Christopher Hall is an applications engineer in the Precision Delta-Sigma Data Converters group at Texas Instruments where he supports high-resolution industrial and seismic products and applications. Christopher received both his BSEE and MSEE from the University of Arizona.

9 Acknowledgements & References

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TI Documents:

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9. *Chioye, Luis. RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248. (March 2013). (SBAA201).*

Appendix A. PCB Schematic and Bill of Materials

A.1 Electrical Schematic

The schematic for this design can be seen in Figure A-1.

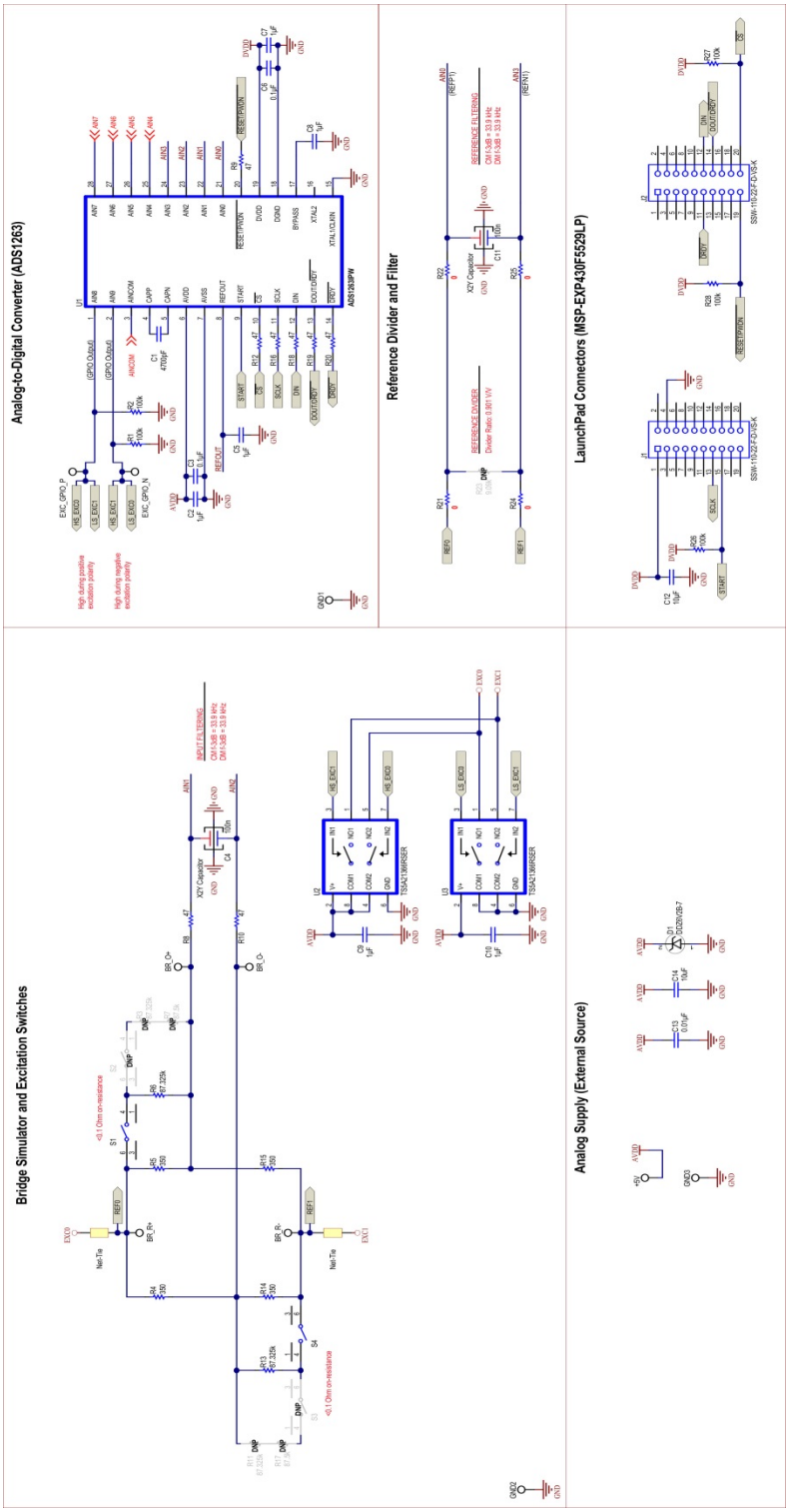

Figure A-1: Electrical Schematic

A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure A-2.

Quantity	Value	Designator	Description	Manufacturer	PartNumber	Supplier 1	Supplier Part Number 1
10		+5V, BR_O+, BR_O-, BR_R+, BR_R-, EXC_GPIO_N, EXC_GPIO_P, GND1, GND2, GND3	TEST POINT, MINIATURE, SMT	Keystone Electronics	5015	Digi-Key	5015KCT-ND
1	4700pF	C1	CAP, CERM, 4700 pF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H472KA01D	Digi-Key	490-1506-1-ND
6	1µF	C2, C5, C7, C8, C9, C10	CAP, CERM, 1uF, 16V, +/-10%, X5R, 0603	MuRata	GRM185R61C105KE44D	Digi-Key	490-3894-1-ND
2	0.1µF	C3, C6	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C104KA01D	Digi-Key	490-1532-1-ND
2	100n	C4, C11	CAP, CERM X2Y, 100 nF, 25V, X7R, +/-20%, 0805	Johanson Dielectrics Inc	250X15W104MV4E	Digi-Key	709-1330-1-ND
1	10µF	C12	CAP, CERM, 10 uF, 16V, X7R +/-20%, 1206	TDK	C3216X7R1C106M160AC	Digi-Key	445-1601-1-ND
1	0.01uF	C13	CAP, CERM, 0.01uF, 25V, +/-10%, X7R, 0603	MuRata	GRM188R71E103KA01D	Digi-Key	490-1520-1-ND
1	10uF	C14	CAP, CERM, 10 uF, 16V, X7R +/-20%, 1206	TDK	C3216X7R1C106M	Digi-Key	445-1601-1-ND
1	6.2V	D1	DIODE, ZENER, 6.2V, 500mW, SOD-123	Diodes Inc	DDZ6V2B-7	Digi-Key	DDZ6V2BDICT-ND
2		J1, J2	Connector, Receptacle, 100mil, 10x2, Gold plated, SMD	Samtec	SSW-110-22-F-D-VS-K	Digi-Key	SSW-110-22-F-D-VS-K-ND
5	100k	R1, R2, R26, R27, R28	RES, 100k Ohm, 5%, 1/10W, 0603	Panasonic	ERJ-3GEYJ104V	Digi-Key	P100KGCT-ND
4	350	R4, R5, R14, R15	RES, 350 Ohm, 0.25%, 0.3W, 1206	Vishay	804-1206	Digi-Key	804-1206-ND
2	87.325k	R6, R13	RES, 87.325k Ohm, 0.01%, 0.75W, 2512	Vishay	804-2512	Digi-Key	804-2512-ND
2	47	R8, R10	RES, 47 Ohm, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF47R0V	Digi-Key	P47.0HCT-ND
6	47	R9, R12, R16, R18, R19, R20	RES, 47 Ohm, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF47R0V	Digi-Key	P47.0HCT-ND
4	0	R21, R22, R25, R24	RES, 0 Ohm, 5%, 0.1W, 0603	Rohm	MCR03EZPJ000	Digi-Key	RHM0.0GCT-ND
2		S1, S4	Switch, Toggle, SPST, 1Pos, TH	E-Switch	200USP9T1A1M2RE	Digi-Key	EG4914-ND
1		U1	IC, 32-bit, 38kSPS ADC	Texas Instruments	ADS1263IPW	Texas Instruments	ADS1263IPW
2		U2, U3	IC, Single-Channel 10 Ohms SPDT Analog Switch	Texas Instruments	TS5A21366RSER	Texas Instruments	TS5A21366RSER

Figure A-2: Bill of Materials

Appendix B. Software

The entire Code Composer Studio (CCS) project can be found in the TIPD188 design files (TIDCAN1). These files may also be referenced for ADS1262 example code.

B.1 Measuring the External Reference Voltage with the ADS1262

This code sequence provides a method to approximately measure an external reference voltage. It assumes an accurate knowledge of the internal reference voltage and a stable supply voltage. The supply voltage must be used as a reference voltage when the external reference voltage is greater than internal reference voltage

The ADS1262 first measures the supply voltage (divided by 4) with respect to the internal reference. The internal reference voltage may either be assumed to be 2.5 V, or it may be measured (externally) for better accuracy. Once the supply voltage is known, the external reference is measured with respect to the supply reference (the ADS1262 reference MUX may select the supply voltage as the reference).

```
static inline double get_reference(uint8_t print_output)
{
                uint8_t WriteRegData;                          //Stores the register write values
                int32_t AdcOutput = 0;
                const uint8_t Gain = 1;

                double VoltageReading;
                const double IntRefVolt = 2.49906;
                static double SupplyRefVolt = 5;
                static double ExtRefVolt = 5;

                WriteRegData = MUXP_AVDD | MUXN_AVSS;
                ADS126xWriteRegister(INPMUX, 1, &WriteRegData);

                WriteRegData = RMUXP_INTP | RMUXN_INTN;
                ADS126xWriteRegister(REFMUX, 1, &WriteRegData);

                //Read one conversion
                set_adc_START(1);
                WaitForDRDY();
                set_adc_START(0);
                AdcOutput = ADS126xReadData(6, 1);

                VoltageReading = (double) AdcOutput * IntRefVolt / ((double) Gain * exp2(29));
                SupplyRefVolt = VoltageReading; //VREF = previous supply reading

                WriteRegData = MUXP_AIN0 | MUXN_AIN3;
                ADS126xWriteRegister(INPMUX, 1, &WriteRegData);

                WriteRegData = RMUXP_AVDD | RMUXN_AVSS;
                ADS126xWriteRegister(REFMUX, 1, &WriteRegData);

                //Read one conversion
                set_adc_START(1);
                WaitForDRDY();
                set_adc_START(0);
                AdcOutput = ADS126xReadData(6, 1);

                VoltageReading = (double) AdcOutput * SupplyRefVolt / ((double) Gain * exp2(31));
                ExtRefVolt = VoltageReading;

                return ExtRefVolt;
}
```

Figure B-1: Code Snippet

Appendix C. Test & Calibration Procedure

An Excel document was used to post-process and analyze the data. This Excel file is included in the TIPD188 design files (TIDCAM8) for reference.

9.1 Overview of Test Setup

The PCB (TIPD188 BoosterPack) connects to the MSP430F5529 LaunchPad, as shown in Figure C-1. The LaunchPad provides the SPI and PC interfaces to collect and display the ADC bridge measurement data to the PC.

The PCB (TIPD188 BoosterPack) is placed under a thermostream temperature controller and the bridge output is measured across temperature (-40°C to +125°C), with and without utilizing ac bridge excitation. The data is post-processed and compared to the digital multimeter (DMM) measurements to determine the relative bridge measurement errors, with dc bridge excitation and ac bridge excitation technique

NOTE: The term “dc bridge excitation” indicates that the bridge was measured without ac excitation. In this case, the bridge output is only measured once, without switching the bridge’s excitation voltage polarity.

The digital multimeter (DMM) measurements are required to provide a standard reference value for the ADC measurements, because the bridge resistors and bridge output will also drift over temperature. However, we only want to observe how much the ADC measurement results drift over temperature; not how much the bridge output voltage drifts over temperature.

NOTE: The DMMs measure both the bridge excitation voltage and bridge output voltage (DMM1 measures the bridge output and DMM2 measures the bride excitation voltage). Since a single DMM cannot measure the bridge ratiometrically, both measurements are needed to determine the ADC’s ideal output code. The accuracy of the DMMs is crucial for determining the ADC’s accuracy; therefore, high resolution DMMs, such as the HP 3458A, are required for this test. The ADC and DMM measurements are also separately calibrated to provide matching results at room temperature. Offset and gain calibration are only performed at this single temperature-point so that ADC and DMM mismatches are only the effect of temperature-related offset drifts. The DMM must also measure the ac-excited bridge with both excitation voltage polarities to remove offsets in the path from the bridge output to the DMM input.

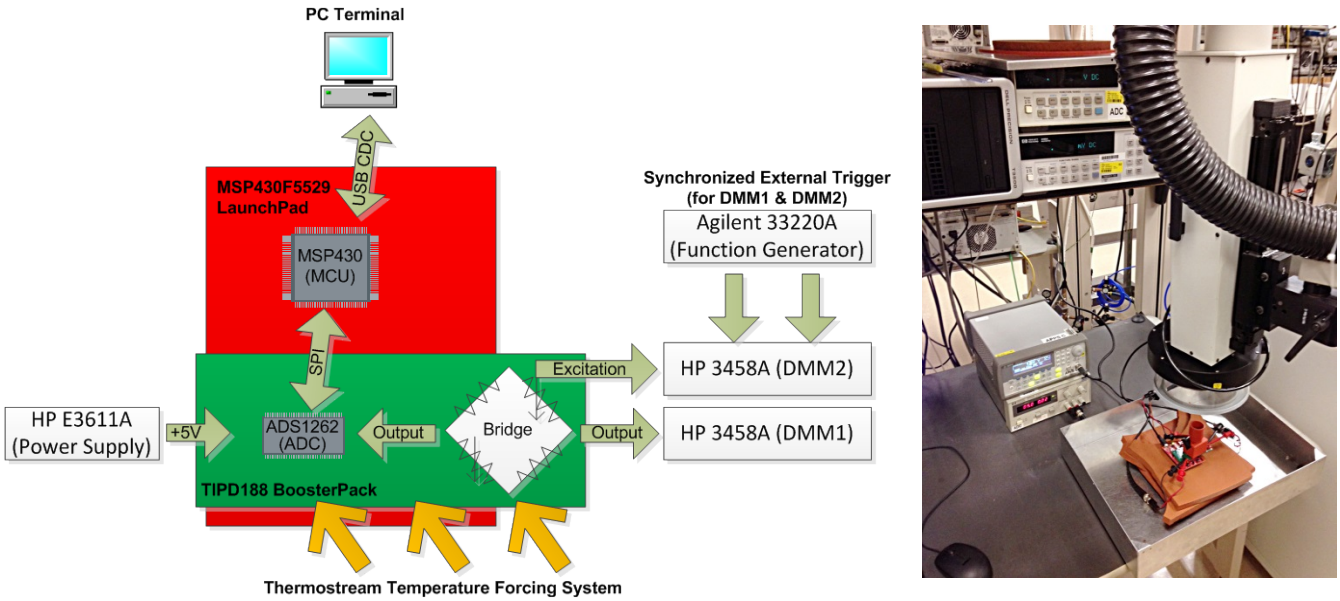

Figure C-1: Test System Block Diagram (Left) and Test Bench Setup (Right)

9.2 Calibration and Measurement Procedure

System offset and gain calibrations were performed once at room temperature for both the ADC and DMM results. Calibration correction calculations were only performed during data post-processing. The ADC calibration registers were configured to their respective default values. Overall three separate sets of calibration coefficients were measured and applied during post-processing; one set per measurement type. The three bridge measurement types are:

A. Measuring the dc-excited bridge with the ADC. This is the traditional bridge measurement technique that is measured here to acquire a baseline performance specification.

B. Measuring the ac excited bridge with the ADC. This is the bridge measurement technique that is applied in this TI design to improve the offset drift performance of the system.

C. Measuring the ac-excited bridge with multimeters DMM1 and DMM2. The multimeters provide an accurate bridge voltage which is used as a reference for calculating the error in the ADC measurements.

The calibration and measurement procedure is broken up into four steps: Offset-calibration, bridge measurement for “no load”, gain calibration, and bridge measurement for “max load”. Offset-calibration correction is applied to all subsequent steps. However, gain-calibration is only applied to the bridge measurement for “max load” (full-scale output) because gain-error is insignificant for the “no load” (0V input) case.

The offset-calibration procedure was performed as follows:

1. Set the thermostream to a standard room temperature (25°C). The system will be calibrated at this temperature.
2. Open switches SW1 and SW4 so that the bridge output voltage is nearly 0 V.
3. Measure the initial ADC’s reference voltage (using the ADC). See Appendix B.1 for this software procedure. Store the result as $\mathbf{V_{REF\_INIT\_ADC}}$. (This value is only used to convert the ADC codes to voltages. In practice, the reference voltage does not need to be measured as the ADC code can be converted to a percentage of the full-scale load.)
4. Measure the excitation voltage of the bridge with the DMM2. Store the result as $\mathbf{V_{REF\_INIT\_DMM}}$.
5. Measure the initial offset voltage of the bridge in three different ways:
    a. Measure the (average) dc-excited bridge output offset voltage with the ADC. Take the average of 16 samples (it may help to convert the samples from hexadecimal to decimal, making sure the sign is correct) to reduce the noise in the offset measurement result. Convert the average code to a voltage (using $\mathbf{V_{REF\_INIT\_ADC}}$) as shown in Equation C-1. Store the result as $\mathbf{OFFSET_{DC}}$

$$\mathrm{OFFSET_{DC}\ (V)} = \left(\frac{\mathrm{CODE}}{2^{32}} \cdot \frac{2 \cdot V_{REF\_INIT\_ADC}}{\mathrm{GAIN}} \right) \quad \text{(C-1)}$$

    (NOTE: “CODE” is the ADC’s output code and “GAIN” is 32 V/V. Equation C-1 may be used generally to convert ADS1262 output codes to their voltage representations).

    b. Measure the (average) ac-excited bridge output offset voltages with the ADC. Take a total of 32 samples (16 samples for each excitation polarity). Average the 16 samples taken with each excitation polarity. Convert these average codes to voltages (using $\mathbf{V_{REF\_INIT\_ADC}}$) then plug these averages into Equation 3 to calculate the average ac-excited bridge offset voltage (subtract these two averages, and then divide by 2). Store the result as $\mathbf{OFFSET_{AC}}$.

c. Measure the (average) ac-excited bridge output offset voltages with DMM1. Take a measurement for each excitation polarity and store the results as $\mathbf{V_{OS\_DMM\_P}}$ and $\mathbf{V_{OS\_DMM\_N}}$.
("$\mathbf{V_{OS\_DMM\_P}}$" is the bridge output offset voltage with a positive excitation polarity and "$\mathbf{V_{OS\_DMM\_N}}$" is the bridge output offset voltage with a negative excitation polarity).

While measuring the bridge output, also measure the bridge excitation voltages with DMM2.Take a measurement for each excitation polarity and store the results as $\mathbf{V_{REF\_OS\_DMM\_P}}$ and $\mathbf{V_{REF\_OS\_DMM\_N}}$.
("$\mathbf{V_{REF\_OS\_DMM\_P}}$" is the bridge output offset voltage for a positive excitation polarity, "$\mathbf{V_{REF\_OS\_DMM\_N}}$" is the bridge output offset voltage for a negative excitation polarity).

To compute the offset voltage coefficient of the DMM measurements normalize and average the DMM voltage readings to simulate a ratiometric measurement, as shown in Equations C-2 through C-4. Store the result as $\mathbf{OFFSET_{DMM}}$.

$$V_{OS\_DMM\_P\_NORM} = \left(\frac{V_{REF\_INIT\_DMM}}{\left| V_{REF\_OS\_DMM\_P} \right|} \cdot V_{OS\_DMM\_P} \right) \quad \text{(C-2)}$$

$$V_{OS\_DMM\_N\_NORM} = \left(\frac{V_{REF\_INIT\_DMM}}{\left| V_{REF\_OS\_DMM\_N} \right|} \cdot V_{OS\_DMM\_N} \right) \quad \text{(C-3)}$$

$$OFFSET_{DMM} = \frac{V_{OS\_DMM\_P\_NORM} - V_{OS\_DMM\_N\_NORM}}{2} \quad \text{(C-4)}$$

Next the bridge offset drift was measured across temperature for the "no load" condition:

6. Change the temperature setting of the thermostream. Wait 5 minutes ("soaking time") for the system temperature to stabilize to the ambient temperature.

7. Measure the output voltage of the bridge using the three measurement methods.

   a. Measure the (average) dc-excited bridge output offset voltage with the ADC. Take the average of 16 samples and convert the average code to a voltage (using $\mathbf{V_{REF\_INIT\_ADC}}$). Subtract $\mathbf{OFFSET_{DC}}$ from this value and store the result as $\mathbf{V_{OS\_DC\_<x>°C}}$ (where "<x>" is the current ambient temperature).

   b. Measure the (average) ac-excited bridge output offset voltage with the ADC. Take 32 samples (16 samples for each excitation polarity). Calculate the average values for each polarity and convert these values to voltages (using $\mathbf{V_{REF\_INIT\_ADC}}$). Calculate a single average voltage using Equation 3. Subtract $\mathbf{OFFSET_{DC}}$ from this value and store the result as $\mathbf{V_{OS\_AC\_<x>°C}}$ (where "<x>" is the current ambient temperature).

c. Measure the (average) ac-excited bridge output offset voltages with DMM1. Take a measurement for each excitation polarity and store the results as $\mathbf{V_{OS\_DMM\_<X>°C\_P}}$ and $\mathbf{V_{OS\_DMM\_<X>°C\_N}}$.
("$\mathbf{V_{OS\_DMM\_<X>°C\_P}}$" is the bridge output offset voltage with a positive excitation polarity and "$\mathbf{V_{OS\_DMM\_<X>°C\_N}}$" is the bridge output offset voltage with a negative excitation polarity).

While measuring the bridge output, also measure the bridge excitation voltages with DMM2.Take a measurement for each excitation polarity and store the results as $\mathbf{V_{REF\_OS\_DMM\_<X>°C\_P}}$ and $\mathbf{V_{REF\_OS\_DMM\_<X>°C\_N}}$.
("$\mathbf{V_{REF\_OS\_DMM\_<X>°C\_P}}$" is the bridge output offset voltage for a positive excitation polarity, "$\mathbf{V_{REF\_OS\_DMM\_<X>°C\_N}}$" is the bridge output offset voltage for a negative excitation polarity, and "<X>" is the current ambient temperature).

To compute the ideal voltage (as should have been seen by the ADC) normalize, average, and subtract the offset from the DMM voltage readings then store the result as $\mathbf{V_{OS\_DMM\_<X>°C}}$, as shown in Equations C-5 through C-7.

$$V_{OS\_DMM\_<X>°C\_P\_NORM} = \left(\frac{V_{REF\_INIT\_DMM}}{V_{REF\_DMM\_<X>°C\_P}} \cdot V_{OS\_DMM\_<X>°C\_P} \right) \quad (C\text{-}5)$$

$$V_{OS\_DMM\_<X>°C\_N\_NORM} = \left(\frac{V_{REF\_INIT\_DMM}}{V_{REF\_DMM\_<X>°C\_N}} \cdot V_{OS\_DMM\_<X>°C\_N} \right) \quad (C\text{-}6)$$

$$V_{OS\_DMM\_<X>°C} = \frac{V_{OS\_DMM\_<X>°C\_P\_NORM} - V_{OS\_DMM\_<X>°C\_N\_NORM}}{2} - OFFSET_{DMM} \quad (C\text{-}7)$$

8. Repeat steps 6 and 7 for all desired temperature settings. Compare all $\mathbf{V_{OS\_DC\_<X>°C}}$ and $\mathbf{V_{OS\_AC\_<X>°C}}$ to $\mathbf{V_{OS\_DMM\_<X>°C}}$ to see if the ac bridge excitation improved the offset drift performance for the "no load" condition.

Next the gain-calibration procedure was performed as follows:

9. Set the thermostream to a standard room temperature (25°C). The system will be calibrated at this temperature. (Allow time for the system to stabilize back to room temperature if needed.)
10. Close switches SW1 and SW4. (The full-scale bridge output voltage is about 10 mV).
11. Measure the full-scale output voltage of the bridge in three different ways:

    a. Measure the dc-excited full-scale bridge output voltage with the ADC. Take the average of 16 samples to reduce the noise in the offset measurement result. Convert the average code to a voltage (using $\mathbf{V_{REF\_INIT\_ADC}}$) and subtract $\mathbf{OFFSET_{DC}}$. Finally, divide 10 mV by this result and store as $\mathbf{GAIN_{DC}}$.

    b. Measure the (average) ac-excited full-scale bridge output voltages with the ADC. Take a total of 32 samples (16 samples for each excitation polarity). Average the 16 samples taken with each excitation polarity. Convert these average codes to voltages (using $\mathbf{V_{REF\_INIT\_ADC}}$) then substitute these two average measurements into Equation 3, to get a single averaged result. Finally, divide 10 mV by this result and store as $\mathbf{GAIN_{AC}}$.

c. Measure the ac-excited full-scale bridge output voltages with DMM1. Take a measurement for each excitation polarity and store the results as $\mathbf{V_{FS\_DMM\_P}}$ and $\mathbf{V_{FS\_DMM\_N}}$. ("$\mathbf{V_{FS\_DMM\_P}}$" is the full-scale bridge output voltage with a positive excitation polarity and "$\mathbf{V_{FS\_DMM\_N}}$" is the full-scale bridge output voltage with a negative excitation polarity).

While measuring the bridge output, also measure the bridge excitation voltages with DMM2.Take a measurement for each excitation polarity and store the results as $\mathbf{V_{REF\_FS\_P}}$ and $\mathbf{V_{REF\_FS\_N}}$.
("$\mathbf{V_{REF\_FS\_DMM\_P}}$" is the full-scale bridge output voltage with a positive excitation polarity and "$\mathbf{V_{REF\_FS\_DMM\_N}}$" is the full-scale bridge output voltage with a negative excitation polarity).

To compute the gain calibration coefficient for the DMM measurements, normalize, average, and subtract the (averaged) ac-excited bridge offset voltage from the DMM voltage readings. Then, divide 10 mV by this result and store this value as $\mathbf{GAIN_{DMM}}$, as shown in Equations C-8 through C-10.

$$V_{FS\_DMM\_P\_NORM} = \left(\frac{V_{REF\_INIT\_DMM}}{V_{REF\_FS\_DMM\_P}} \cdot V_{FS\_DMM\_P} \right) \quad (C\text{-}8)$$

$$V_{FS\_DMM\_N\_NORM} = \left(\frac{V_{REF\_INIT\_DMM}}{V_{REF\_FS\_DMM\_N}} \cdot V_{FS\_DMM\_N} \right) \quad (C\text{-}9)$$

$$GAIN_{DMM} = \frac{10mV}{\left(\frac{V_{FS\_DMM\_P\_NORM} - V_{FS\_DMM\_N\_NORM}}{2} - OFFSET_{DMM} \right)} \quad (C\text{-}10)$$

Finally, the bridge offset drift was measured across temperature for the "max load" condition:

12. Change the temperature setting of the thermostream. Wait 5 minutes ("soaking time") for the system temperature to stabilize to the ambient temperature.

13. Measure the output voltage of the bridge using the three measurement methods.

    a. Measure the dc-excited full-scale bridge output voltage with the ADC. Take 16 samples and convert the average result to a voltage (using $\mathbf{V_{REF\_INIT\_ADC}}$). Subtract $\mathbf{OFFSET_{DC}}$ from this value, multiply by $\mathbf{GAIN_{DC}}$, and store the result as $\mathbf{V_{FS\_DC\_<X>°C}}$ (where "<x>" is the current ambient temperature).

    b. Measure the (average) ac-excited full-scale bridge output voltage with the ADC. Take 32 samples (16 samples for each excitation polarity). Average the 16 samples taken with each excitation polarity. Convert the averages to voltages (using $\mathbf{V_{REF\_INIT\_ADC}}$). Calculate a single average voltage using Equation 3. Subtract $\mathbf{OFFSET_{DC}}$ from this value, multiply by $\mathbf{GAIN_{AC}}$, and store the result as $\mathbf{V_{FS\_AC\_<X>°C}}$ (where "<x>" is the current ambient temperature).

c. Measure the ac-excited full-scale bridge output voltages with DMM1. Take a measurement for each excitation polarity and store the results as $\mathbf{V_{FS\_DMM\_<X>°C\_P}}$ and $\mathbf{V_{FS\_DMM\_<X>°C\_N}}$.
("$\mathbf{V_{FS\_DMM\_<X>°C\_P}}$" is the full-scale bridge output voltage for a positive excitation polarity and "$\mathbf{V_{FS\_DMM\_<X>°C\_N}}$" is the full-scale bridge output voltage for a negative excitation polarity, and "<X>" is the current ambient temperature).

While measuring the bridge output, also measure the bridge excitation voltages with DMM2.Take a measurement for each excitation polarity and store the results as $\mathbf{V_{REF\_FS\_DMM\_<X>°C\_P}}$ and $\mathbf{V_{REF\_FS\_DMM\_<X>°C\_N}}$.
("$\mathbf{V_{REF\_FS\_DMM\_<X>°C\_P}}$" is the bridge output offset voltage with a positive excitation polarity, "$\mathbf{V_{REF\_FS\_DMM\_<X>°C\_N}}$" is the bridge output offset voltage with a negative excitation polarity, and "<X>" is the current ambient temperature).

To compute the ideal voltage (as should have been seen by the ADC) normalize, average, subtract the offset, and multiply by the gain calibration coefficient before storing the result as $\mathbf{V_{FS\_DMM\_<X>°C}}$, as shown in Equations C-11 through C-13.

$$V_{FS\_DMM\_<X>°C\_P\_NORM} = \left(\frac{V_{REF\_INIT\_DMM}}{V_{REF\_FS\_DMM\_<X>°C\_P}} \cdot V_{FS\_DMM\_<X>°C\_P} \right) \quad \text{(C-11)}$$

$$V_{FS\_DMM\_<X>°C\_N\_NORM} = \left(\frac{V_{REF\_INIT\_DMM}}{V_{REF\_FS\_DMM\_<X>°C\_N}} \cdot V_{FS\_DMM\_<X>°C\_N} \right) \quad \text{(C-12)}$$

$$V_{FS\_DMM\_<X>°C} = \left(\frac{V_{FS\_DMM\_<X>°C\_P\_NORM} - V_{FS\_DMM\_<X>°C\_N\_NORM}}{2} - OFFSET_{DMM} \right) \cdot GAIN_{DMM} \quad \text{(C-13)}$$

14. Repeat steps 12 and 13 for all desired temperature settings. Compare all $\mathbf{V_{FS\_DC\_<X>°C}}$ and $\mathbf{V_{FS\_AC\_<X>°C}}$ to $\mathbf{V_{FS\_DMM\_<X>°C}}$ to see if ac bridge excitation improved the offset drift performance for the "max load" condition.

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