COMP 122/L Spring 2022 Schedule Subject to Change

Section 0: (1 week)	General Setup and Tools
Section 1: (2 weeks)	Models for Communication and Computation
Section 2: (4 weeks)	Data Formats and Encodings for Computing
Section 3: (2 weeks)	Digital Logic: Combinational and Sequential Circuits
Section 4: (6 weeks)	Three Address Code and Assembly-Level Programming

Week#	Date	<u>Tuesday</u>	<u>Thursday</u>	<u>F</u>
1	1/24	Administrative Overview Tools and Assignments	Administrative Overview Tools and Assignments	
2	1/31	Models of Computing and Communication	Models of Computing and Communication	
3	2/7	Instruction Set Architecture MIPS	Space for Computing Main Memory Intro to OS and Execution Model	Q u i z # 1
4	2/14	Encodings: Functions /Mapping / State system calls ASCII / UTF-8 Lookup Tables MIPS Instructions Base64 Base Conversions via lookup	Numbering Systems Review Status Flags Fixed numbers Scientific Notation	
5	2/21	Base Conversions	Binary Numbering Systems Complements	
6	2/28	Mathematical Operations Addition, Carry Operations	Scientific Notation Floating Point Representation	

Revised: 1/20/21

		BCD / Binary Addition		
7	3/7	Review	Exam #2	
8	3/14	Boolean Algebra (and, or, not) 2 inputs Intro to Circuit	Boolean Algegra (cont) Combinational Circuits Half and Full Adder Decoders, Multiplexiers, BCD-7Segment	
	3/21	Seme	ester Break	
9	3/28	Sequential Circuits FlipFlop Register Data & Instructions Memory: Decoder and Registers	Online Quiz #2 No Class on Thursday	Q u - z # 3
10	4/4	MIPS Architecture Overview Pipeline Architecture Instruction Decoding	MIPS Architecture II Types of Instructions Instruction Encoding Memory Addressing Modes	
11	4/11			
12	4/18	Basic Blocks Control Flow Branch and Jump Instructions	Data Declarations Memory Instructions & Alignments Endianness	
13	4/25	TAC Instructions MIPS: Arithmetic and Logical Instructions	Shifts, Rotates, and Masks Endianness	
14	5/2	Special Registers: Multi/Divide (Hi/Lo)	Stack Operations: PUSH, POP	

Revised: 1/20/21

15	5/9	System Calls & Subroutine Calls	Exam #4	
		Register Conventions: trap, interrupt, and call		

Revised: 1/20/21