

General Purpose Timers:

- GPTM = General purpose Time & module (GPTM)
 - Six 16/32-bit GPTM block
 - Six 32/64-bit GPTM block
 - Each GPTM block has two timers

<u>timer A</u> <u>16 bit</u>	<u>timer B</u> <u>16 bit</u>	<u>timer A</u> <u>32 bit</u>	<u>timer B</u> <u>32 bit</u>
\rightarrow configure independently as 16 bit as timer or counter		\rightarrow 32 bit	\rightarrow concatenated = 64 bit

- Like GPTM- PWM timers
Systic timers etc ✓
 - Functional operation:
 - 16-32 bit operation mode:
 - 16-32 bit programmable one-shot timer ✓
 - periodic timer ✓
 - 16 bit GPTM + 8 bit prescaler $\Rightarrow 24\text{bit}$
 - 32 bit RTC using 32.768 kHz clock
 - 16 bit input edge count or time count with 8 bit prescaler

→ 16 bit PWM mode with 8 bit prescaler

- 32-64 bit operating mode:

→ programmable one shot ✓

→ periodic timer ✓

→ 32 bit General Timer + 16 bit prescaler = 48 bit

→ 64 bit RTC using 8.768 kHz clock

→ 32 bit input edge count or time cap.

mode with 16 bit prescaler

→ 32-bit PWM mode with 16-bit prescaler }

- count up/down

• 12 16/32 bit CCP Pins ✓

• 12 32/64 bit CCP Pins ,

• parallel chaining of timers ✓

• timer synchronization ✓

• ADC event trigger ✓

• snapshot ability ✓

• efficient transfer using MDMA ✓

Figure 11-1. GPTM Module Block Diagram

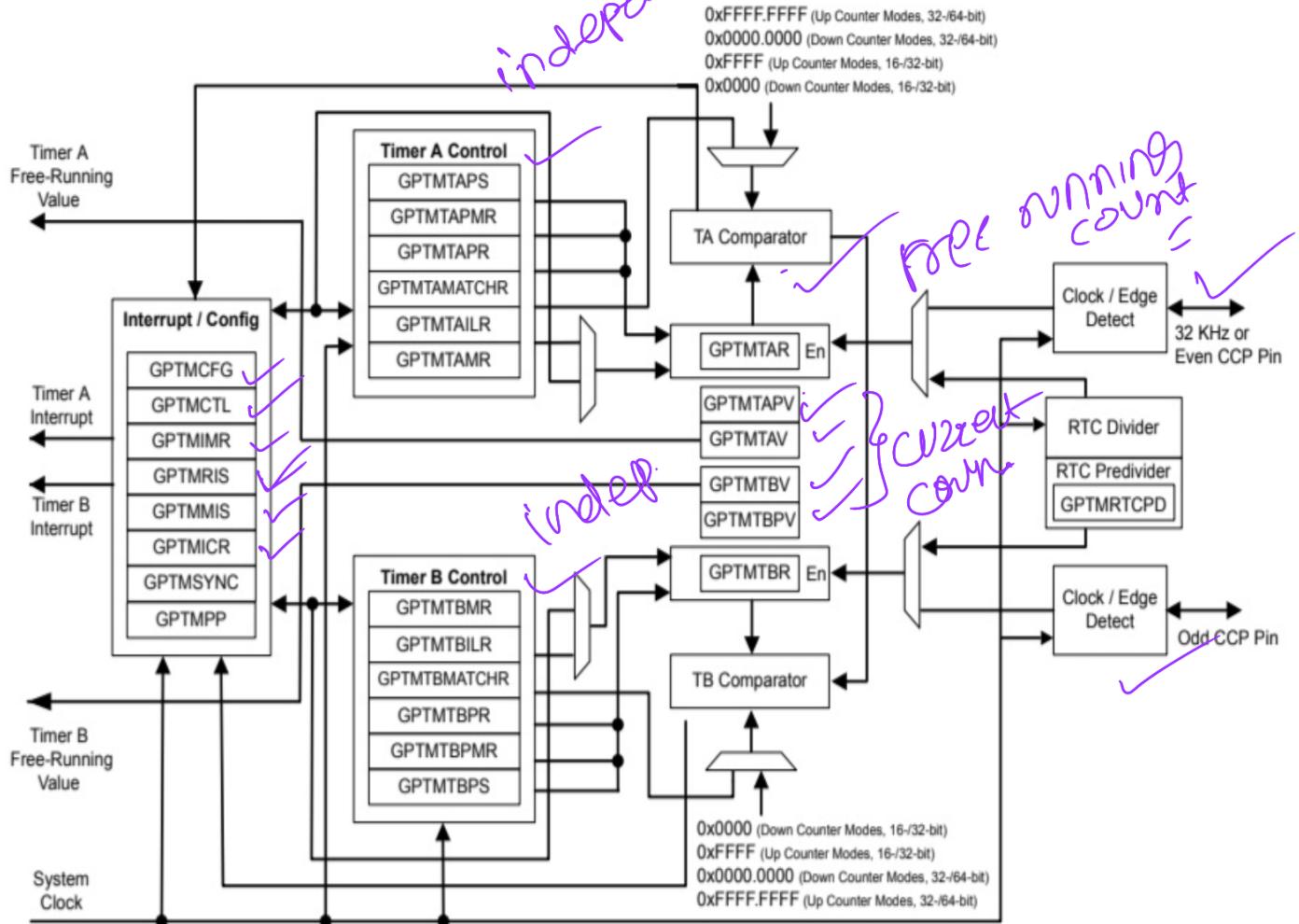


Table 11-1. Available CCP Pins

Timer	Up/Down Counter	Even CCP Pin	Odd CCP Pin
16/32-Bit Timer 0	Timer A	T0CCP0	-
	Timer B	-	T0CCP1
16/32-Bit Timer 1	Timer A	T1CCP0	-
	Timer B	-	T1CCP1
16/32-Bit Timer 2	Timer A	T2CCP0	-
	Timer B	-	T2CCP1
16/32-Bit Timer 3	Timer A	T3CCP0	-
	Timer B	-	T3CCP1
16/32-Bit Timer 4	Timer A	T4CCP0	-
	Timer B	-	T4CCP1
16/32-Bit Timer 5	Timer A	T5CCP0	-
	Timer B	-	T5CCP1
32/64-Bit Wide Timer 0	Timer A	WT0CCP0	-
	Timer B	-	WT0CCP1
32/64-Bit Wide Timer 1	Timer A	WT1CCP0	-
	Timer B	-	WT1CCP1
32/64-Bit Wide Timer 2	Timer A	WT2CCP0	-
	Timer B	-	WT2CCP1
32/64-Bit Wide Timer 3	Timer A	WT3CCP0	-
	Timer B	-	WT3CCP1
32/64-Bit Wide Timer 4	Timer A	WT4CCP0	-
	Timer B	-	WT4CCP1
32/64-Bit Wide Timer 5	Timer A	WT5CCP0	-
	Timer B	-	WT5CCP1

Signal description:

✓

- The general purpose timer signals are alternate functions for some GPIO pins
- AFSEL bit → set to timer Function ✓
GPIO Port Control → GPIO PCTL = GP timer signal

Table 11-2. General-Purpose Timers Signals (64LQFP)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type ^a	Description
T0CCP0	1 28	PB6 (7) PF0 (7)	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
T0CCP1	4 29	PB7 (7) PF1 (7)	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.

Table 11-2. General-Purpose Timers Signals (64LQFP) (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type ^a	Description
T1CCP0	30 58	PF2 (7) PB4 (7)	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
T1CCP1	31 57	PF3 (7) PB5 (7)	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
T2CCP0	5 45	PF4 (7) PB0 (7)	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
T2CCP1	46	PB1 (7)	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 1.
T3CCP0	47	PB2 (7)	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
T3CCP1	48	PB3 (7)	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
T4CCP0	52	PC0 (7)	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
T4CCP1	51	PC1 (7)	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
T5CCP0	50	PC2 (7)	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 0.
T5CCP1	49	PC3 (7)	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 1.
WT0CCP0	16	PC4 (7)	I/O	TTL	32/64-Bit Wide Timer 0 Capture/Compare/PWM 0.
WT0CCP1	15	PC5 (7)	I/O	TTL	32/64-Bit Wide Timer 0 Capture/Compare/PWM 1.
WT1CCP0	14	PC6 (7)	I/O	TTL	32/64-Bit Wide Timer 1 Capture/Compare/PWM 0.
WT1CCP1	13	PC7 (7)	I/O	TTL	32/64-Bit Wide Timer 1 Capture/Compare/PWM 1.
WT2CCP0	61	PD0 (7)	I/O	TTL	32/64-Bit Wide Timer 2 Capture/Compare/PWM 0.
WT2CCP1	62	PD1 (7)	I/O	TTL	32/64-Bit Wide Timer 2 Capture/Compare/PWM 1.
WT3CCP0	63	PD2 (7)	I/O	TTL	32/64-Bit Wide Timer 3 Capture/Compare/PWM 0.
WT3CCP1	64	PD3 (7)	I/O	TTL	32/64-Bit Wide Timer 3 Capture/Compare/PWM 1.
WT4CCP0	43	PD4 (7)	I/O	TTL	32/64-Bit Wide Timer 4 Capture/Compare/PWM 0.
WT4CCP1	44	PD5 (7)	I/O	TTL	32/64-Bit Wide Timer 4 Capture/Compare/PWM 1.
WT5CCP0	53	PD6 (7)	I/O	TTL	32/64-Bit Wide Timer 5 Capture/Compare/PWM 0.
WT5CCP1	10	PD7 (7)	I/O	TTL	32/64-Bit Wide Timer 5 Capture/Compare/PWM 1.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

Functional discription: ✓



Main components:

- i) Free running Counter - up/down ✓
- ii) two prescale registers ✓
- iii) two match registers ✓ !
- iv) two prescale match registers
- v) two shadow registers
- vi) two load / initialization registers.

* when counting down →

True prescaler



* when counting up →

Time2 extension



* In edge time, edge count, PWM mode the prescaler always acts as time2 extension

• For configuring GPTM = GPTMCFG register ✓

Mode Select ✓ = GPTMTAMR ✓
GPTMTBMR .

Table 11-3. General-Purpose Timer Capabilities

Mode	Timer Use	Count Direction	Counter Size		Prescaler Size ^a		Prescaler Behavior (Count Direction)
			16/32-bit GPTM	32/64-bit Wide GPTM	16/32-bit GPTM	32/64-bit Wide GPTM	
One-shot	Individual	Up or Down	16-bit	32-bit	8-bit	16-bit	Timer Extension (Up), Prescaler (Down)
	Concatenated	Up or Down	32-bit	64-bit	-	-	N/A
Periodic	Individual	Up or Down	16-bit	32-bit	8-bit	16-bit	Timer Extension (Up), Prescaler (Down)
	Concatenated	Up or Down	32-bit	64-bit	-	-	N/A
RTC	Concatenated	Up	32-bit	64-bit	-	-	N/A
Edge Count	Individual	Up or Down	16-bit	32-bit	8-bit	16-bit	Timer Extension (Both)
Edge Time	Individual	Up or Down	16-bit	32-bit	8-bit	16-bit	Timer Extension (Both)
PWM	Individual	Down	16-bit	32-bit	8-bit	16-bit	Timer Extension

a. The prescaler is only available when the timers are used individually

Initialization:

Load Registers:

- GPTM timer A interval load (GPTMTA I[R])
- GPTM timer B interval load (GPTMTB I[R])

Shadow registers:

- GPTM timer A value (GPTMTAV) ✓
- B value (GPTMTBV) ✗

Prescale counters initialized to 0's

- GPTM timer A prescale ✓ (GPTMTAPR)
- GPTM timer B prescale ✓ (GPTMTBPR)
- GPTM timer A prescale snap ✗ (GPTMTAPS)
- GPTM timer B pre-snapshot ✓ (GPTMTAPS)

- GPTM timer A prescale value ✓ (GPTM_nAPV)
- GPTM timer B prescale value ✓ (GPTM_nBPV)

① Timer Modes:-

one shot / periodic



→ (i) GPTM_nMR (mode register) ✓

$$\left\{ \begin{array}{l} TnMR = 0/1 = \text{one shot / periodic} \\ TnCDIR = 0/1 = \text{up / down} \\ TnWOT = \text{if set wait for trigger} \\ \quad \quad \quad \text{to begin counting.} \end{array} \right.$$

3

(ii) GPTM CTL (control)

✓ $TnEn = 1$ = counting starts ✓

→ When counting down, if reaches time-out event (0x0) ✓, timer reloads value from GPTM_nELR & GPTM_nPR & vice versa for up counter.

→ For one shot after timeout ✓
 $TnEn = 0$... cleared Stop counting

→ In periodic snapshot mode: ✓ ~
 $TnMR = 0x2$ or
 $TnSNAPS = 1$

→ using snapshot software can determine time elapsed from interrupt assertion to the ISR entry by examining the snapshot value & current value of free running Dⁿ counter

→ Not available for one shot ✓

* Interrupt at timeout: $0 \rightarrow 1$

→ Interrupts, CCP outputs, triggers are generated at timeout event.

→ TnTDRIS = 1 ✓ in GPTM Raw interrupt status (GPTMRIS) holds until it is cleared by writing (GPTM ICR) interrupt clear register

→ If interrupt enable: GPTMIMR ✓
(interrupt mask)

set bit TnTOMIS = mask interrupt status ✓

→ What else you can do??

TnMIE bit → GPTMTnMR

→ An interrupt will get generated when timer value equals the value loaded into GPTM timer n Match (GPTMTnMATCH R) & GPTMTnPMR

- Interrupt has same status as timeout interrupt but uses match interrupt bits.
 - The RIS & MIS bit will not set if TnMIE is not set
 - For ADC trigger = TnOTE bit in GPTM or ~~TnOTE~~
- ① what happens when GPTM Tn ILR & GPTM Tn PR registers get update in betⁿ counting ??
- case 1 :- if Tn ILD = 0 in Mode register counter will load new value on next clock cycle and Continue running from new value
- case 2 :- IF Tn ILD = 1 the new value will load after timeout.
 30 → 40
 26 → 40
- ② when GPTM Tn MR value gets updated betⁿ counting;

- case 1 :- Tn MRSU = 0 } Same as above
- case 2 :- Tn MRSU = 1 , ✓

Table 11-4. Counter Values When the Timer is Enabled in Periodic or One-Shot Modes

Register	Count Down Mode	Count Up Mode
GPTMTnR	GPTMTnILR <i>↙ ↘</i>	0x0
GPTMTnV	GPTMTnILR in concatenated mode; GPTMTnPR in combination with GPTMTnILR in individual mode	0x0
GPTMTnPS	GPTMTnPR in individual mode; not available in concatenated mode	0x0 in individual mode; not available in concatenated mode
GPTMTnPV	GPTMTnPR in individual mode; not available in concatenated mode	0x0 in individual mode; not available in concatenated mode

28 80 ✓ (25)

Table 11-5. 16-Bit Timer With Prescaler Configurations

Prescale (8-bit value) <i>✓</i>	# of Timer Clocks (Tc) ^a <i>✓</i>	Max Time <i>✓</i>	Units
00000000	1 <i>✓</i>	0.8192 <i>✓</i>	ms
00000001 <i>✓</i>	2	1.6384	ms
00000010	3	2.4576	ms
----- <i>28</i>	--	--	--
11111101	254	208.0768	ms
11111110	255	208.896	ms
11111111	256	209.7152	ms

a. Tc is the clock period.

Table 11-6. 32-Bit Timer (configured in 32/64-bit mode) With Prescaler Configurations *✓*

Prescale (16-bit value)	# of Timer Clocks (Tc) ^a	Max Time	Units
0x0000	1	53.687	s
0x0001	2	107.374	s
0x0002	3	214.748	s
-----	--	--	--
0xFFFFD	65534	0.879	10^6 s
0xFFFFE	65535	1.759	10^6 s
0xFFFFF	65536	3.518	10^6 s

a. Tc is the clock period.

* Input Edge - count Mode:

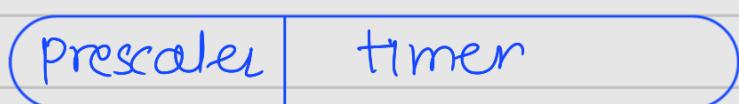
Criteria:-

$$\text{maximum input frequency} = \frac{1}{4} \times \text{system frequency}$$

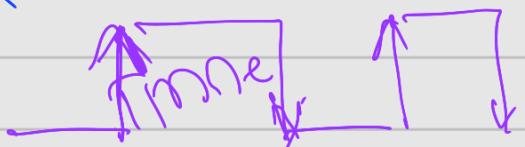
80 MHz
20MHz

→ timer configured as :

- 24 bit - up/down or
- ✓ 48 bit - up/down



GPTMTnPR GPTMTnR



→ capturing Events:-

- i> rising Edge
- ii> falling Edge
- iii> Or both



→ To place timer in Edge count mode

TnCMR bit = 0 in GPTMTnMR

→ type of Edge

TnEVENT field in GPTMCTL

→ No. Edge events count in down count mode

Value in (GPTMTnILR + PR) - Value in

↑

(GPTMTnMR + PMR)

↑

→ Vice versa for up count.

Table 11-8. Counter Values When the Timer is Enabled in Input Edge-Count Mode

Register	Count Down Mode	Count Up Mode
GPTMTnR	GPTMTnPR in combination with GPTMTnILR	0x0
GPTMTnV	GPTMTnPR in combination with GPTMTnILR	0x0
GPTMTnPS	GPTMTnPR	0x0
GPTMTnPV	GPTMTnPR	0x0

→ When TnEN = 1

timer starts counting & enable for event capture

→ Each input Event on CCP pin decrements or increments the counter by 1 until the event count matches GPTMnMATCHR & PMR.

→ when counts match

CnMRIS = 1 --- Raw interrupt statu.

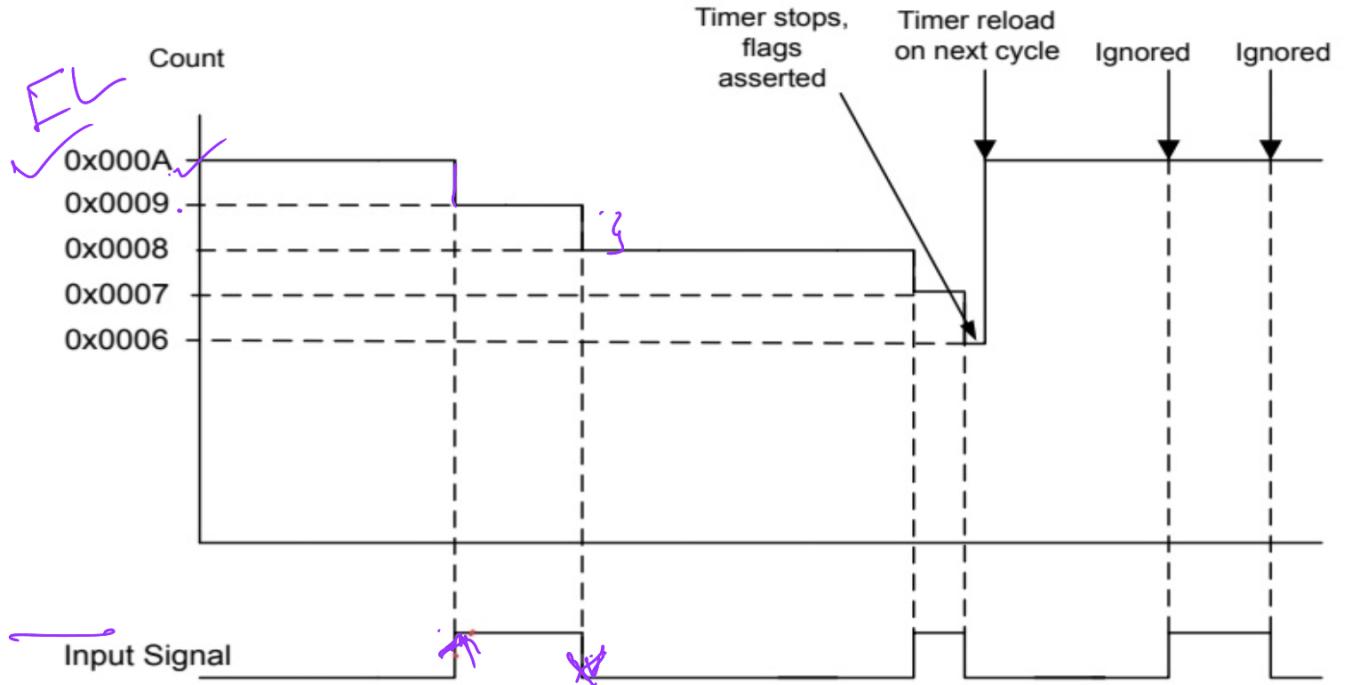
→ GPTMTnR & GPTMTnPS hold value of input events. GPTMTnV & GPTMTnPV holds free running value of counter

→ for up-count = GPTMTnR & GPTMTnV

→ After match value reached

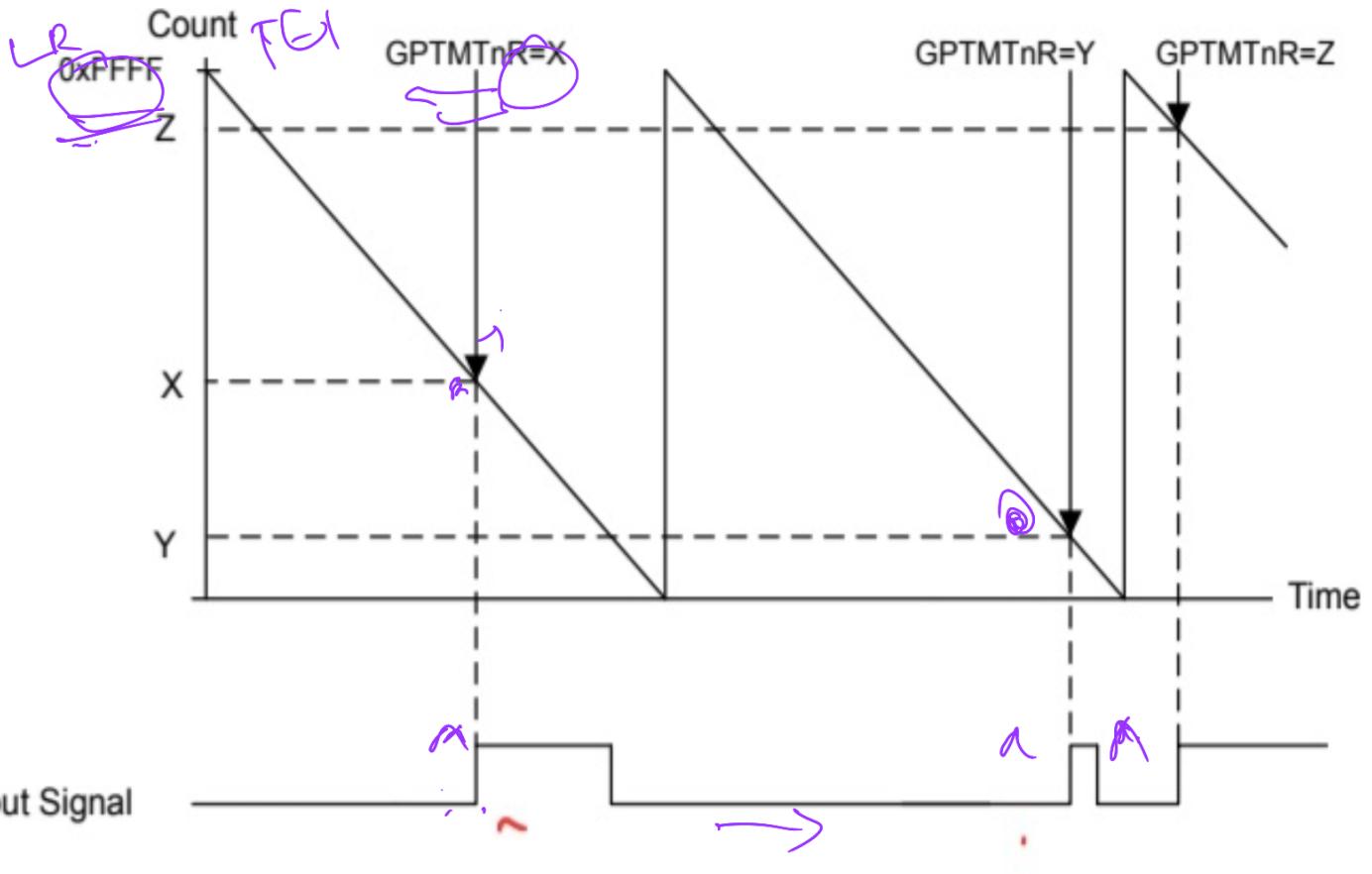
Counter reloaded with ILR & PR & GPTM stops because TnEN = 0.

Figure 11-3. Input Edge-Count Mode Example, Counting Down



* Input Edge time mode :- ✓

- configuration is same as Edge count
- GPTM TnR and GPTM TnPS holds the time at which the selected input event occurred
- GPTM TnV & GPTM TnPv holds free running value
- After Event capture, timer does not stop counting. it continue to count until TnEn = 0
- When time reaches timeout it reloaded with 0x0 in up count & ILR+PR in down count.



① If there is possibility the edge could take longer than count, then another timer configured in periodic timer mode to ensure detection of missing edge.

Criteria: i) periodic timer cycle rate should be same as edge-time timer.

ii) interrupt pos > Time out interrupt pos.

iii) In ISR or periodic time interrupt check timeout interrupt pending or not. If yes counter value -1.

Initialization and configuration:-

1. Make time disable first $TnEN = 0$ ✓
2. $GPTMCFG = 0x0000.0000$ ✓
3. GPTM n MR Register
 $TnMR$ field
 - $0x1$ = one shot
 - $0x2$ = periodic
 - .
4. Optionally:
 ~~$TnSNAPS$, $TnWDT$, $TnMTE$, $TnCDTR$~~
5. Load ILR ✓ from music
6. if interrupt required set ~~GPTM n MR~~
7. $TnEN = 1$. ✓
8. GPTM RIS poll or wait for interrupt to occur.
9. Handler ✓
10. Clear RIS trigger bit. ✓

- Attendance
- 21) 21)
- 1) Present 11)
2) Present 12) Present
3) Present 13) Present
4) Present 14) Present
5) Present 15) Present
6) Present 16) Present
7) Present 17) Present
8) Present 18) Present
9) Present 19) Present
10) Present 20) Present