DWG. NO. | REV. | SHT.

| ECN | DESCRIPTION | REV | DATE |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |

## ANALOG SIGNALS

- reversing polarity variable amplitude analog signal
- fixed polarity variable amplitude analog signal
- fixed polarity constant amplitude analog signal
- current regulated passive recovery stimulus pulse
- biopotential signal
- radiofrequency link
- near field link

## DIGITAL SIGNALS

- high level true
- low level true
- pulse width modulated

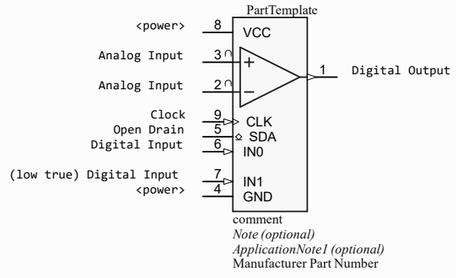
## MIXED SIGNALS

- FESCAN bus power and data signal

## ANALOG CURRENT FLOW or DIGITAL SIGNAL DIRECTION

- bidirectional
- unidirectional
- unidirectional

## COMPONENT LABELLING



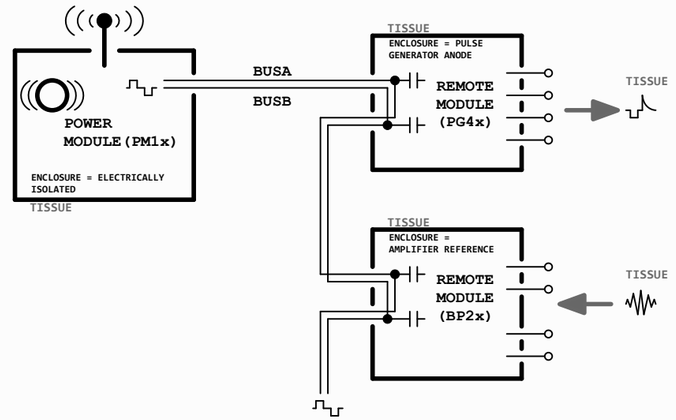

## MODULE SYSTEMS

```
MODULE SYSTEM GROUPING
----
-x,-1x non-tissue interfaces
-2x power conditioning
-3x internal energy systems
-4x processing
-6x tissue interfaces


MODULE SYSTEMS LIST
----
-1 MODULE HEADER SYSTEM
-2 ENCLOSURE THERMISTOR SYSTEM
-3 TEST HEADER SYSTEM
-11 CPLD SYSTEM
-12 NETWORK DRIVE SYSTEM
-13 NETWORK CURRENT SENSE SYSTEM
-14 RADIO SYSTEM

-21 NEAR FIELD LINK SYSTEM
-22 4V6 POWER SUPPLY SYSTEM
-23 MODULE CURRENT SENSE SYSTEM
-24 3V3 POWER SUPPLY SYSTEM
-25 N3V3 POWER SUPPLY SYSTEM
-26 1V8 POWER SUPPLY SYSTEM
-27 NETWORK POWER SUPPLY SYSTEM

BATTERY CONDITIONING SYSTEMS
-31 BATTERY 1 CONDITIONING SYSTEM
-32 BATTERY 2 CONDITIONING SYSTEM
-33 BATTERY 3 CONDITIONING SYSTEM

-41 UCONTROLLER SYSTEM
-42 DIGITAL PERIPHERAL SYSTEM
-43 ANALOG PERIPHERAL SYSTEM
-44 I2C MULTIPLEXING SYSTEM
```

## DESIGN NOTES

1) 3V3 and GND are global power objects and not shown for clarity
2) Unless otherwise specified, all resistors have 1% tolerance

## TYPICAL APPLICATION




## DESIGN RATINGS

| | _Parent | _Min | _Nom | _Max | _Units | _Desc |
|---|---|---|---|---|---|---|
| _DRT1 | VSYS | 2.6 | 4.6 | 5.5 | V | Min from LTC4411,Max from LM3670MF-1.8 and LTC3440 |
| _DRT2 | VBR | 6.3 | 20 | 34 | V | Min,Max from LT1933 |
| _DRT3 | VREC | 6.3 | 20 | 34 | V | Min,Max from LT1933 |
| _DRT4 | VNET | 4.5 | | 10 | V | Min from EL7156,Max from LT3464 on PG4 |
| _DRT11 | P0.7 | | 3.3 | | V | P0.7 set high to enable SPI master. |
| _DRT12 | P0.20 | | 3.3 | | V | P0.20 set high to enable SPI master. |
| _DRT13 | P1.20 | | 3.3 | | V | P1.20 set high to disable TRACE port. |
| _DRT14 | P1.26 | | 0 | | V | P1.26 has interanl PUP. |

| APPROVALS | DATE |
|---|---|
| ENG: R. Yoder | 7-19-2018 |
| DSN: K. Kowalski | 4-12-2022 |
| CHK: T. Crish | 4-12-2022 |
| REFERENCE DOCUMENTS | |
| BOM: * | |
| ASSY DWG: 51-2001 | |
| FAB DWG: * | |
| PCB DWG: 52-2001 | |

SYNAPSE Biomedical Inc.

PROJECT REVISION: * | DOCUMENT REVISION: * | DESIGN ITEM: *

TITLE: Concept 1

SIZE: B | DWG NO.: 51-2001-01-2 | REV: 4

SCALE: * | FILE NAME: 51-2001-01-2_04.SchDoc | SHEET 2 OF 18