CS 3220

Processor Design

Lab Report

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Questions

1. Design options and approaches that you have taken

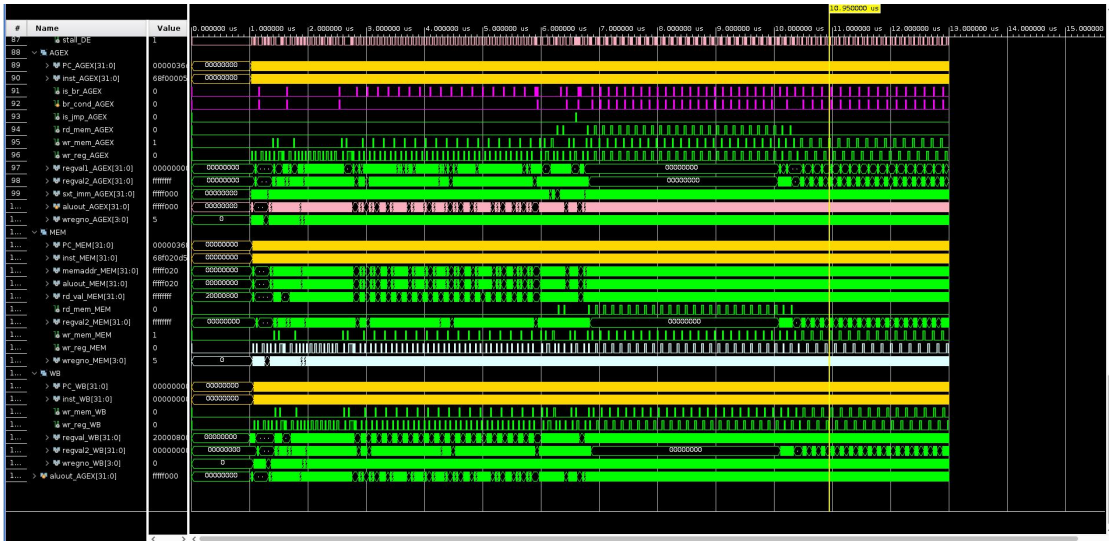
   The overall approach I have taken is incremental. The approximate route I have taken is organizing code -> implement register write-back -> ALU switch statement -> stall logic -> jump logic. Frequent compilation and waveform testing made it easier to make progress without having to worry underlying problems.

   I have taken several measures to make my design process easier.

   a) Good naming practice. I named all my signals in the following format to aid code readability: <signal name>_(from_<stage generated>)_<STAGE IN>. For example:

   ```
   wire dependency_stall_DE
   wire wr_reg_from_agex_DE
   ```

   b) Well organized waveform. I divided all signals into stages and assigned them different colors depending what purpose they serve.



   c) Frequent push to Github after completing various milestones and code documentation.

2. Problems/issues and how you solved

   Incorrect stalling behavior is the most troublesome problem I have come cross. My resolution to this problem is to draw out my pipeline on paper with stall related signals and try to understand the flow of instructions and stall signals. With this approach, I was able to identify the cause of the problem: I did not apply separate stall behavior to the two types of stall (dependency stall and jump/branch stall).

3. Contribution to the project: What you have done and what percentage your contribution is.

   I am a single-member team, so EVERYTHING.

Pipeline design graph