Chang-Pao Chang

E-mail: chang.pao.chang@gmail.com
Cell: +886-915-646091
Website: http://cpchang.github.io/
Linkedin: http://tw.linkedin.com/pub/chang-bao-chang/69/8a5/758

RESEARCH INTEREST

● Signal/Power Integrity, ● Linear/Non-linear Optimization ● Finite Element / Boundary Element / Meshfree Method

EDUCATION

National Taiwan University (NTU), Taipei, Taiwan

- Bachelor of Science in Electrical Engineering — Sep.2006 – Jun.2010
- Master of Science in Communication Engineering (GPA 4.29/4.3, Ranked **5** of 114) — Sep.2011 – Jun.2013

PUBLICATION

Journal Papers

[1] K.-Y. Yang, **C.-P. Chang**, T.-Y. Wu, W.-S. Wang, Y.-H. Lin, R.-B. Wu, "*Modeling and fast eye-diagram estimation of ringing effects on branch line,*" *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol.4, no.4, pp.641,647, April 2014

Conference Papers

[2] **C.-P. Chang**, M.-K. Kang, T.-Y. Huang, K.-B. Wu, R.-B. Wu, "*A Novel Noise Mitigation Design for TSV-to-Device Coupling Using Power Distribution Network,*" *Electrical Performance of Electronic Packaging and Systems (EPEPS), 2014 IEEE 23rd Conference,* Oct. 2014.

[3] W.-C. Chen, **C.-P. Chang**, M.-K. Kang, T.-Y. Huang, K.-B. Wu, R.-B. Wu, "*Artificial Neural Network Modeling for Extrinsic Capacitance of FinFET,*" *Electrical Performance of Electronic Packaging and Systems (EPEPS), 2014 IEEE 23rd Conference,* Oct. 2014.

[4] **C.-B. Chang**, T.-Y. Huang, M.-C. Wu, R.-B. Wu, "*Inductance Modeling of TSV for time domain simulation*," in 2013 Asia-Pacific Radio Science Conference (AP-RASC), 2013.

[5] K.-B. Wu, **C.-B. Chang**, M.-C. Wu, R.-B. Wu, "*Simplified Array Model of Vertical Interconnect in Through-Silicon-Via Application*," in 2013 Asia-Pacific Radio Science Conference (AP-RASC), 2013.

[6] Y.-C. Tseng, **C.-B. Chang**, C.-K. Tang, C.-H. Cheng, Y.-C. Lu, K.-Y. Lin, T.-L. Wu, and R.-B. Wu, *"Design considerations for radio frequency 3DICs,"* E*lectrical Design of Advanced Packaging and Systems Symposium (EDAPS), 2012 IEEE* , vol., no., pp.197,200, 9-11 Dec. 2012.

Books

[7] **C.-B. Chang**, [A Detailed Explanation on Basic Electrical Science], GreatBooks Co. Ltd., Aug. 2012, ISBN: 978-986-7015-86-0. (in Chinese)

RESEARCH EXPERIENCE

- **National Taiwan University, Dept. of Electrical Engineering, Taipei, Taiwan.** — Jul.2013 – Aug.2014
  Position: Research Assistant
  Project: *3D Transistors and 3D Interconnects for Advanced VLSI System*. [2][3]
  - Collaboration between five different fields: nano-electronic, material science, thermal & mechanical engineering, computer-aid design, electromagnetic design.
  - Analysis and design of clock distribution network in 3D IC considering thermal and stress effect.
  - Developing parallel computer system for very large scale electromagnetic simulation.

- **Taiwan Semiconductor Manufacturing Company (TSMC), Taipei, Taiwan.** — Jul.2012 – Sep.2012
  Position: Intern, Dept. of PDK, Division of Design Technology Platform (DTP)
  - Analyzed and developed electrical model in Process Design Kit (PDK) for radio frequency (RF) IC in sub-micron process.
  - Developed Electrical Model for Three-Dimensional IC (3D IC).

PROJECTS

- **3D Transistors and 3D Interconnects for Advanced VLSI System** — Sep.2012 – Jun.2014
  - *Cooperate with: National Science Council, Taiwan*
  - Developed an efficient modeling method for very-large TSV array using cylindrical function.
  - Developed a novel optimization method for noise mitigation in 3D IC and for 3D transistors. [2][3]

- **Electrical Modeling and Design for TSV array in Wide IO** Feb.2012 – Aug.2014
  - *Cooperate with: MediaTek (MTK), Taiwan*

- Analyzed electrical model in electromagnetic and semiconductor aspect.
- Developed efficient tools and methods for next generation 3D stacking memory. [4]

- **Modeling of power-ground planes and optimization of decoupling capacitors** Sep.2011 – Dec.2011
  - *Cooperate with: AVerMedia, Taiwan*
  - Integrated optimization algorithm into commercial tools. [1]

- **Modeling, Simulation, and Design for TSV Interconnects & Substrate Noise Coupling in 3D IC Stacking Application.**
  - *Cooperate with: Taiwan Semiconductor Manufacturing Company (TSMC)* Sep.2011 – Feb.2012
  - Developed efficient methods to model three-dimensional integrated circuit (3D IC). [5]

- **Signal Integrity Analysis and Design in 3D IC Packaging** Sep.2011 – Jun.2013
  - *Cooperate with: National Science Council, Taiwan*
  - Developed a fast power/signal/ground through silicon via optimization algorithm for 3D IC integration. [6]

SELECTED EXTRACURRICULAR

- Member, Swimming Team, NTU. Sep.2006 – Jun.2010.
- Captain , Swimming Team, NTU. Jul. 2009 – Jun.2010.

SKILLS & LANGUAGE

- Languages: Mandarin (Native Fluency); English (Excellent Fluency); Japanese (Basic Fluency)
- Computer programming: Git/Github, C/C++, HTML5/CSS3/js, VBScript, Matlab® , Intel MPI Library.