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## Education

National Taiwan University (NTU), Taipei, Taiwan

* Bachelor of Science in Electrical Engineering (GPA 81.99/100, 3.7/4.3 Ranked 142 of 224) 09/2006 – 06/2010
* Master of Science in Communication Engineering (GPA 4.29/4.30, Ranked 5 of 114) 09/2011 – 06/2013

## professional experience

* **Taiwan Semiconductor Manufacturing Company (TSMC), Taipei, Taiwan.** 07/2012 – 09/2012   
  Position: Intern, Dept. of PDK, Division of DTP (Design Technology Platform)
  + Analyzed and developed electrical model in Process Design Kit (PDK) for radio frequency (RF) IC in sub-micron process.
  + Developed Electrical Model for Three-Dimensional IC (3D IC).
* **National Taiwan University, Dept. of Electrical Engineering, Taipei, Taiwan** 07/2013 – Now  
  Position: Executive Assistant  
  Project: *3D Transistors and 3D Interconnects for Advanced VLSI System*, National Science Council.
  + Managing team of five different fields: nano-electronic, material science, thermal & mechanical engineering, computer-aid design, electromagnetic design.
  + Analysis and design of clock distribution network in 3D IC considering thermal and stress effect.
  + Developing parallel computer network for very large scale electromagnetic simulation.

## publication

* Y.-C. Tseng, **C.-B. Chang**, C.-K. Tang, C.-H. Cheng, Y.-C. Lu, K.-Y. Lin, T.-L. Wu, and R.-B. Wu, *“Design considerations for radio frequency 3DICs,”* in 2012 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), 2012, pp. 197–200.
* K.-B. Wu, **C.-B. Chang**, M.-C. Wu, R.-B. Wu, “*Simplified Array Model of Vertical Interconnect in Through-Silicon-Via Application*,” in 2013 Asia-Pacific Radio Science Conference (AP-RASC), 2013.
* **C.-B. Chang**, T.-Y. Huang, M.-C. Wu, R.-B. Wu, “*Inductance Modeling of TSV for time domain simulation*,” in 2013 Asia-Pacific Radio Science Conference (AP-RASC), 2013.
* K.-Y. Yang, **C.-B. Chang**, T.-Y. Wu, W.-S. Wang, Y.-H. Lin, R.-B. Wu, “*Modeling and fast eye-diagram estimation of ringing effects on branch line,*” *IEEE Trans. Compon. Packag. Manuf. Technol. IEEE Transactions on* , vol.4, no.4, pp.641,647, April 2014

## ProjectS

* **AVerMedia** 09/2011 – 12/2011*Modeling of power-ground planes and optimization of decoupling capacitors* 
  + Integrated optimization algorithm into commercial tools.
* **Taiwan Semiconductor Manufacturing Company (TSMC)** 09/2011 – 02/2012   
  *Modeling, Simulation, and Design for TSV Interconnects & Substrate Noise Coupling in 3D IC Stacking Application.* 
  + Developed efficient methods to model three-dimensional integrated circuit (3D IC).
* **National Science Council, Taiwan (R.O.C)** 09/2011 – 06/2013  
  *Signal Integrity Analysis and Design in 3D IC Packaging*
  + Developed a fast power/signal/ground through silicon via placing algorithm in 3D IC integration
* **National Science Council, Taiwan (R.O.C)** 09/2012 – 06/2013  
  *3D Transistors and 3D Interconnects for Advanced VLSI System*
  + Developed an efficient modeling method for very-large TSV array using cylindrical function.
* **MediaTeK (MTK)** 02/2012 – Now  
  *Electrical Modeling and Design for TSV array in Wide IO*
  + Analyzed electrical model in electromagnetic and semiconductor aspect.
  + Developed efficient tools and methods for next generation 3D stacking memory.

## selected extracurricular

2006-2009, Member, Swimming Team, NTU.

2009-2010, Captain, Swimming Team, NTU.

## skills

Languages: Mandarin (Native Fluency); English (Excellent Fluency); Taiwanese / Japanese (Basic Fluency)

Computer programming: C, C++, HTML, javaScript, VBScript, Matlab®, Wolfram Mathematica®