Lab Report #02

2021.05.11. 실험 보고서

과   목 : 논리회로설계및실험

분   반 : 공통

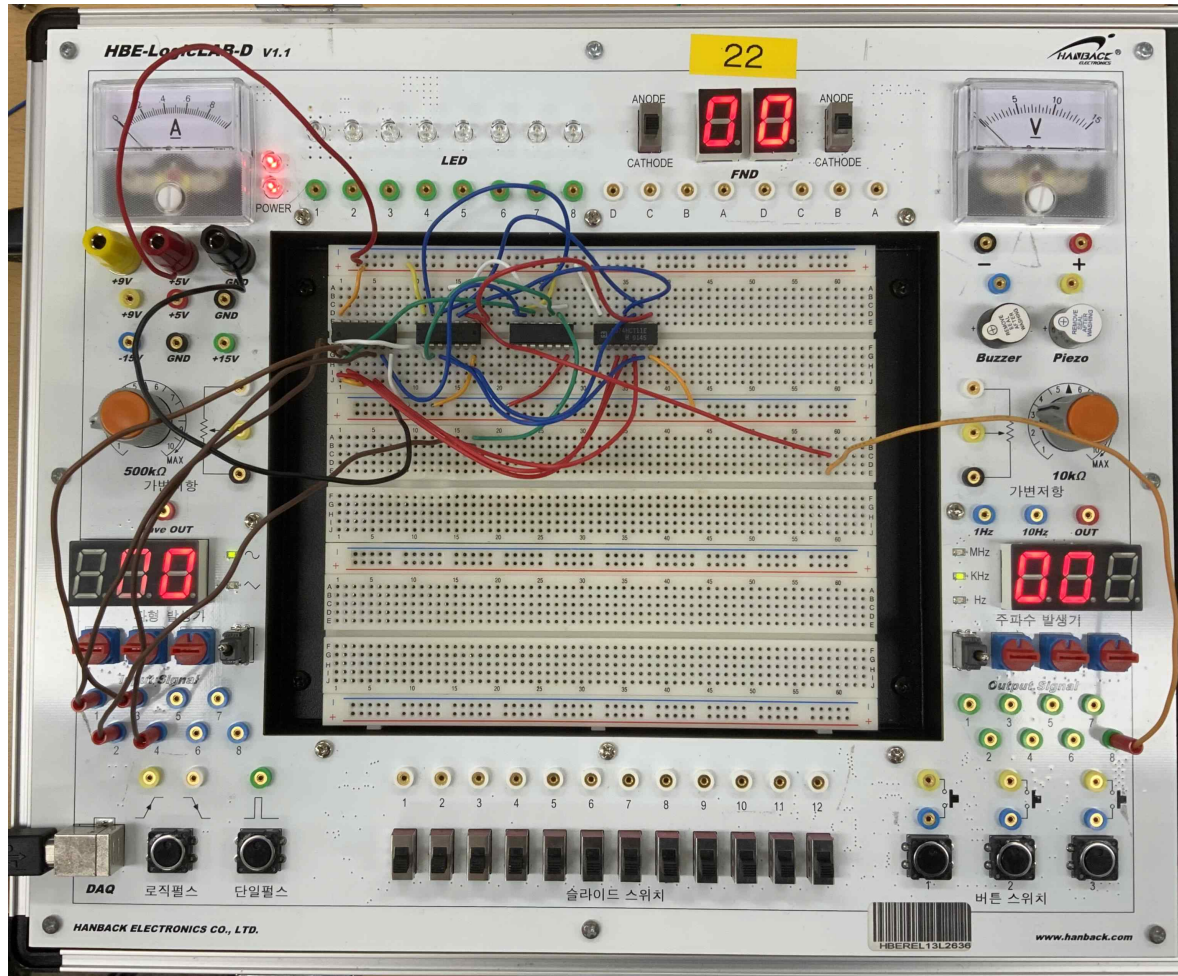담당교수 : 김석윤교수님

실 험 일 : 2021.05.11.
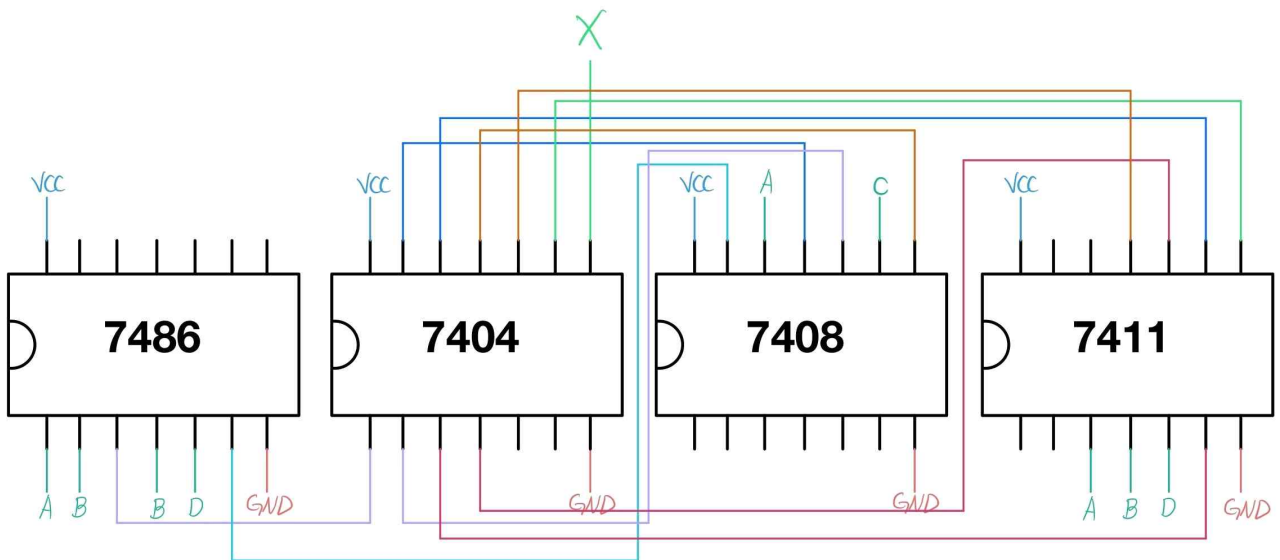
조 번 호 : 22

학   번 : 20163340   20193438

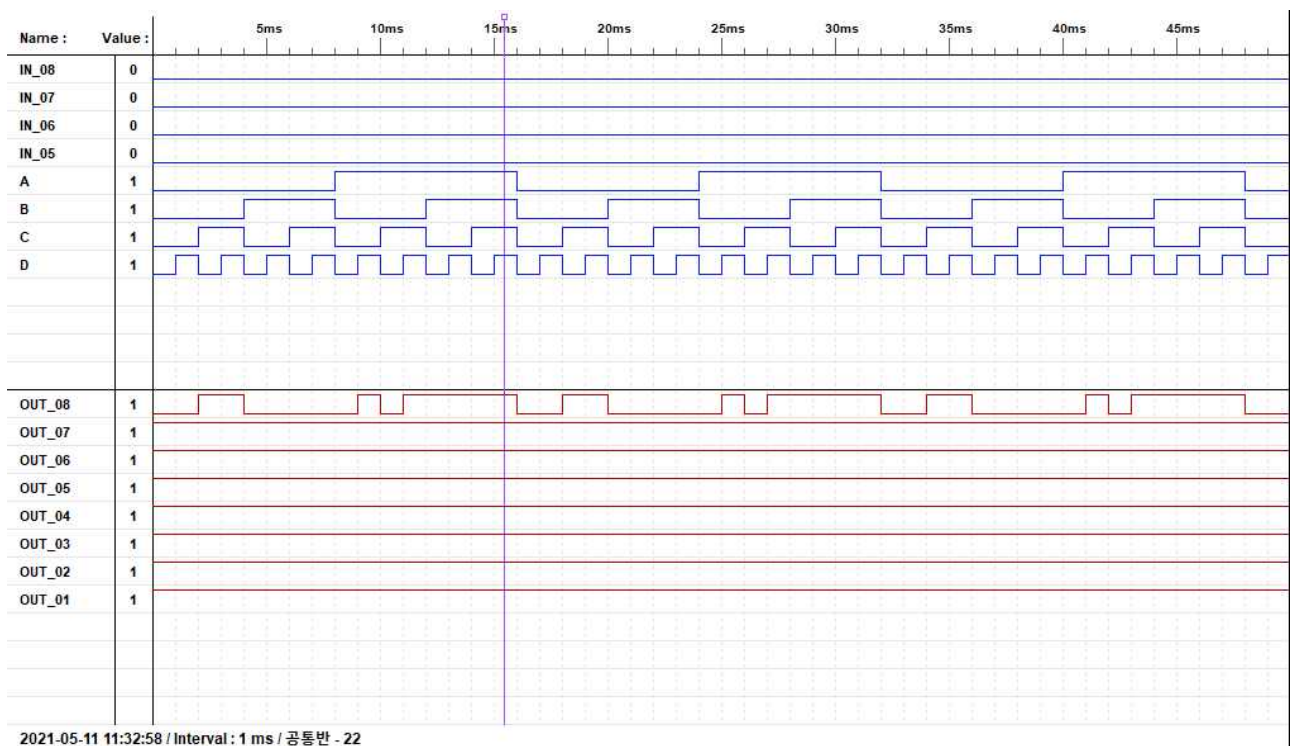이   름 : 강 원 경   이 민 철

1)

HBE-LogicalLab-D 사진

회로도

A	B	C	D	B⊕D	(A⊕B)'	A·(B⊕D)	(A⊕B)'·C	A·B·D	X
0	0	0	0	0	1	0	0	0	0
0	0	0	1	1	1	0	0	0	0
0	0	1	0	0	1	0	1	0	1
0	0	1	1	1	1	0	1	0	1
0	1	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	0	1
1	0	1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	0	0	1
1	1	0	0	1	1	1	0	0	1
1	1	0	1	0	1	0	0	1	1
1	1	1	0	1	1	1	1	0	1
1	1	1	1	0	1	0	1	1	1

진리표

2021-05-11 11:32:58 / Interval : 1 ms / 공통반 - 22

f1) Canonical form (Sum-of-Products) :

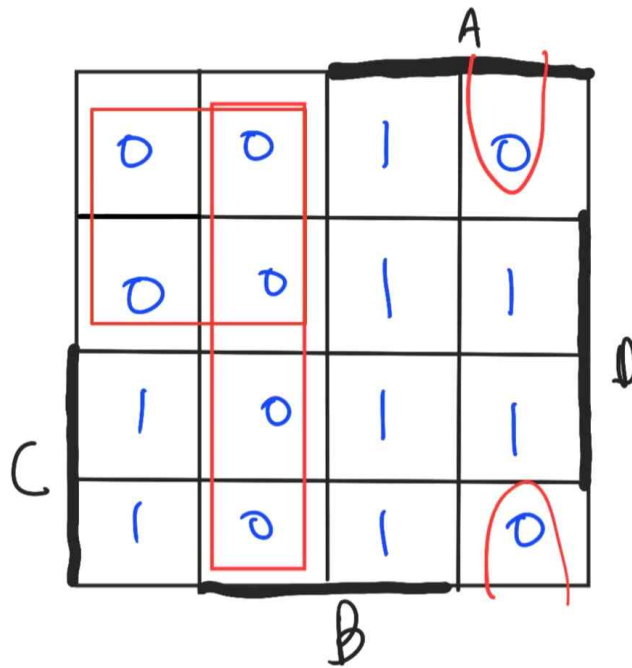0010 + 0011 + 1011 + 1100 + 1101 + 1110 + 1111

$$= \sum m(2,3,9,11,12,13,14,15)$$

f2) Canonical form (Product-of-Sums) :

0000 + 0001 + 0100 + 0101 + 0110 + 0111 + 1000 + 1010
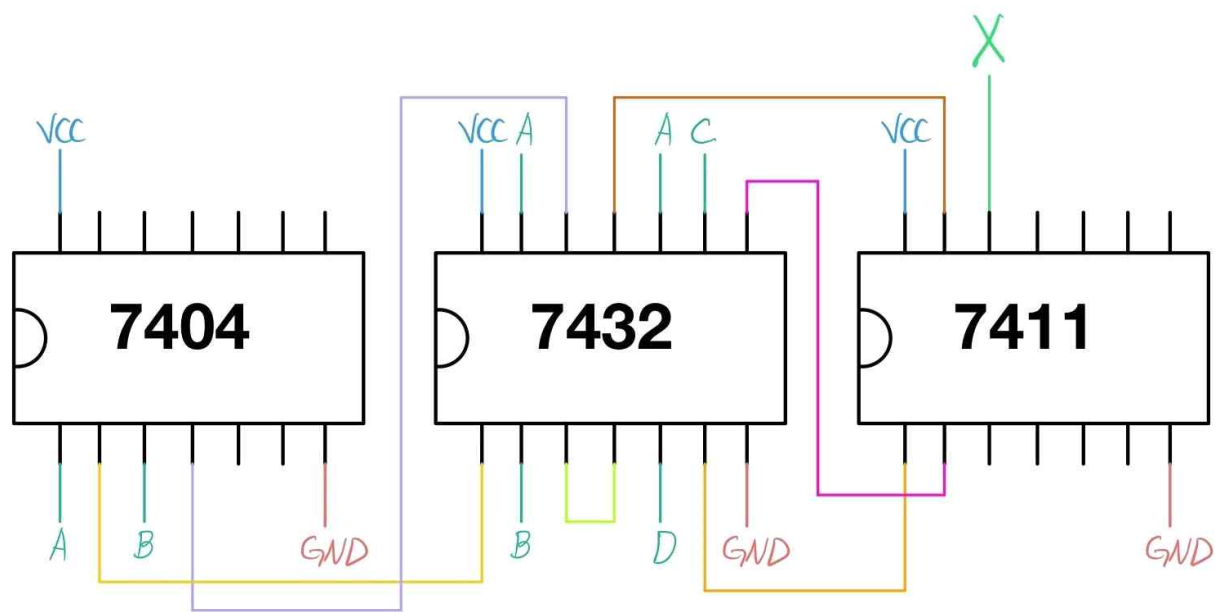
$$= \prod M(0,1,4,5,6,7,8,10)$$

2)

Minimized product of sums : (A′+B+D)(A+B′)(A+C)

A	B	C	D	A′+B+D	A+B′	A+C	X
0	0	0	0	1	1	0	0
0	0	0	1	1	1	0	0
0	0	1	0	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	0	1	0	0	0
0	1	0	1	1	0	0	0
0	1	1	0	1	0	1	0
0	1	1	1	1	0	1	0
1	0	0	0	0	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	1	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	1
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1

진리표

회로도

3)

Minimized sum of products : AB+AD+A′B′C
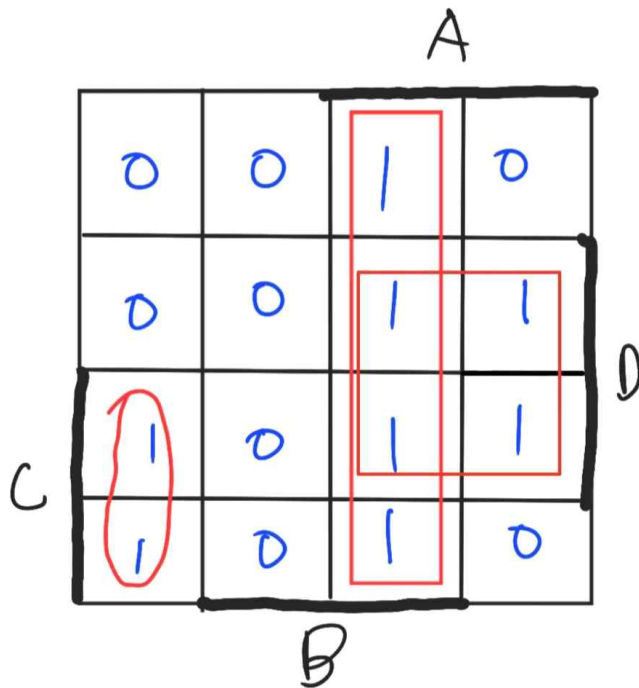
A	B	C	D	AB	AD	A′B′C	X
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	1
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	0	0
1	0	1	1	0	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	1	0	1
1	1	1	0	1	0	0	1
1	1	1	1	1	1	0	1

진리표

회로도