Lab Report #01

2021.05.04. 실험 보고서

과 목: 논리회로설계및실험

분 반: 공통

담당교수 : 김석윤과

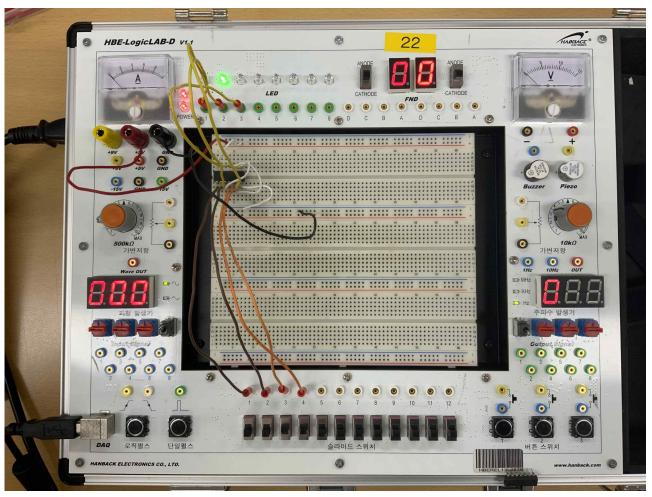
실 험 일: 2021.05.04.

조 번 호 : 22

학 번: 20163340 20193438

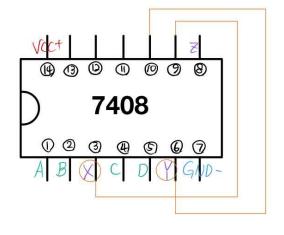
이 름: 강원경 이민철

[그림 6]



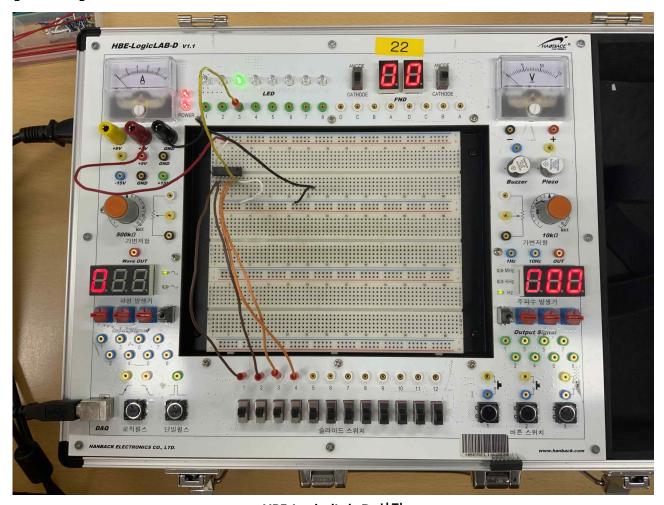
HBE-LogicalLab-D 사진

Α	В	С	D	Х	Υ	Z
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0 1	0	0	0
0	1	1	1	0	1	0
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	1	1



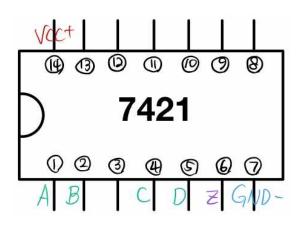
진리표 회로도

[그림 7]



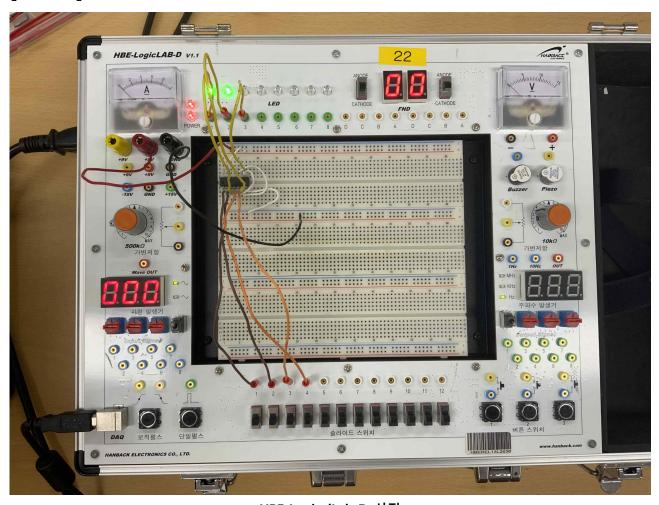
HBE-LogicalLab-D 사진

Α	В	С	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



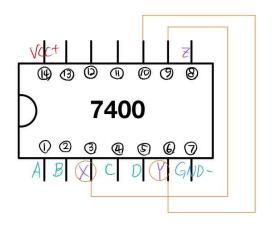
진리표 회로도

[그림 8]



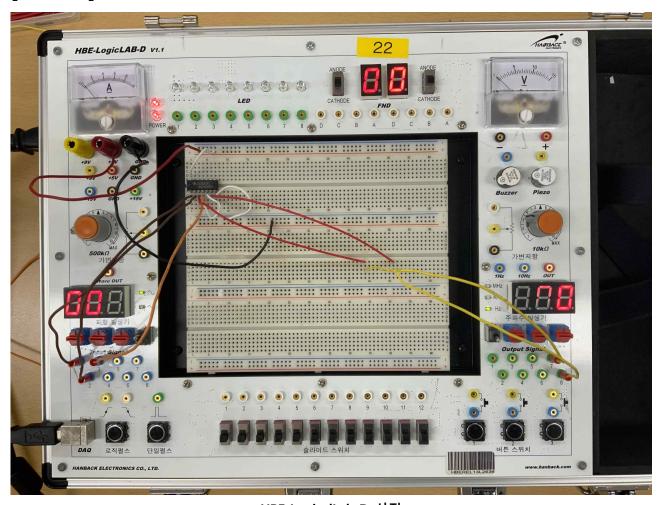
HBE-LogicalLab-D 사진

Α	В	С	D	X	Υ	Z
0	0	0	0	1	1	0
0	0	0	1	1	1	0
0	0	1	0	1	1	0
0	0	1	1	1	0	1
0	1	0	0	1	1	0
0	1	0	1	1	1	0
0	1	1	0	1	1	0
0	1	1	1	1	0	1
1	0	0	0	1	1	0
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	0	0	1



진리표 회로도

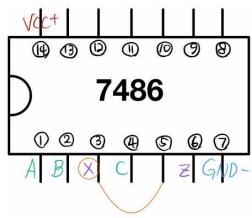
[그림 10]



HBE-LogicalLab-D 사진

В	С	X	Z
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0	1	0	1
1	0	1	1
1	1	1	0
0	0	1	1
0	1	1	0
1	0	0	0
1	1	0	1
	0 0 1 1	0 0 0 1 1 0 1 1 0 0 0 1 1 0	0 0 0 1 1 0 1 1 1 1 0 0 1 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0





회로도



파형 사진