20. TCA - 16-bit Timer/Counter Type A

20.1 Features

- 16-Bit Timer/Counter
- Three Compare Channels
- Double-Buffered Timer Period Setting
- Double-Buffered Compare Channels
- Waveform Generation:
  - Frequency generation
  - Single-slope PWM (Pulse-Width Modulation)
  - Dual-slope PWM
- Count on Event
- Timer Overflow Interrupts/Events
- One Compare Match per Compare Channel
- Two 8-Bit Timer/Counters in Split Mode

20.2 Overview

The flexible 16-bit PWM Timer/Counter type A (TCA) provides accurate program execution timing, frequency and waveform generation, and command execution.

A TCA consists of a base counter and a set of compare channels. The base counter can be used to count clock cycles or events, or let events control how it counts clock cycles. It has direction control and period setting that can be used for timing. The compare channels can be used together with the base counter to do compare match control, frequency generation, and pulse-width waveform modulation.

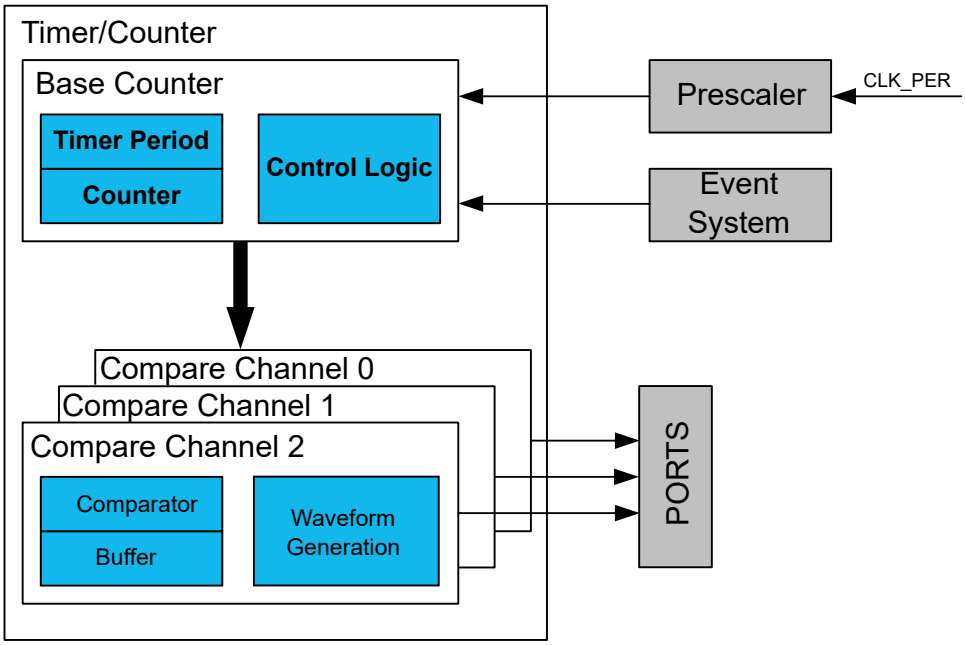
Depending on the mode of operation, the counter is cleared, reloaded, incremented, or decremented at each timer/counter clock or event input.

A timer/counter can be clocked and timed from the peripheral clock, with optional prescaling, or from the Event System. The Event System can also be used for direction control or to synchronize operations.

By default, the TCA is a 16-bit timer/counter. The timer/counter has a Split mode feature that splits it into two 8-bit timer/counters with three compare channels each.

A block diagram of the 16-bit timer/counter with closely related peripheral modules (in grey) is shown in the figure below.

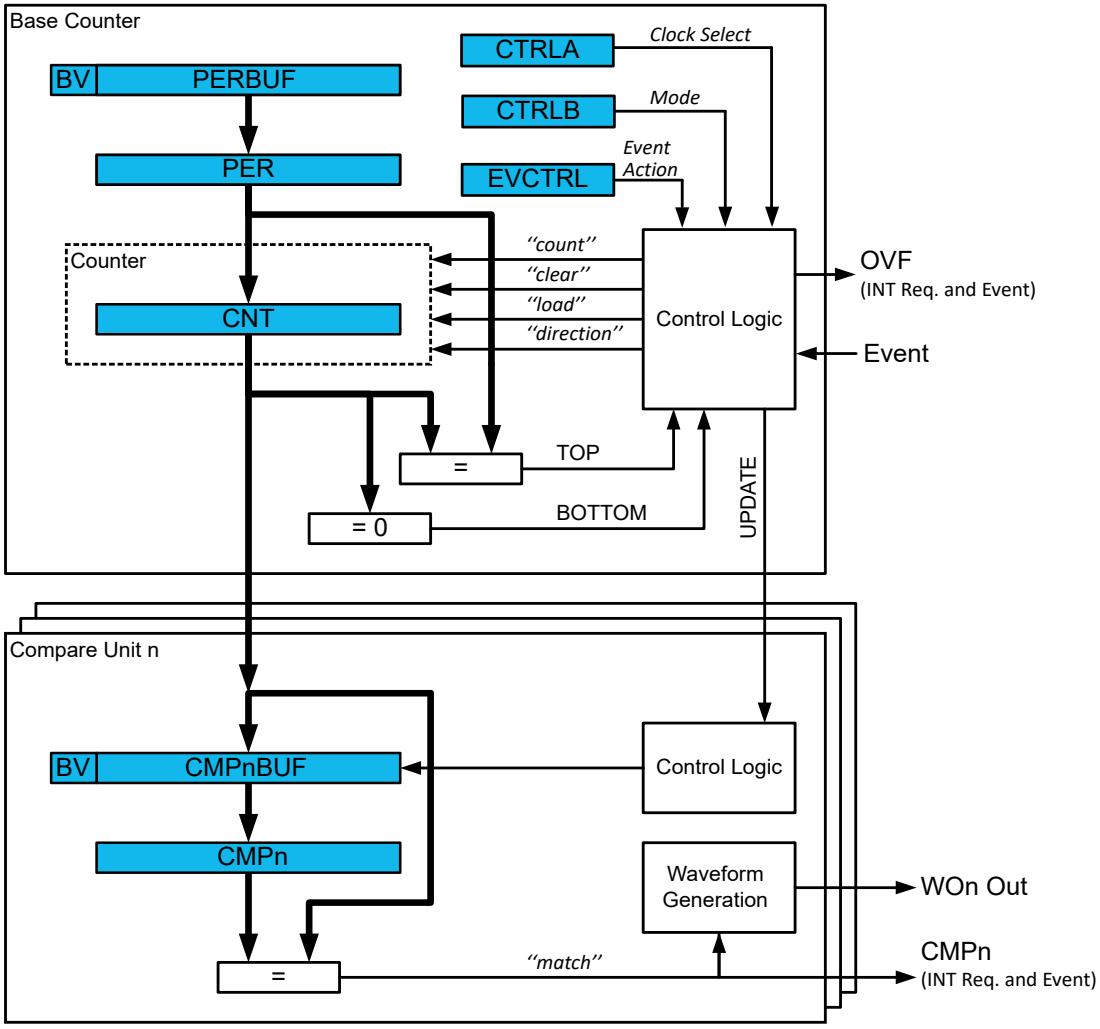
Figure 20-1. 16-bit Timer/Counter and Closely Related Peripherals



20.2.1 Block Diagram

The figure below shows a detailed block diagram of the timer/counter.

Figure 20-2. Timer/Counter Block Diagram



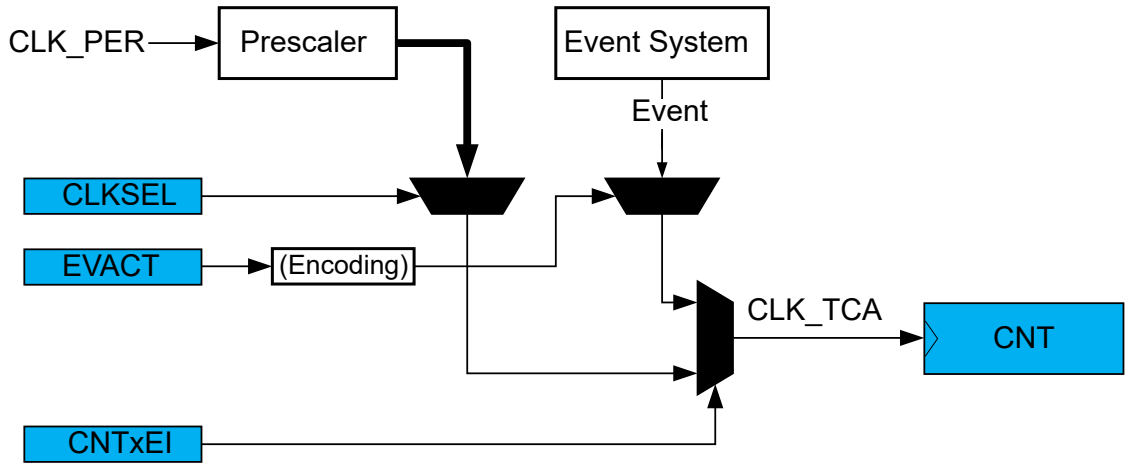
The Counter register (TCAn.CNT), Period and Compare registers (TCAn.PER and TCAn.CMPm) and their corresponding buffer registers (TCAn.PERBUF and TCAn.CMPBUFm) are 16-bit registers. All buffer registers have a Buffer Valid (BV) flag that indicates when the buffer contains a new value.

During normal operation, the counter value is continuously compared to zero and the period (PER) value to determine whether the counter has reached TOP or BOTTOM.

The counter value is also compared to the TCAn.CMPm registers. These comparisons can be used to generate interrupt requests. The Waveform Generator modes use these comparisons to set the waveform period or pulse width.

A prescaled peripheral clock and events from the Event System can be used to control the counter as shown in the figure below.

Figure 20-3. Timer/Counter Clock Logic



20.2.2 Signal Description

Signal	Description	Type
WOn	Digital output	Waveform output

20.3 Functional Description

20.3.1 Definitions

The following definitions are used throughout the documentation:

Table 20-1. Timer/Counter Definitions

Name	Description
BOTTOM	The counter reaches BOTTOM when it becomes 0x0000.
MAX	The counter reaches MAXimum when it becomes all ones.
TOP	The counter reaches TOP when it becomes equal to the highest value in the count sequence.
UPDATE	The update condition is met when the timer/counter reaches BOTTOM or TOP, depending on the Waveform Generator mode. Buffered registers with valid buffer values will be updated unless the Lock Update bit (LUPD) in TCAn.CTRLE has been set.
CNT	Counter register value.
CMP	Compare register value.

In general, the term timer is used when the timer/counter is counting periodic clock ticks. The term counter is used when the input signal has sporadic or irregular ticks. The latter can be the case when counting events.

20.3.2 Initialization

To start using the timer/counter in a basic mode, follow these steps:

1. Write a TOP value to the Period register (TCAn.PER).
2. Enable the peripheral by writing a '1' to the ENABLE bit in the Control A register (TCAn.CTRLA). The counter will start counting clock ticks according to the prescaler setting in the Clock Select bit field (CLKSEL) in TCAn.CTRLA.
3. Optional: By writing a '1' to the Enable Count on Event Input bit (CNTEI) in the Event Control register (TCAn.EVCTRL), events are counted instead of clock ticks.

4. The counter value can be read from the Counter bit field (CNT) in the Counter register (TCAn.CNT).

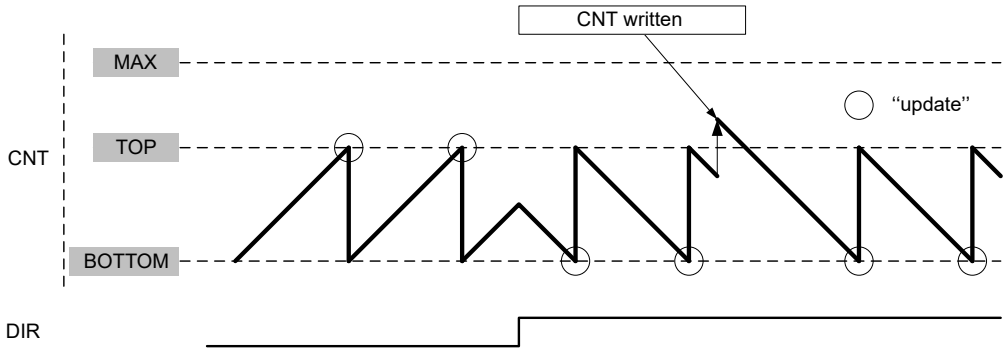
20.3.3 Operation

20.3.3.1 Normal Operation

In normal operation, the counter is counting clock ticks in the direction selected by the Direction bit (DIR) in the Control E register (TCAn.CTRLE), until it reaches TOP or BOTTOM. The clock ticks are given by the peripheral clock (CLK_PER), prescaled according to the Clock Select bit field (CLKSEL) in the Control A register (TCAn.CTRLA).

When TOP is reached while the counter is counting up, the counter will wrap to '0' at the next clock tick. When counting down, the counter is reloaded with the Period register value (TCAn.PER) when BOTTOM is reached.

Figure 20-4. Normal Operation



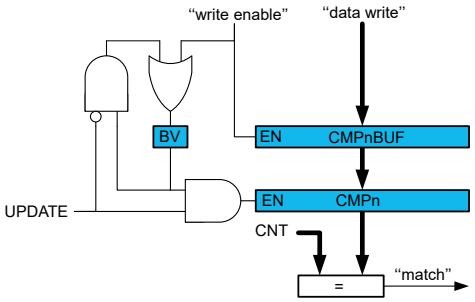
It is possible to change the counter value in the Counter register (TCAn.CNT) when the counter is running. The write access to TCAn.CNT has higher priority than count, clear or reload, and will be immediate. The direction of the counter can also be changed during normal operation by writing to DIR in TCAn.CTRLE.

20.3.3.2 Double Buffering

The Period register value (TCAn.PER) and the Compare n register values (TCAn.CMPn) are all double-buffered (TCAn.PERBUF and TCAn.CMPnBUF).

Each buffer register has a Buffer Valid flag (PERBV, CMPnBV) in the Control F register (TCAn.CTRLF), which indicates that the buffer register contains a valid (new) value that can be copied into the corresponding Period or Compare register. When the Period register and Compare n registers are used for a compare operation, the BV flag is set when data are written to the buffer register and cleared on an UPDATE condition. This is shown for a Compare register (CMPn) in the figure below.

Figure 20-5. Period and Compare Double Buffering



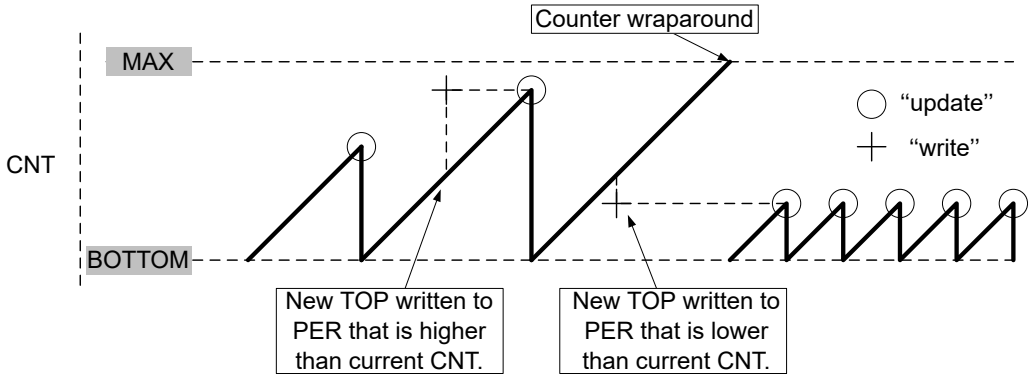
Both the TCAn.CMPn and TCAn.CMPnBUF registers are available as I/O registers. This allows initialization and bypassing of the buffer register and the double-buffering function.

20.3.3.3 Changing the Period

The Counter period is changed by writing a new TOP value to the Period register (TCAn.PER).

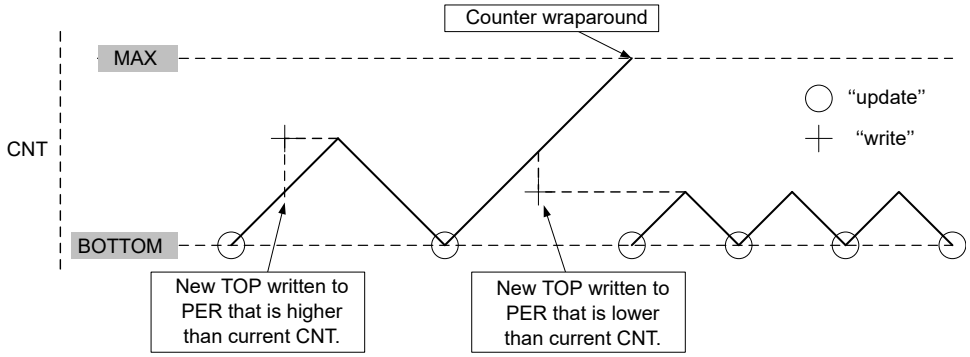
No Buffering: If double-buffering is not used, any period update is immediate.

Figure 20-6. Changing the Period Without Buffering



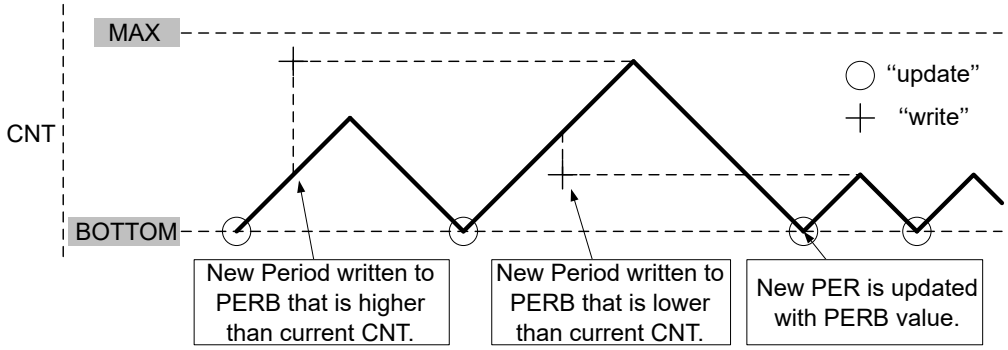
A counter wraparound can occur in any mode of operation when counting up without buffering, as the TCAn.CNT and TCAn.PER registers are continuously compared. If a new TOP value is written to TCAn.PER that is lower than the current TCAn.CNT, the counter will wrap first, before a compare match occurs.

Figure 20-7. Unbuffered Dual-Slope Operation



With Buffering: When double-buffering is used, the buffer can be written at any time and still maintain correct operation. The TCAn.PER is always updated on the UPDATE condition, as shown for dual-slope operation in the figure below. This prevents wraparound and the generation of odd waveforms.

Figure 20-8. Changing the Period Using Buffering



Note: Buffering is used in figures illustrating TCA operation if not otherwise specified.

20.3.3.4 Compare Channel

Each Compare Channel n continuously compares the counter value (TCAn.CNT) with the Compare n register (TCAn.CMPn). If TCAn.CNT equals TCAn.CMPn, the Comparator n signals a match. The match will set the Compare Channel's interrupt flag at the next timer clock cycle, and the optional interrupt is generated.

The Compare n Buffer register (TCAn.CMPnBUF) provides double-buffer capability equivalent to that for the period buffer. The double-buffering synchronizes the update of the TCAn.CMPn register with the buffer value to either the TOP or BOTTOM of the counting sequence, according to the UPDATE condition. The synchronization prevents the occurrence of odd-length, non-symmetrical pulses for glitch-free output.

20.3.3.4.1 Waveform Generation

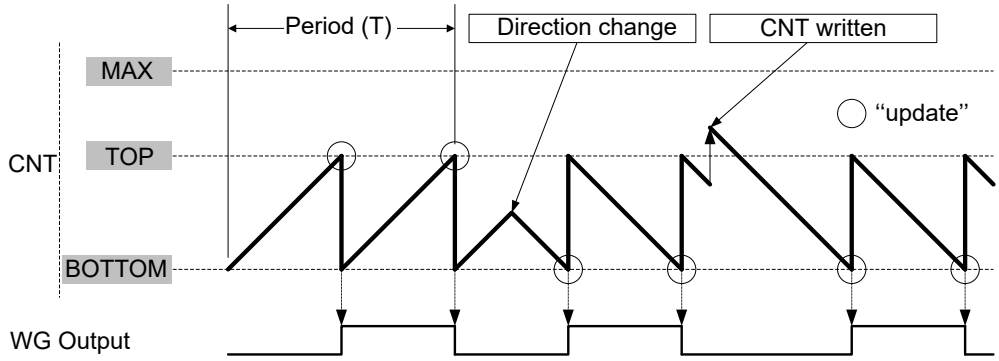
The compare channels can be used for waveform generation on the corresponding port pins. The following requirements must be met to make the waveform visible on the connected port pin:

1. A Waveform Generation mode must be selected by writing the WGMODE bit field in TCAn.CTRLB.
2. The TCA is counting clock ticks, not events (CNTEI = `0` in TCAn.EVCTRL).
3. The compare channels used must be enabled (CMPnEN = `1` in TCAn.CTRLB). This will override the output value for the corresponding pin. An alternative pin can be selected by configuring the Port Multiplexer (PORTMUX). Refer to the *PORTMUX* chapter for details.
4. The direction for the associated port pin n must be configured as an output (PORTx.DIR[n] = `1`).
5. Optional: Enable the inverted waveform output for the associated port pin n (INVEN = `1` in PORTx.PINnCTRL).

20.3.3.4.2 Frequency (FRQ) Waveform Generation

For frequency generation, the period time (T) is controlled by the TCAn.CMP0 register instead of the Period register (TCAn.PER). The corresponding waveform generator output is toggled on each compare match between the TCAn.CNT and TCAn.CMPm registers.

Figure 20-9. Frequency Waveform Generation



The waveform frequency (f_{FRQ}) is defined by the following equation:

$$f_{\mathrm{FRQ}} = \frac{\mathrm{f_{CLK\_PER}}}{2N(\mathrm{CMPn}+1)}$$

where *N* represents the prescaler divider used (CLKSEL in TCAn.CTRLA), and f_{CLK_PER} is the peripheral clock frequency.

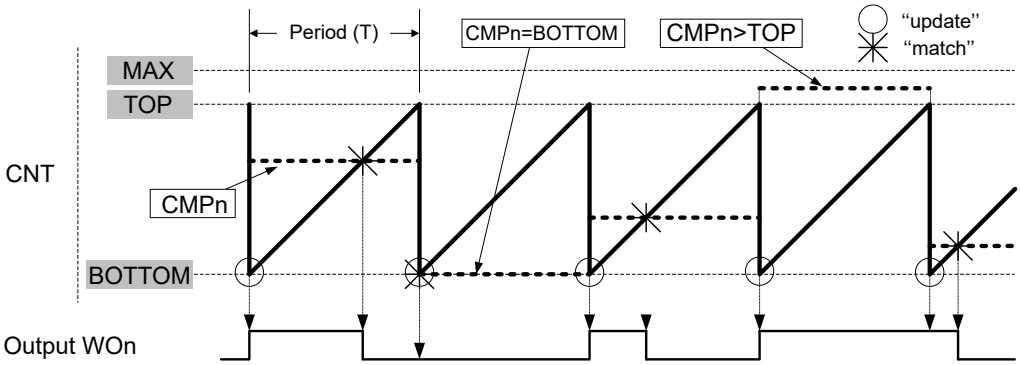
The maximum frequency of the waveform generated is half of the peripheral clock frequency ($f_{CLK\_PER}/2$) when TCAn.CMP0 is written to 0x0000 and no prescaling is used (*N* = `1`, CLKSEL = `0x0` in TCAn.CTRLA).

20.3.3.4.3 Single-Slope PWM Generation

For single-slope Pulse-Width Modulation (PWM) generation the period (T) is controlled by TCAn.PER, while the values of the TCAn.CMPm registers control the duty cycles of the generated waveforms. The figure below shows how the counter counts from BOTTOM to TOP and then restarts from BOTTOM. The waveform generator output is set at BOTTOM and cleared on the compare match between the TCAn.CNT and TCAn.CMPm registers.

CMPn = BOTTOM will produce a static low signal on WOn while CMPn > TOP will produce a static high signal on WOn.

Figure 20-10. Single-Slope Pulse-Width Modulation



The TCAn.PER register defines the PWM resolution. The minimum resolution is 2 bits (TCA.PER = 0x0002), and the maximum resolution is 16 bits (TCA.PER = MAX-1).

The following equation calculates the exact resolution in bits for single-slope PWM (R_{PWM_SS}):

$$R_{PWM\_SS} = \frac{\log(PER+2)}{\log(2)}$$

The single-slope PWM frequency (f_{PWM_SS}) depends on the period setting (TCA_PER), the system's peripheral clock frequency f_{CLK_PER} and the TCA prescaler (CLKSEL in TCAn.CTRLA). It is calculated by the following equation where *N* represents the prescaler divider used:

$$f_{PWM\_SS} = \frac{f_{CLK\_PER}}{N(PER+1)}$$

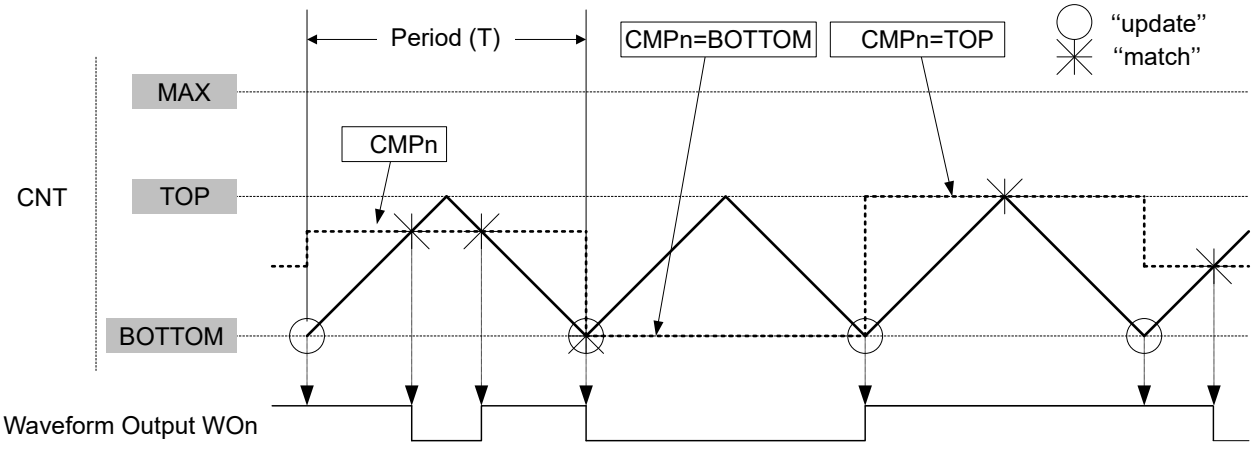
20.3.3.4.4 Dual-Slope PWM

For dual-slope PWM generation, the period (T) is controlled by TCAn.PER, while the values of TCAn.CMPm control the duty cycle of the WG output.

The figure below shows how, for dual-slope PWM, the counter counts repeatedly from BOTTOM to TOP and then from TOP to BOTTOM. The waveform generator output is set on BOTTOM, cleared on compare match when up-counting and set on compare match when down-counting.

CMPn = BOTTOM will produce a static low signal on WOn, while CMPn = TOP will produce a static high signal on WOn.

Figure 20-11. Dual-Slope Pulse-Width Modulation



Using dual-slope PWM results in half the maximum operation frequency compared to single-slope PWM operation, due to twice the number of timer increments per period.

The period register (TCAn.PER) defines the PWM resolution. The minimum resolution is 2 bits (TCAn.PER = 0x0003), and the maximum resolution is 16 bits (TCAn.PER = MAX).

The following equation calculates the exact resolution in bits for dual-slope PWM (R_{PWM_DS}):

$$R_{PWM\_DS} = \frac{\log(PER+1)}{\log(2)}$$

The PWM frequency depends on the period setting (TCAn.PER), the peripheral clock frequency (f_{CLK_PER}) and the prescaler divider used (CLKSEL in TCAn.CTRLA). It is calculated by the following equation:

$$f_{PWM\_DS} = \frac{f_{CLK\_PER}}{2N \cdot PER}$$

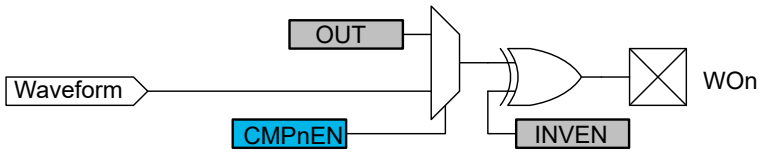
N represents the prescaler divider used.

20.3.3.4.5 Port Override for Waveform Generation

To make the waveform generation available on the port pins, the corresponding port pin direction must be set as output (PORTx.DIR[n] = 1). The TCA will override the port pin values when the compare channel is enabled (CMPnEN = 1 in TCAn.CTRLB) and a Waveform Generation mode is selected.

The figure below shows the port override for TCA. The timer/counter compare channel will override the port pin output value (OUT) on the corresponding port pin. Enabling inverted I/O on the port pin (INVEN = 1 in PORT.PINn) inverts the corresponding WG output.

Figure 20-12. Port Override for Timer/Counter Type A



20.3.3.5 Timer/Counter Commands

A set of commands can be issued by software to immediately change the state of the peripheral. These commands give direct control of the UPDATE, RESTART and RESET signals. A command is issued by writing the respective value to the Command bit field (CMD) in the Control E register (TCAn.CTRLESET).

An UPDATE command has the same effect as when an UPDATE condition occurs, except that the UPDATE command is not affected by the state of the Lock Update bit (LUPD) in the Control E register (TCAn.CTRLE).

The software can force a restart of the current waveform period by issuing a RESTART command. In this case, the counter, direction, and all compare outputs are set to '0'.

A RESET command will set all timer/counter registers to their initial values. A RESET command can be issued only when the timer/counter is not running (ENABLE = 0 in TCAn.CTRLA).

20.3.3.6 Split Mode - Two 8-Bit Timer/Counters

Split Mode Overview

To double the number of timers and PWM channels in the TCA, a Split mode is provided. In this Split mode, the 16-bit timer/counter acts as two separate 8-bit timers, which each have three compare channels for PWM generation. The Split mode will only work with single-slope down-count. Event controlled operation is not supported in Split mode.

Activating Split mode results in changes to the functionality of some registers and register bits. The modifications are described in a separate register map (see 20.6 Register Summary - TCAn in Split Mode).

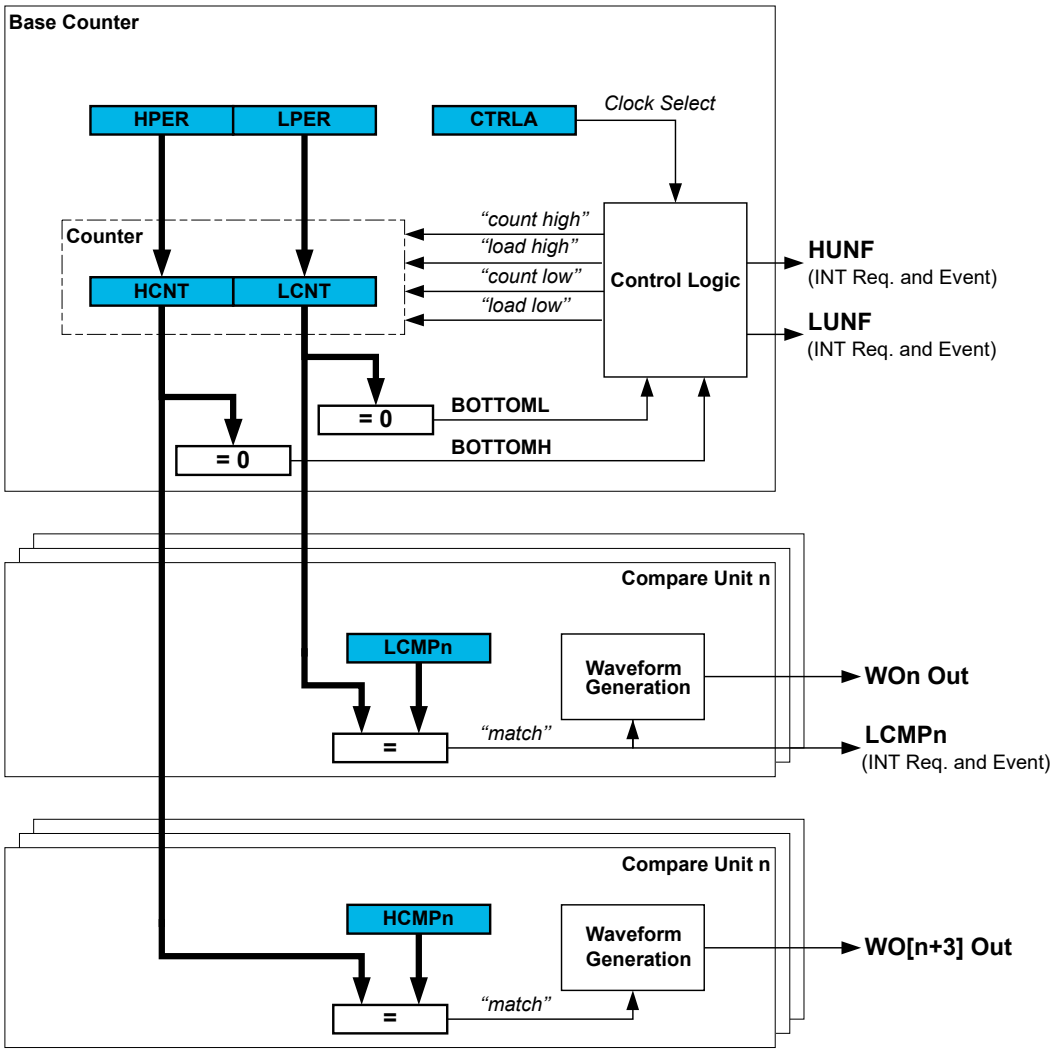
Split Mode Differences Compared to Normal Mode

- Count:
  - Down-count only
  - Low Byte Timer Counter Register (TCAn.LCNT) and High Byte Timer Counter Register (TCAn.HCNT) are independent
- Waveform Generation:
  - Single-slope PWM only (WGMODE = SINGLESLOPE in TCAn.CTRLB)
- Interrupt:
  - No change for Low Byte Timer Counter Register (TCAn.LCNT)
  - Underflow interrupt for High Byte Timer Counter Register (TCAn.HCNT)

  - No compare interrupt or flag for High Byte Compare Register n (TCAn.HCMPn)
- Event Actions: Not Compatible
- Buffer Registers and Buffer Valid Flags: Unused
- Register Access: Byte Access to All Registers

Block Diagram

Figure 20-13. Timer/Counter Block Diagram Split Mode



Split Mode Initialization

When shifting between Normal mode and Split mode, the functionality of some registers and bits changes, but their values do not. For this reason, disabling the peripheral (ENABLE = 0 in TCAn.CTRLA) and doing a hard Reset (CMD = RESET in TCAn.CTRLESET) is recommended when changing the mode to avoid unexpected behavior.

To start using the timer/counter in basic Split mode after a hard Reset, follow these steps:

1. Enable Split mode by writing a '1' to the Split mode enable bit in the Control D register (SPLITM in TCAn.CTRLD).
2. Write a TOP value to the Period registers (TCAn.PER).
3. Enable the peripheral by writing a '1' to the ENABLE bit in the Control A register (TCAn.CTRLA).
   The counter will start counting clock ticks according to the prescaler setting in the Clock Select bit field (CLKSEL) in TCAn.CTRLA.

4. The counter values can be read from the Counter bit field in the Counter registers (TCAn.CNT).

20.3.4 Events

The TCA can generate the events described in the table below. All event generators except TCAn_HUNF are shared between Normal mode and Split mode operation.

Table 20-2. Event Generators in TCA

Generator Name		Description	Event Type	Generating Clock Domain	Length of Event
Peripheral	Event				
TCAn	OVF_LUNF	Normal mode: Overflow Split mode: Low byte timer underflow	Pulse	CLK_PER	One CLK_PER period
	HUNF	Normal mode: Not available Split mode: High byte timer underflow	Pulse	CLK_PER	One CLK_PER period
	CMP0	Normal mode: Compare Channel 0 match Split mode: Low byte timer Compare Channel 0 match	Pulse	CLK_PER	One CLK_PER period
	CMP1	Normal mode: Compare Channel 1 match Split mode: Low byte timer Compare Channel 1 match	Pulse	CLK_PER	One CLK_PER period
	CMP2	Normal mode: Compare Channel 2 match Split mode: Low byte timer Compare Channel 2 match	Pulse	CLK_PER	One CLK_PER period

Note: The conditions for generating an event are identical to those that will raise the corresponding interrupt flag in the TCAn.INTFLAGS register for both Normal mode and Split mode.

The TCA has one event user for detecting and acting upon input events. The table below describes the event user and the associated functionality.

Table 20-3. Event User in TCA

User Name	Description	Input Detection	Async/Sync
TCAn	Count on positive event edge	Edge	Sync
	Count on any event edge	Edge	Sync
	Count while event signal is high	Level	Sync
	Event level controls count direction, up when low and down when high	Level	Sync

The specific actions described in the table above are selected by writing to the Event Action bits (EVACT) in the Event Control register (TCAn.EVCTRL). Input events are enabled by writing a '1' to the Enable Count on Event Input bit (CNTEI in TCAn.EVCTRL).

Event inputs are not used in Split mode.

Refer to the *Event System (EVSYS)* chapter for more details regarding event types and Event System configuration.

20.3.5 Interrupts

Table 20-4. Available Interrupt Vectors and Sources in Normal Mode

Name	Vector Description	Conditions
OVF	Overflow or underflow interrupt	The counter has reached TOP or BOTTOM.
CMP0	Compare Channel 0 interrupt	Match between the counter value and the Compare 0 register.
CMP1	Compare Channel 1 interrupt	Match between the counter value and the Compare 1 register.
CMP2	Compare Channel 2 interrupt	Match between the counter value and the Compare 2 register.

Table 20-5. Available Interrupt Vectors and Sources in Split Mode

Name	Vector Description	Conditions
LUNF	Low-byte Underflow interrupt	Low byte timer reaches BOTTOM.
HUNF	High-byte Underflow interrupt	High byte timer reaches BOTTOM.
LCMP0	Compare Channel 0 interrupt	Match between the counter value and the low byte of the Compare 0 register.
LCMP1	Compare Channel 1 interrupt	Match between the counter value and the low byte of the Compare 1 register.
LCMP2	Compare Channel 2 interrupt	Match between the counter value and the low byte of the Compare 2 register.

When an interrupt condition occurs, the corresponding interrupt flag is set in the peripheral's Interrupt Flags (*peripheral*.INTFLAGS) register.

An interrupt source is enabled or disabled by writing to the corresponding enable bit in the peripheral's Interrupt Control (*peripheral*.INTCTRL) register.

An interrupt request is generated when the corresponding interrupt source is enabled, and the interrupt flag is set. The interrupt request remains active until the interrupt flag is cleared. See the peripheral's INTFLAGS register for details on how to clear interrupt flags.

20.3.6 Sleep Mode Operation

The timer/counter will continue operation in Idle Sleep mode.

20.4 Register Summary - TCAn in Normal Mode

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0					CLKSEL[2:0]			ENABLE
0x01	CTRLB	7:0		CMP2EN	CMP1EN	CMP0EN	ALUPD	WGMODE[2:0]		
0x02	CTRLC	7:0						CMP2OV	CMP1OV	CMP0OV
0x03	CTRLD	7:0								SPLITM
0x04	CTRLECLR	7:0					CMD[1:0]		LUPD	DIR
0x05	CTRLESET	7:0					CMD[1:0]		LUPD	DIR
0x06	CTRLFCLR	7:0					CMP2BV	CMP1BV	CMP0BV	PERBV
0x07	CTRLFSET	7:0					CMP2BV	CMP1BV	CMP0BV	PERBV
0x08	Reserved									
0x09	EVCTRL	7:0					EVACT[2:0]			CNTEI
0x0A	INTCTRL	7:0		CMP2	CMP1	CMP0				OVF
0x0B	INTFLAGS	7:0		CMP2	CMP1	CMP0				OVF
0x0C ... 0x0D	Reserved									
0x0E	DBGCTRL	7:0								DBGRUN
0x0F	TEMP	7:0	TEMP[7:0]							
0x10 ... 0x1F	Reserved									
0x20	CNT	7:0	CNT[7:0]							
		15:8	CNT[15:8]							
0x22 ... 0x25	Reserved									
0x26	PER	7:0	PER[7:0]							
		15:8	PER[15:8]							
0x28	CMP0	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x2A	CMP1	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x2C	CMP2	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x2E ... 0x35	Reserved									
0x36	PERBUF	7:0	PERBUF[7:0]							
		15:8	PERBUF[15:8]							
0x37	PERBUFH	7:0	PERBUF[15:8]							
0x38	CMP0nBUF	7:0	CMPBUF[7:0]							
		15:8	CMPBUF[15:8]							
0x3A	CMP1nBUF	7:0	CMPBUF[7:0]							
		15:8	CMPBUF[15:8]							
0x3C	CMP2nBUF	7:0	CMPBUF[7:0]							
		15:8	CMPBUF[15:8]							

20.5 Register Description - Normal Mode

20.5.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					CLKSEL[2:0]			ENABLE
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:1 – CLKSEL[2:0] Clock Select
These bits select the clock frequency for the timer/counter.

Value	Name	Description
0x0	DIV1	$f_{TCA} = f_{CLK\_PER}$
0x1	DIV2	$f_{TCA} = f_{CLK\_PER}/2$
0x2	DIV4	$f_{TCA} = f_{CLK\_PER}/4$
0x3	DIV8	$f_{TCA} = f_{CLK\_PER}/8$
0x4	DIV16	$f_{TCA} = f_{CLK\_PER}/16$
0x5	DIV64	$f_{TCA} = f_{CLK\_PER}/64$
0x6	DIV256	$f_{TCA} = f_{CLK\_PER}/256$
0x7	DIV1024	$f_{TCA} = f_{CLK\_PER}/1024$

Bit 0 – ENABLE Enable

Value	Description
0	The peripheral is disabled
1	The peripheral is enabled

20.5.2 Control B - Normal Mode

Name: CTRLB
Offset: 0x01
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
		CMP2EN	CMP1EN	CMP0EN	ALUPD	WGMODE[2:0]		
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 4, 5, 6 – CMPEN Compare n Enable
In the FRQ and PWM Waveform Generation modes the Compare n Enable bits (CMPnEN) will make the waveform output available on the pin corresponding to WOn, overriding the value in the corresponding PORT output register. The corresponding pin direction must be configured as an output in the PORT peripheral.

Value	Description
0	Waveform output WOn will not be available on the corresponding pin
1	Waveform output WOn will override the output value of the corresponding pin

Bit 3 – ALUPD Auto-Lock Update
The Auto-Lock Update bit controls the Lock Update (LUPD) bit in the TCAn.CTRLE register. When ALUPD is written to '1', LUPD will be set to '1' until the Buffer Valid (CMPnBV) bits of all enabled compare channels are '1'. This condition will clear LUPD.
It will remain cleared until the next UPDATE condition, where the buffer values will be transferred to the CMPn registers and LUPD will be set to '1' again. This makes sure that the CMPnBUF register values are not transferred to the CMPn registers until all enabled compare buffers are written.

Value	Description
0	LUPD in TCA.CTRLE is not altered by the system
1	LUPD in TCA.CTRLE is set and cleared automatically

Bits 2:0 – WGMODE[2:0] Waveform Generation Mode
These bits select the Waveform Generation mode and control the counting sequence of the counter, TOP value, UPDATE condition, Interrupt condition, and the type of waveform generated.
No waveform generation is performed in the Normal mode of operation. For all other modes, the waveform generator output will only be directed to the port pins if the corresponding CMPnEN bit has been set. The port pin direction must be set as output.

Table 20-6. Timer Waveform Generation Mode

Value	Group Configuration	Mode of Operation	TOP	UPDATE	OVF
0x0	NORMAL	Normal	PER	TOP(1)	TOP(1)
0x1	FRQ	Frequency	CMP0	TOP(1)	TOP(1)
0x2	-	Reserved	-	-	-
0x3	SINGLESLOPE	Single-slope PWM	PER	BOTTOM	BOTTOM
0x4	-	Reserved	-	-	-
0x5	DSTOP	Dual-slope PWM	PER	BOTTOM	TOP
0x6	DSBOTH	Dual-slope PWM	PER	BOTTOM	TOP and BOTTOM
0x7	DSBOTTOM	Dual-slope PWM	PER	BOTTOM	BOTTOM

Note:
1. When counting up.

20.5.3 Control C - Normal Mode

Name: CTRLC
Offset: 0x02
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
						CMP2OV	CMP1OV	CMP0OV
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – CMP2OV Compare Output Value 2
See CMP0OV.

Bit 1 – CMP1OV Compare Output Value 1
See CMP0OV.

Bit 0 – CMP0OV Compare Output Value 0
The CMPnOV bits allow direct access to the waveform generator's output compare value when the timer/counter is not enabled. This is used to set or clear the WG output value when the timer/counter is not running.

20.5.4 Control D

Name: CTRLD
Offset: 0x03
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
								SPLITM
Access								R/W
Reset								0

Bit 0 – SPLITM Enable Split Mode
This bit sets the timer/counter in Split mode operation. It will then work as two 8-bit timer/counters. The register map will change compared to normal 16-bit mode.

20.5.5 Control Register E Clear - Normal Mode

Name: CTRLECLR
Offset: 0x04
Reset: 0x00
Property: -

This register can be used instead of a Read-Modify-Write (RMW) to clear individual bits by writing a '1' to its bit location.

Bit	7	6	5	4	3	2	1	0
					CMD[1:0]		LUPD	DIR
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:2 – CMD[1:0] Command
These bits are used for software control of update, restart and Reset of the timer/counter. The command bits are always read as '0'.

Value	Name	Description
0x0	NONE	No command
0x1	UPDATE	Force update
0x2	RESTART	Force restart
0x3	RESET	Force hard Reset (ignored if the timer/counter is enabled)

Bit 1 – LUPD Lock Update
Lock update can be used to ensure that all buffers are valid before an update is performed.

Value	Description
0	The buffered registers are updated as soon as an UPDATE condition has occurred
1	No update of the buffered registers is performed, even though an UPDATE condition has occurred

Bit 0 – DIR Counter Direction
Normally this bit is controlled in hardware by the Waveform Generation mode or by event actions, but it can also be changed from software.

Value	Description
0	The counter is counting up (incrementing)
1	The counter is counting down (decrementing)

20.5.6 Control Register E Set - Normal Mode

Name: CTRLESET
Offset: 0x05
Reset: 0x00
Property: -

This register can be used instead of a Read-Modify-Write (RMW) to set individual bits by writing a '1' to its bit location.

Bit	7	6	5	4	3	2	1	0
					CMD[1:0]		LUPD	DIR
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:2 – CMD[1:0] Command
These bits are used for software control of update, restart and Reset the timer/counter. The command bits are always read as '0'.

Value	Name	Description
0x0	NONE	No command
0x1	UPDATE	Force update
0x2	RESTART	Force restart
0x3	RESET	Force hard Reset (ignored if the timer/counter is enabled)

Bit 1 – LUPD Lock Update
Locking the update ensures that all buffers are valid before an update is performed.

Value	Description
0	The buffered registers are updated as soon as an UPDATE condition has occurred
1	No update of the buffered registers is performed, even though an UPDATE condition has occurred

Bit 0 – DIR Counter Direction
Normally this bit is controlled in hardware by the Waveform Generation mode or by event actions, but it can also be changed from software.

Value	Description
0	The counter is counting up (incrementing)
1	The counter is counting down (decrementing)

20.5.7 Control Register F Clear

Name: CTRLFCLR
Offset: 0x06
Reset: 0x00
Property: -

This register can be used instead of a Read-Modify-Write (RMW) to clear individual bits by writing a '1' to its bit location.

Bit	7	6	5	4	3	2	1	0
					CMP2BV	CMP1BV	CMP0BV	PERBV
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – CMP2BV Compare 2 Buffer Valid
See CMP0BV.

Bit 2 – CMP1BV Compare 1 Buffer Valid
See CMP0BV.

Bit 1 – CMP0BV Compare 0 Buffer Valid
The CMPnBV bits are set when a new value is written to the corresponding TCAn.CMPnBUF register. These bits are automatically cleared on an UPDATE condition.

Bit 0 – PERBV Period Buffer Valid
This bit is set when a new value is written to the TCAn.PERBUF register. This bit is automatically cleared on an UPDATE condition.

20.5.8 Control Register F Set

Name: CTRLFSET
Offset: 0x07
Reset: 0x00
Property: -

This register can be used instead of a Read-Modify-Write (RMW) to set individual bits by writing a '1' to its bit location.

Bit	7	6	5	4	3	2	1	0
					CMP2BV	CMP1BV	CMP0BV	PERBV
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – CMP2BV Compare 2 Buffer Valid
See CMP0BV.

Bit 2 – CMP1BV Compare 1 Buffer Valid
See CMP0BV.

Bit 1 – CMP0BV Compare 0 Buffer Valid
The CMPnBV bits are set when a new value is written to the corresponding TCAn.CMPnBUF register. These bits are automatically cleared on an UPDATE condition.

Bit 0 – PERBV Period Buffer Valid
This bit is set when a new value is written to the TCAn.PERBUF register. This bit is automatically cleared on an UPDATE condition.

20.5.9 Event Control

Name: EVCTRL
Offset: 0x09
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					EVACT[2:0]			CNTEI
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:1 – EVACT[2:0] Event Action
These bits define what action the counter will take upon certain event conditions.

Value	Name	Description
0x0	EVACT_POSEDGE	Count on positive event edge
0x1	EVACT_ANYEDGE	Count on any event edge
0x2	EVACT_HIGHLVL	Count prescaled clock cycles while the event signal is high
0x3	EVACT_UPDOWN	Count prescaled clock cycles. The event signal controls the count direction, up when low and down when high.
Other		Reserved

Bit 0 – CNTEI Enable Count on Event Input

Value	Description
0	Count on Event input is disabled
1	Count on Event input is enabled according to EVACT bit field

20.5.10 Interrupt Control Register - Normal Mode

Name: INTCTRL
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
		CMP2	CMP1	CMP0				OVF
Access		R/W	R/W	R/W				R/W
Reset		0	0	0				0

Bit 6 – CMP2 Compare Channel 2 Interrupt Enable
See CMP0.

Bit 5 – CMP1 Compare Channel 1 Interrupt Enable
See CMP0.

Bit 4 – CMP0 Compare Channel 0 Interrupt Enable
Writing the CMPn bit to '1' enables the interrupt from Compare Channel n.

Bit 0 – OVF Timer Overflow/Underflow Interrupt Enable
Writing the OVF bit to '1' enables the overflow/underflow interrupt.

20.5.11 Interrupt Flag Register - Normal Mode

Name: INTFLAGS
Offset: 0x0B
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
		CMP2	CMP1	CMP0				OVF
Access		R/W	R/W	R/W				R/W
Reset		0	0	0				0

Bit 6 – CMP2 Compare Channel 2 Interrupt Flag
See the CMP0 flag description.

Bit 5 – CMP1 Compare Channel 1 Interrupt Flag
See the CMP0 flag description.

Bit 4 – CMP0 Compare Channel 0 Interrupt Flag
The Compare Interrupt flag (CMPn) is set on a compare match on the corresponding compare channel.
For all modes of operation, the CMPn flag will be set when a compare match occurs between the Count register (CNT) and the corresponding Compare register (CMPn). The CMPn flag is not cleared automatically. It will be cleared only by writing a '1' to its bit location.

Bit 0 – OVF Overflow/Underflow Interrupt Flag
This flag is set either on a TOP (overflow) or BOTTOM (underflow) condition, depending on the WGMODE setting.
The OVF flag is not cleared automatically. It will be cleared only by writing a '1' to its bit location.

20.5.12 Debug Control Register

Name: DBGCTRL
Offset: 0x0E
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Run in Debug

Value	Description
0	The peripheral is halted in Break Debug mode and ignores events
1	The peripheral will continue to run in Break Debug mode when the CPU is halted

20.5.13 Temporary Bits for 16-Bit Access

Name: TEMP
Offset: 0x0F
Reset: 0x00
Property: -

The Temporary register is used by the CPU for single-cycle, 16-bit access to the 16-bit registers of this peripheral. It can be read and written by software. Refer to 16-bit access in the AVR CPU chapter. There is one common Temporary register for all the 16-bit registers of this peripheral.

Bit	7	6	5	4	3	2	1	0
	TEMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TEMP[7:0] Temporary Bits for 16-bit Access

20.5.14 Counter Register - Normal Mode

Name: CNT
Offset: 0x20
Reset: 0x00
Property: -

The TCAn.CNTL and TCAn.CNTH register pair represents the 16-bit value, TCAn.CNT. The low byte [7:0] (suffix L) is accessible at the original offset. The high byte [15:8] (suffix H) can be accessed at offset + 0x01.

CPU and UPDI write access has priority over internal updates of the register.

Bit	15	14	13	12	11	10	9	8
	CNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – CNT[15:8] Counter High Byte
These bits hold the MSB of the 16-bit Counter register.

Bits 7:0 – CNT[7:0] Counter Low Byte
These bits hold the LSB of the 16-bit Counter register.

20.5.15 Period Register - Normal Mode

Name: PER
Offset: 0x26
Reset: 0xFFFF
Property: -

TCAn.PER contains the 16-bit TOP value in the timer/counter in all modes of operation, except Frequency Waveform Generation (FRQ).

The TCAn.PERL and TCAn.PERH register pair represents the 16-bit value, TCAn.PER. The low byte [7:0] (suffix L) is accessible at the original offset. The high byte [15:8] (suffix H) can be accessed at offset + 0x01.

Bit	15	14	13	12	11	10	9	8
	PER[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	PER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 15:8 – PER[15:8] Periodic High Byte
These bits hold the MSB of the 16-bit Period register.

Bits 7:0 – PER[7:0] Periodic Low Byte
These bits hold the LSB of the 16-bit Period register.

20.5.16 Compare n Register - Normal Mode

Name: CMPn
Offset: 0x28 + n*0x02 [n=0..2]
Reset: 0x00
Property: -

This register is continuously compared to the counter value. Normally, the outputs from the comparators are used to generate waveforms.

TCAn.CMPn registers are updated with the buffer value from their corresponding TCAn.CMPnBUF register when an UPDATE condition occurs.

The TCAn.CMPnL and TCAn.CMPnH register pair represents the 16-bit value, TCAn.CMPn. The low byte [7:0] (suffix L) is accessible at the original offset. The high byte [15:8] (suffix H) can be accessed at offset + 0x01.

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – CMP[15:8] Compare High Byte
These bits hold the MSB of the 16-bit Compare register.

Bits 7:0 – CMP[7:0] Compare Low Byte
These bits hold the LSB of the 16-bit Compare register.

20.5.17 Period Buffer Register

Name: PERBUF
Offset: 0x36
Reset: 0xFFFF
Property: -

This register serves as the buffer for the Period register (TCAn.PER). Writing to this register from the CPU or UPDI will set the Period Buffer Valid bit (PERBV) in the TCAn.CTRLF register.

The TCAn.PERBUFL and TCAn.PERBUFH register pair represents the 16-bit value, TCAn.PERBUF. The low byte [7:0] (suffix L) is accessible at the original offset. The high byte [15:8] (suffix H) can be accessed at offset + 0x01.

Bit	15	14	13	12	11	10	9	8
	PERBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	PERBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 15:8 – PERBUF[15:8] Period Buffer High Byte
These bits hold the MSB of the 16-bit Period Buffer register.

Bits 7:0 – PERBUF[7:0] Period Buffer Low Byte
These bits hold the LSB of the 16-bit Period Buffer register.

20.5.18 Period Buffer Register High

Name: PERBUFH
Offset: 0x37
Reset: 0xFF
Property: -

Bit	7	6	5	4	3	2	1	0
	PERBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 7:0 – PERBUF[15:8] Period Buffer High Byte
These bits hold the MSB of the 16-bit Period Buffer register. Refer to TCAn.PERBUFL register description for details.

20.5.19 Compare n Buffer Register

Name: CMPnBUF
Offset: 0x38 + n*0x02 [n=0..2]
Reset: 0x00
Property: -

This register serves as the buffer for the associated Compare register (TCAn.CMPn). Writing to this register from the CPU or UPDI will set the Compare Buffer valid bit (CMPnBV) in the TCAn.CTRLF register.

The TCAn.CMPnBUFL and TCAn.CMPnBUFH register pair represents the 16-bit value, TCAn.CMPnBUF. The low byte [7:0] (suffix L) is accessible at the original offset. The high byte [15:8] (suffix H) can be accessed at offset + 0x01.

Bit	15	14	13	12	11	10	9	8
	CMPBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMPBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – CMPBUF[15:8] Compare High Byte
These bits hold the MSB of the 16-bit Compare Buffer register.

Bits 7:0 – CMPBUF[7:0] Compare Low Byte
These bits hold the LSB of the 16-bit Compare Buffer register.