Computer Architecture

Keivan Navi

Cal Poly Pomona University

knavi@cpp.edu

Office hours: Tu/Th 5:25 Pm to 6:55 Pm

Office: 8-49

Computer Architecture

Latch

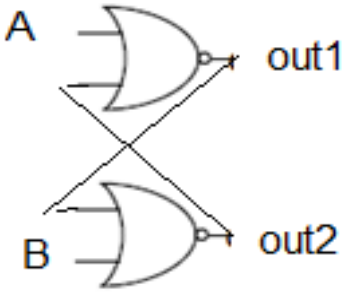
Flip Flop

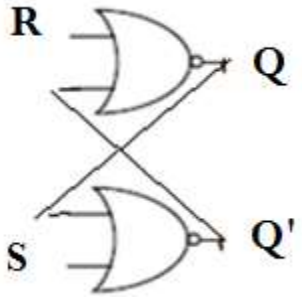
Latch

- What is a Latch:
- SR-Latches **use two inputs named S (for set) and R (for reset), and two outputs named Q and Q'** (by convention, Q is nearly always used to label the output signal from a memory device). The S input, when asserted, sets the output to a '1', and the R input resets the output to a '0'.
- A latch is a sequential circuit that **watches all the inputs continuously and changes its outputs at any time independently of a clocking signal**.

Simplest latch circuit

- The simplest bistable device, therefore, is known as a **set-reset, or S-R, latch**. To create an S-R latch, we can wire two NOR gates in such a way that the output of one feeds back to the input of another, and vice versa, like this: The Q and not-Q outputs are supposed to be in opposite states.





Simplest Latch (continued)

- The Truth table of this latch follows:

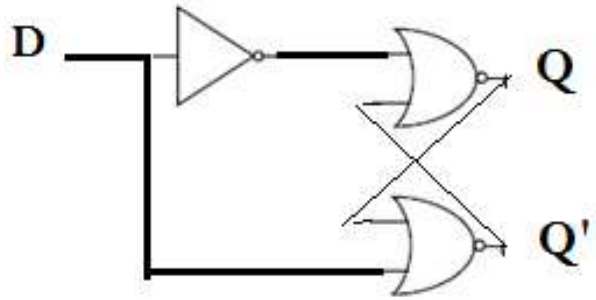
A	B	out1	out2
0	0	Memory	
0	1	1	0
1	0	0	1
1	1	0	0

R	S	Q	Q'
0	0	Memory	
0	1	1	0
1	0	0	1
1	1	0	0

- If S=R=0 the circuit will act as a memory cell and keeps its previous state.
- If S=1 and *R*=0 then Q will be 1 and Q’ will be 0
- If S=0 and R=1 then Q will be 0 and Q’ will be 1
- If S=R=1 then Q will be Q=Q’=0 (Q=Q’?!!!!)

D Latch!

- The D latch is used to capture, or 'latch' the logic level which is present on the Data line.
- The D latch Schema follows:



- If D=0 then Q=0 and Q’=1
- If D=1 then Q=1 and Q’=0
- Do you thing that this can be of use?

Flip Flops Versus Latch

- A flip flop is **an electronic circuit with two stable states that can be used to store binary data**. The stored data can be changed by applying varying inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.
- **The flip-flop alters its output only when the clock pulse is activated along with the input change.** Latch alters the output based on the changes in input constantly. As clock signals synchronize operations of the flip-flop, it operates synchronously.
- In summary when clock is Involved we are facing with Flip-Flops.

High Level Triggered Flip-Flop

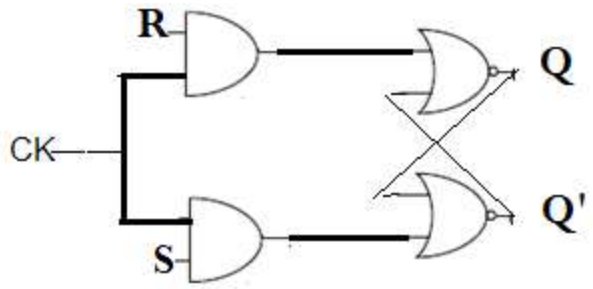
- A "high level triggered flip flop" is a type of flip flop that responds to its input data only when the clock signal is at a high logic level, meaning the output will change based on the input data only while the clock signal is actively high, not during transitions between high and low states. Unlike edge-triggered flip flops which respond to the transition of the clock signal (rising or falling edge), a high level triggered flip flop reacts to the entire duration of the high clock level. When the clock signal is high, the flip flop "latches" the current input data at its output, meaning the output will reflect the input value as long as the clock remains high.

Low Level Triggered Flip-Flop

- A "low level triggered flip flop" is a type of flip flop that changes its output state when the clock signal is at a low logic level, meaning it responds to the "low" voltage period of the clock signal, rather than a transition between high and low levels (edge triggering). The output of the flip flop will change only when the clock signal is actively low (at a logic 0 level). In circuit diagrams, a small circle is often placed near the clock input to indicate a negative level trigger. Low level triggered and high level triggered flip flops are generally less commonly used compared to edge triggered flip flops because they can be more susceptible to timing issues due to the potential for metastable states if the clock signal spends a long time at the low level.

High Level Triggered SR Flip Flop

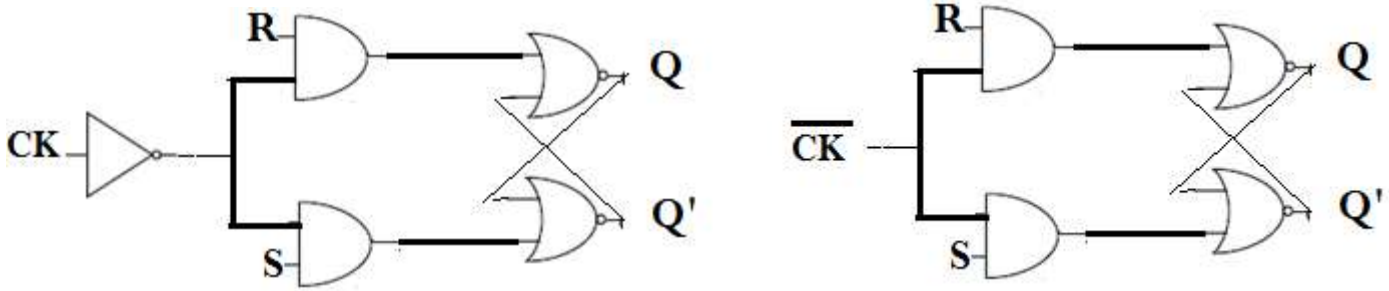
- High level SR Flip Flop schema follows:



- If clock = 0 then This Flip Flop acts as memory cell and nothing can be changed.
- If clock =1 then S and R can change Q and Q’ outputs.

Low Level Triggered SR Flip Flop

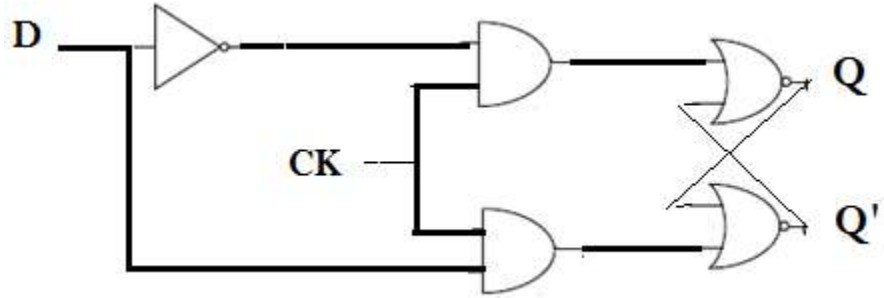
- Two Different Low level SR Flip Flop schema follows:



- If clock = 1 then This Flip Flop acts as memory cell and nothing can be changed.
- If clock =0 then S and R can change Q and Q’ outputs.

High Level Triggered D Flip Flop

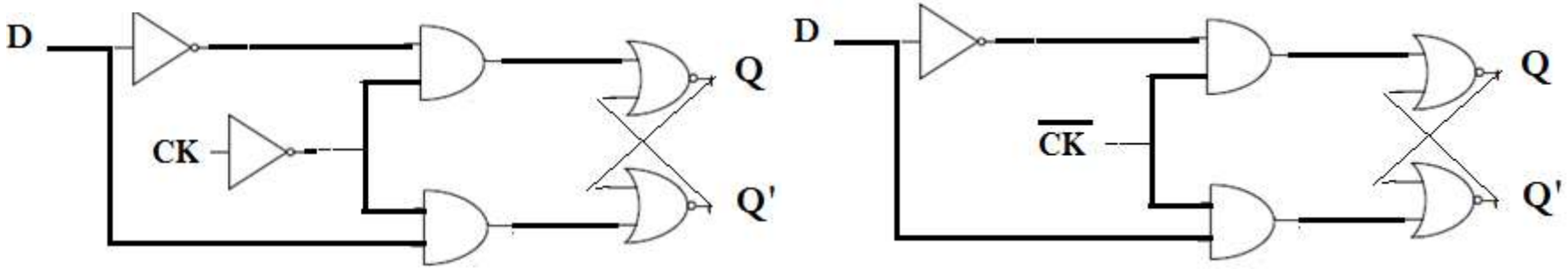
- High level D Flip Flop schema follows:



- If clock = 0 then This Flip Flop acts as memory cell and nothing can be changed.
- If clock =1 then D input can change Q and Q’ outputs.

Low Level Triggered D Flip Flop

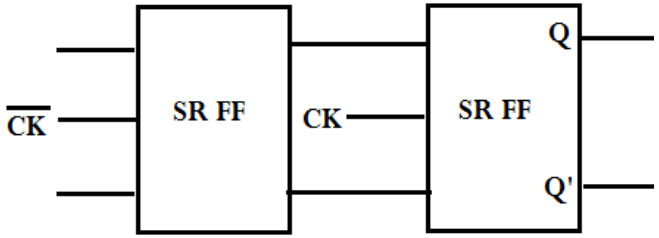
- Two Different Low level D Flip Flop schema follows:



- If clock = 1 then This Flip Flop acts as memory cell and nothing can be changed.
- If clock =0 then D input can change Q and Q’ outputs.

Rising Edge Triggered SR Flip Flop

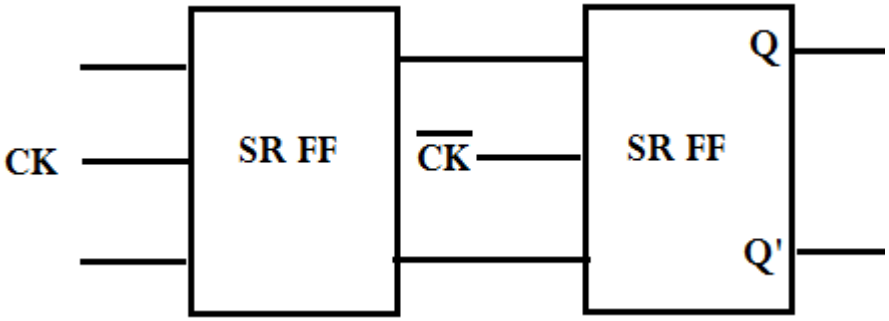
- It is said to trigger on the edge of the clock pulse, and thus is called an edge-triggered flip-flop. The flip-flop can be triggered by a rising edge (0->1, or positive edge trigger) or falling edge (1->0, or negative edge trigger). The rising edge triggered SR flip flop is activated at the positive going edge of the clock pulse.
- Rising Edge SR Flip Flop schema follows:



- If clock goes from 0 to 1 (0->1)then S and R can change Q and Q' outputs.

Falling Edge Triggered SR Flip Flop

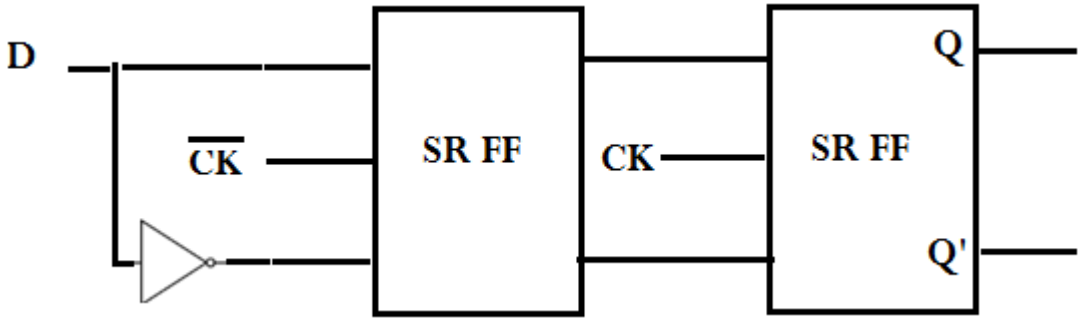
- It is said to trigger on the edge of the clock pulse, and thus is called an edge-triggered flip-flop. The flip-flop can be triggered by a rising edge (0->1, or positive edge trigger) or falling edge (1->0, or negative edge trigger). The falling edge triggered SR flip flop is activated at the negative going edge of the clock pulse. The SR inputs at the clock transition controls the output of SR flip flop.
- Rising Edge SR Flip Flop schema follows:



- If clock goes from 0 to 1 (0->1)then S and R can change Q and Q' outputs.

Rising Edge Triggered D Flip Flop

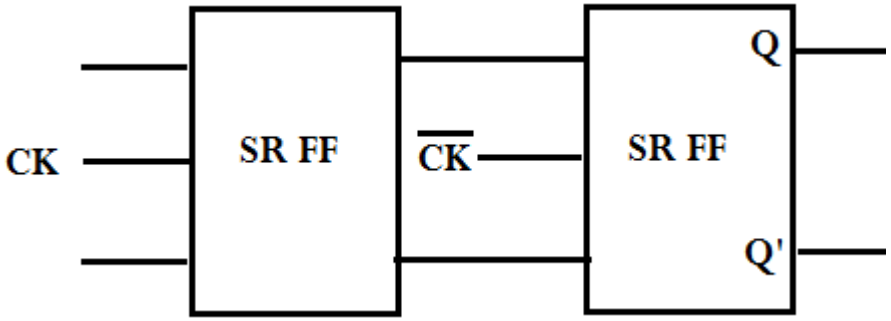
- It is said to trigger on the edge of the clock pulse, and thus is called an edge-triggered flip-flop. The flip-flop can be triggered by a rising edge (0->1, or positive edge trigger) or falling edge (1->0, or negative edge trigger). The rising edge triggered D flip flop is activated at the positive going edge of the clock pulse.
- Rising Edge D Flip Flop schema follows:



- If clock goes from 0 to 1 (0->1)then D can change Q and Q’ outputs.

Falling Edge Triggered D Flip Flop

- It is said to trigger on the edge of the clock pulse, and thus is called an edge-triggered flip-flop. The flip-flop can be triggered by a rising edge (0->1, or positive edge trigger) or falling edge (1->0, or negative edge trigger). The falling edge triggered D flip flop is activated at the negative going edge of the clock pulse. Rising Edge D Flip Flop schema follows:



- If clock goes from 1 to 0 (1->0)then D input can change Q and Q’ outputs.

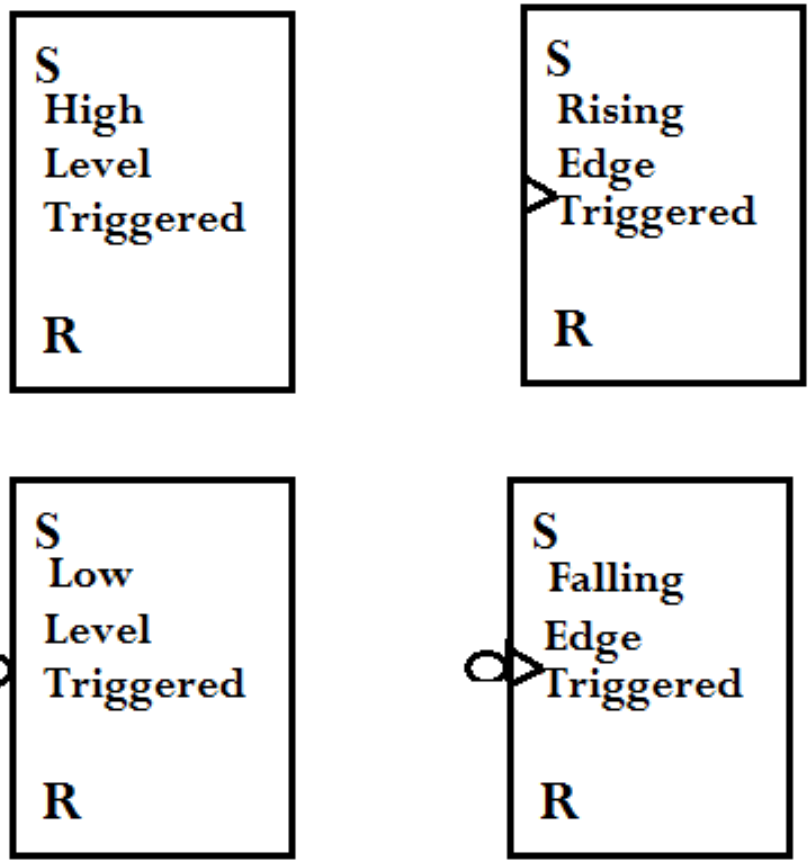
JK Flip-Flop

- K flip flop operates on sequential logic principle, where the output is dependent not only on the current inputs but also on the previous state. There are two inputs in JK Flip Flop Set and Reset denoted by J and K. It also has two outputs Output and complement of Output denoted by Q and $\bar{Q}$. Its function is very similar to SR Flip Flop. The only difference is that when J=K=1 Q output will toggle.
- Do you think that High Level triggered JK Flip Flop makes sense? Why? Consider J=K=1, then as long as the clock is high the output will toggle!!
- Do you think that Low Level triggered JK Flip Flop makes sense? Why? Consider J=K=1, then as long as the clock is low the output will toggle!!

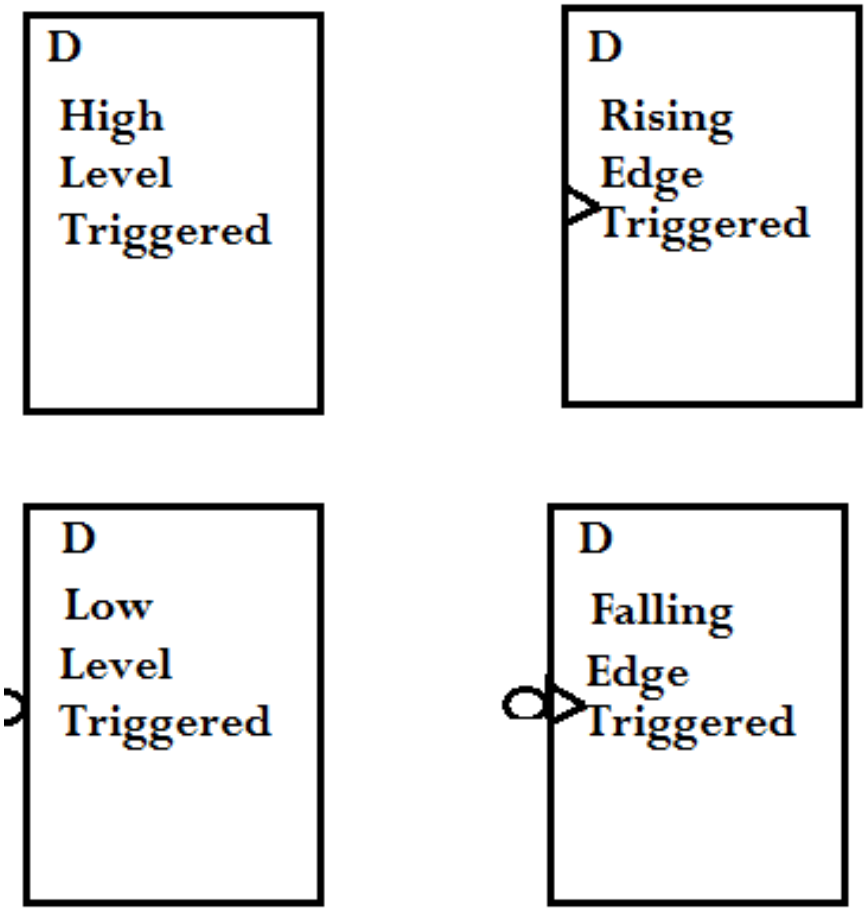
T Flip-Flop

- If T=1 the output will toggle.
- If T=0 the T Flip Flop acts as memory cell.
- Do you think that High Level triggered T Flip Flop makes sense? Why? Consider T=1, then as long as the clock is high the output will toggle!!
- Do you think that Low Level triggered T Flip Flop makes sense? Why? Consider T=1, then as long as the clock is low the output will toggle!!

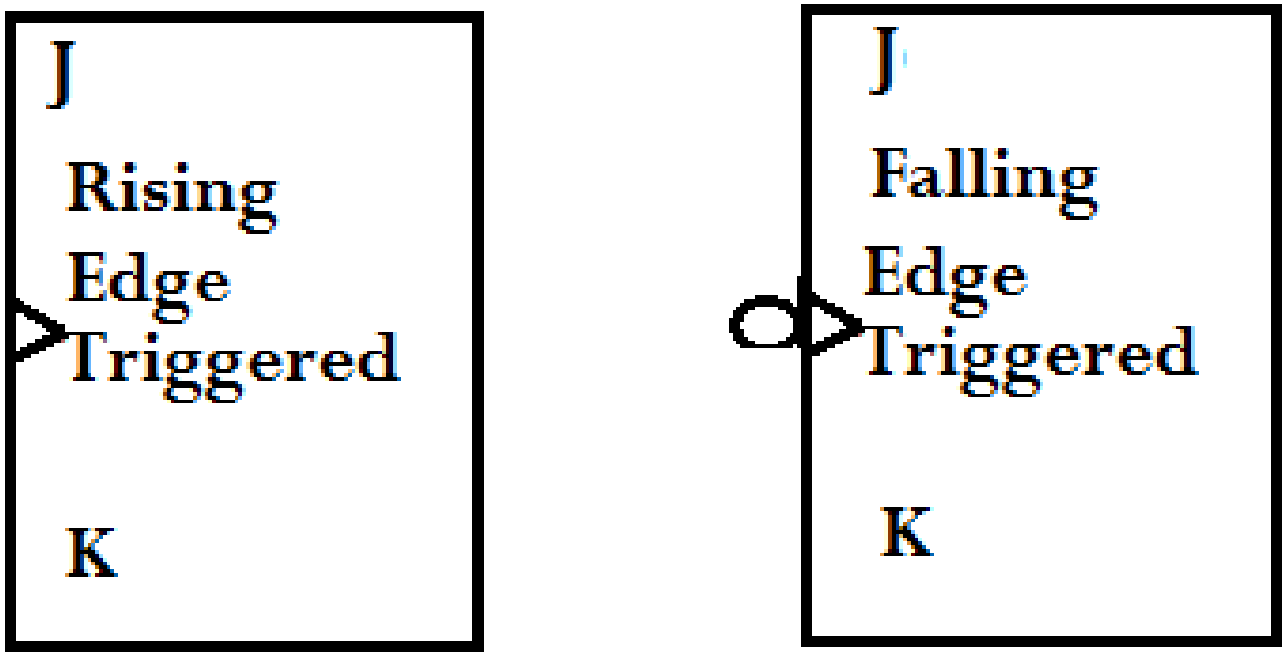
Different Kind of SR Flip-Flop



Different Kind of D Flip-Flop



Different Kind of JK Flip-Flop



Different Kind of T Flip-Flop