Computer Architecture

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Synchronous

Counter

Synchronous counter

- A Synchronous counter is the counter in which the clock input with all the flip-flops uses the same source and produces the output at the same time.
- Asynchronous Counter: Also known as a ripple counter, where flip-flops are triggered by the output of the preceding flip-flop. Each flip-flop changes state sequentially. Synchronous Counter: All flip-flops are triggered simultaneously by a common clock signal, ensuring that all state changes occur at the same time.

Synchronous counter (continued)

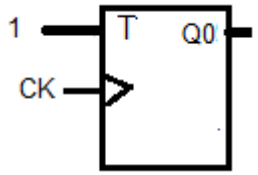
- Synchronous counters eliminate the cumulative flip-flop delay seen in ripple counter. Each flip-flop is clocked by the same clock signal. Each gate selectively controls when each more significant bit flip-flop is to change state (toggle) on the next clock transition. Some times we use “state Diagram” to design a sequential circuit. A state diagram is used in computer science and related fields to describe the behavior of systems.
- The main disadvantage of a synchronous counter is, it needs a lot of additional logic to execute. They need large components & circuitry. This counter uses a complex logic circuit & the increasing number of states.

Asynchronous or Synchronous

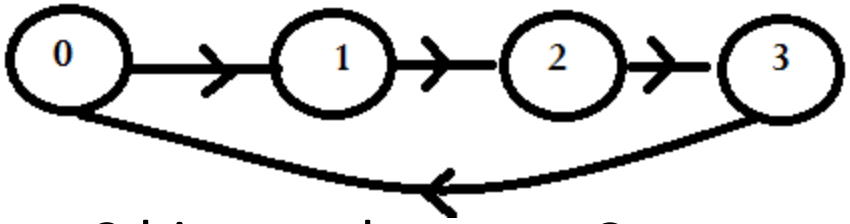
- Synchronous circuits are digital circuits that are synchronized by clock signals. Asynchronous circuits are digital circuits that do not rely on clock signals.
- So many wonderful asynchronous circuits can be designed. We can design and even publish a good scientific paper but sometimes when it is supposed to be mass produced, it may be hard to sell them. The noise is a serious issue.
- That's why even some researchers love asynchronous designing, they prefer synchronous approach.

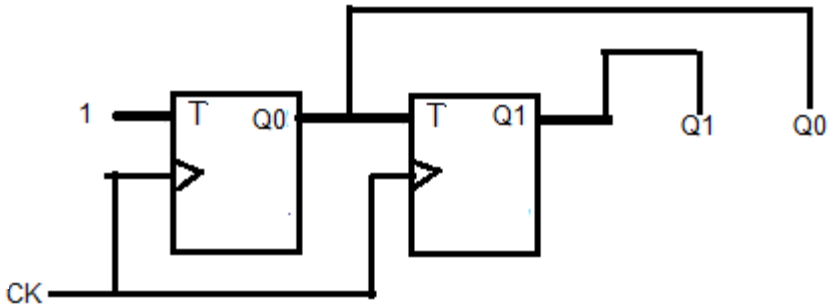
Synchronous Counters (1,2,3 bits)

- 1 bit synchronous Counter:
- State Diagram

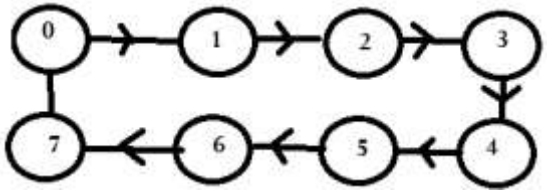


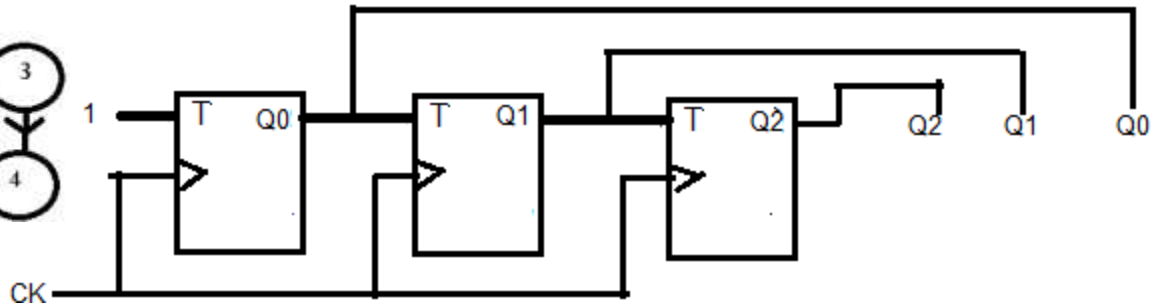
- 2 bits synchronous Counter:





- 3 bits synchronous Counter:

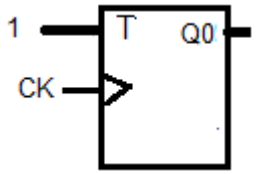




How to design with T Flip-Flop

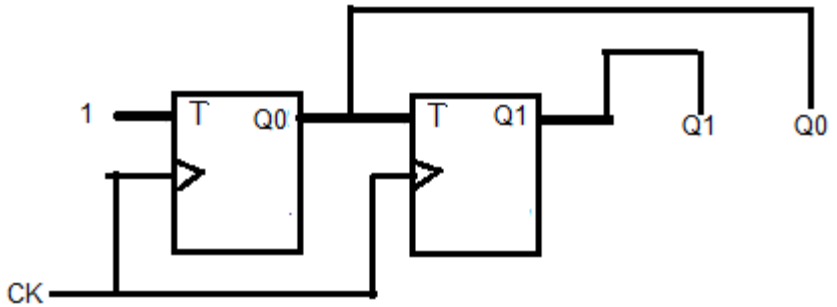
- One bit Up counter:

Q	Q+	T
0	1	1
1	0	1

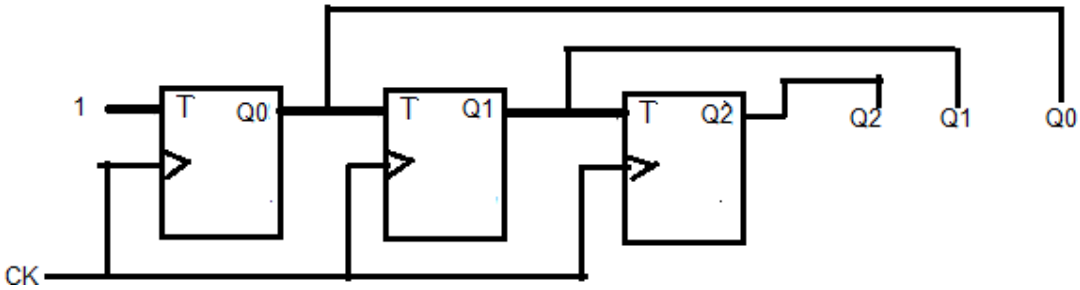


- 2 bits Up Counter:

Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1



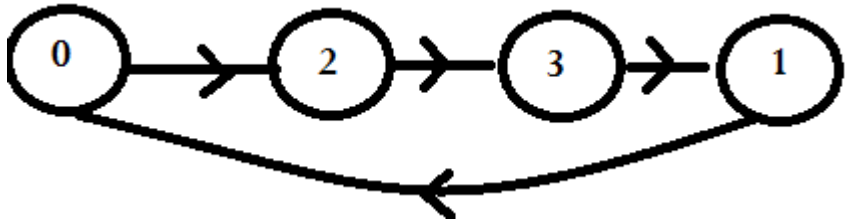
Q2	Q1	Q0	Q2+	Q1+	Q0+	T2	T1	T0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1



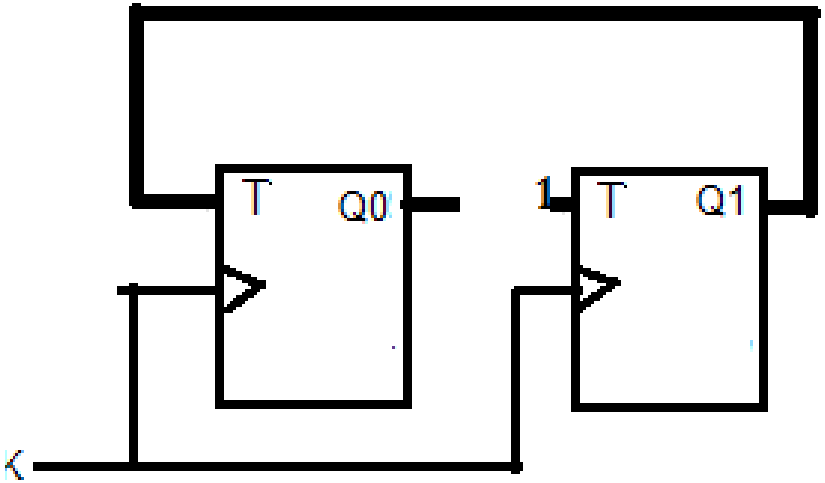
0=>2=>3=>1=>0

00=>10=>11=>01=>00

- Is it OK?
- State Diagram:



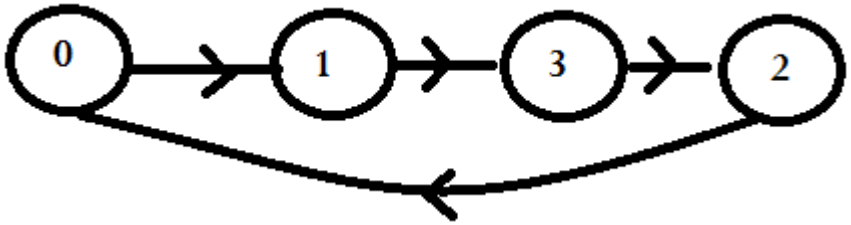
Q1	Q0	Q1+	Q0+	T1	T0
0	0	1	0	1	0
0	1	1	1	1	0
1	0	0	1	1	1
1	1	0	0	1	1



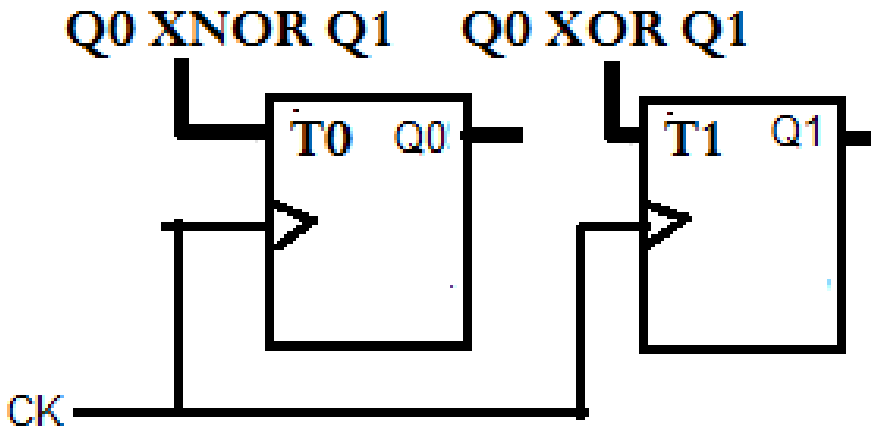
0=>1=>3=>2=>0

00=>01=>11=>10=>00

- Is it OK?
- State Diagram:



Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	1	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	1	1	0	0	1



3=>2=>1=>0=>3

11=>10=>01=>00=>11

- Does it work? It seems that something is going wrong. But that is not true. Why?
- What is the state Diagram?

Q1	Q0	Q1+	Q0+	T1	T0
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	1	1