Computer Architecture

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Office hours: Tu/Th 5:25 Pm to 6:55 Pm

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Outline

- Build combinational circuits with basic logic elements
- Use Decoder, Encoder, and Multiplexer for implementation of logic circuits.
- Explain the structure and function of various adders, registers and counters
- Recognize the characteristics of Flip-Flops;
- Design sequential circuits using state tables (diagrams) and transition tables;
- Describe instruction set architecture and machine organization of a RISC processor (MIPS);
- Structure and design arithmetic and logical units for basic integer and floating operations;
- Design simple processor architecture, in particular, data paths for a set of basic instructions;
- Design the control units for a simple processor architecture;
- Explain the principle of pipelining techniques;
- Summarize cache and memory organization;
- Define cache and storage performance;
- Describe alternative computer architectures (multicores, multiprocessors, and clusters).

Detailed Syllabus (Tentative)

Week# 1	Introduction Basic logic circuits, Buffer, Not, And, Nand, Or, Nor , Xor, Xnor, Majority, Minority, Decoder, Encoder, Mux
Week#2	Half Adder, Full Adder, Addition, Subtraction
Week# 3	Logical Unit, Arithmetic Unit, HA+-, FA+-, Approximation Arithmetic
Week# 4	Multiplication, Division, Compressors, Multi-operand Addition
Week# 5	Problem solving First Exam

Week# 6	Latches, Flip Flops, Level triggered versus edge triggered Flip Flops
Week# 7	Karnaugh Map (K-map), From FF to FF, Sequential circuits using state tables (diagrams) and transition tables
Week# 8	Counters (Asynchronous, Synchronous) Registers, Shift and Rotate
Week # 9	Structure and design of the arithmetic and logical units
Week # 10	Problem solving Second Exam

Week # 11	Interrupt versus Poling, CD (Error detecting and correcting codes), DVD, Flash memory, I/O and Peripheral devices (Printer. Plotter, Monitors, LED LCD)
Week # 12	Memory, Cache. Multilevel Cache system Dynamic, Static, Memory Hierarchy, Access time
Week # 13	Pipeline, Super pipelining, Super Scaling, Super Pipelined Super Scalar
Week # 14	Designing a simple CPU, Designing more advanced CPU Instruction set architecture and machine organization of a RISC processor
Week #15	Problem Solving Overall conclusion

Grading Policy

- First Exam 25%
- Second Exam 25%
- Final Exam 30%
- Home Work 15%
- Final Projects 5%
- In-class exercises+ Contribution Positive Effect
- Pop up Quizzes 1Extra Credit Maximum 5
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Suggested Text & Reference

- Patterson and Hennessy, Computer Organization and Design, 5th edition, 2014. Morgan Kaufmann.
- State-of-the-art papers