Question **1**

Not answered

Points out of 5.00

Remove flag

Active-high decoders are maxterm generators.

Select one:

- True
- False

The correct answer is 'False'.

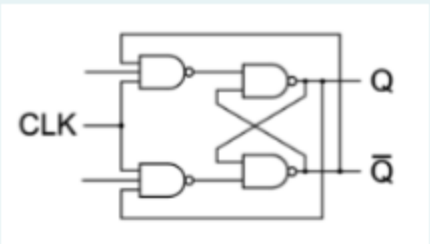
Question **2**

Complete

10.00 points out of 10.00

Flag question

Which memory component does the following circuit describe?



- a. D-Flip Flop
- b. J-K Flip Flop
- c. S-R Latch
- d. D-Latch
- e. T-Flip Flop

The correct answer is:
J-K Flip Flop

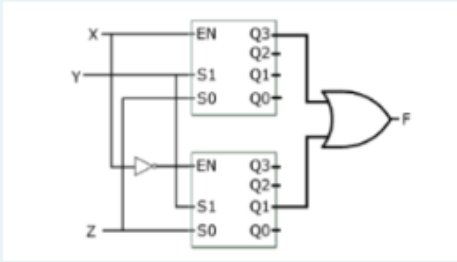
Question **3**

Complete

0.00 points out of 10.00

Flag question

Which Boolean expression describes the behavior of the following circuit?



a. F = X'.Y'.Z' + X.Y.Z'

b. F = 1

c. F = X'.Y'.Z + X.Y.Z

d. F = 0

e. F = X'.Y.Z' + X.Y.Z

The correct answer is:
F = X'.Y'.Z + X.Y.Z

Question **4**

Not answered

Points out of 10.00

Remove flag

For an S-R latch that is built by identical NOR gates, what is the expected behavior of the latch if we take the following actions: we set both input pins simultaneously, wait for a while and reset them simultaneously?

a. The latch continuously outputs 0.

b. The latch continuously outputs 1.

c. None of these.

d. The latch first outputs 1 then 0 and the output value remains 0.

e. The latch first outputs 0 then 1 and the output value remains as 1.

The correct answer is:
None of these.

Question **5**

Not answered

Points out of 5.00

Remove flag

The outputs of Mealy-type sequential circuits (Mealy Finite State Machines) are solely dependent on the state (memory) information of the circuits.

Select one:

- True
- False

The correct answer is 'False'.

Question **6**

Complete

5.00 points out of 5.00

Remove flag

All sequential circuits cannot be built by using only NOT and OR gates.

Select one:

- True
- False

The correct answer is 'False'.

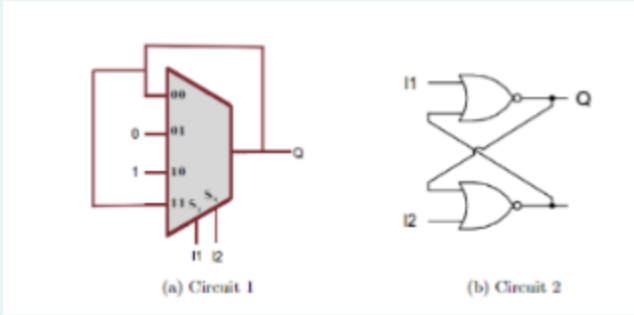
Question **7**

Not answered

Points out of 10.00

Remove flag

Which one of the following statements is wrong for the circuits below?



(a) Circuit 1 (b) Circuit 2

a. After setting I1=0, I2=1, both circuits output the value 0 (Q=0).

b. After setting I1=0, and I2=0 on both circuits, the output values do not change.

c. Both circuits could be used to build a D-flip flop by using additional AND and NOT gates.

d. It is unsafe to set I1=1, I2=1 on both circuits.

e. After setting I1=1, I2=0, both circuits output the value 1 (Q=1).

The correct answers are:
After setting I1=1, I2=0, both circuits output the value 1 (Q=1).,

After setting I1=0, I2=1, both circuits output the value 0 (Q=0).,

It is unsafe to set I1=1, I2=1 on both circuits.

Question **8**

Not answered

Points out of 5.00

Remove flag

D-type flip-flops are more suitable for automated design.

Select one:

- True
- False

The correct answer is 'True'.

Question **9**

Not answered

Points out of 5.00

Remove flag

Propagation delay of logic gates does not affect the maximum frequency value of a clock signal that is applied to a sequential circuit.

Select one:

- True
- False

The correct answer is 'False'.

Question **10**

Complete

25.00 points out of 25.00

Flag question

Below characteristic tables of several memory components are given. Please match the tables with one of the memory components: D-Latch, D-Flip Flop, S-R Latch, J-K Flip Flop, and T-Flip Flop.

Inputs	Output
IO	Q(t)
0	Q(t − 1)
1	Q'(t − 1)

T-Flip Flop

Inputs	Output
IO	Q(t)
0	0
1	1

D-Flip Flop

Inputs		Output
I1	IO	Q(t)
0	0	Q(t − 1)
0	1	0
1	0	1
1	1	-

S-R Latch

Inputs		Output
I1	IO	Q(t)
0	0	Q(t − 1)
0	1	0
1	0	1
1	1	Q'(t − 1)

J-K Flip Flop

Inputs		Output
I1	IO	Q(t)
0	0	Q(t − 1)
0	1	0
1	0	Q(t − 1)
1	1	1

D-Latch

The correct answer is:

Inputs	Output
IO	Q(t)
0	Q(t − 1)
1	Q'(t − 1)

→ T-Flip Flop,

Inputs	Output
IO	Q(t)
0	0
1	1

→ D-Flip Flop,

Inputs		Output
II	IO	Q(t)
0	0	Q(t − 1)
0	1	0
1	0	1
1	1	-

→ S-R Latch,

Inputs		Output
II	IO	Q(t)
0	0	Q(t − 1)
0	1	0
1	0	1
1	1	Q'(t − 1)

→ J-K Flip Flop,

Inputs		Output
II	IO	Q(t)
0	0	Q(t − 1)
0	1	0
1	0	Q(t − 1)
1	1	1

→ D-Latch

Question **11**

Complete

5.00 points out of 5.00

Flag question

One important advantage of using JK-type flip-flops when sequential circuits are designed manually is that the combinational circuitry that determines the values of their inputs is likely to be simpler.

Select one:

- True
- False

The correct answer is 'True'.

Question **12**

Complete

5.00 points out of 5.00

Flag question

Designing sequential circuits with D-type flip flops is complicated by the fact that the input equations for the flip flops must be derived indirectly from the state table.

Select one:

- True
- False

The correct answer is 'False'.