Little Free Radio Datasheet

Rev. 47c3919

1.0 Contents

2.0 Overview

Little Free Radio (LFR) is open source, command, telemetry, and data radio, geared at CubeSats, high altitude balloons, and other applications requiring a small, power efficient, medium-speed communications link. The design is built around inexpensive commercially available components.

The low power integrated processor, the Texas Instruments MSP430FR5994, manages interfacing with the RFIC and provides a convenient interface for the flight computer. This includes an internal packet buffer, storage and configuration of RF parameters, and control of supporting RF switching and amplifier circuitry.

The RFIC, the Silicon Labs Si4464, is a high performance, low power, transceiver IC covering a wide range of VHF and UHF frequencies.

A TCXO provides an accurate and stable frequency reference across the LFR's entire operating range.

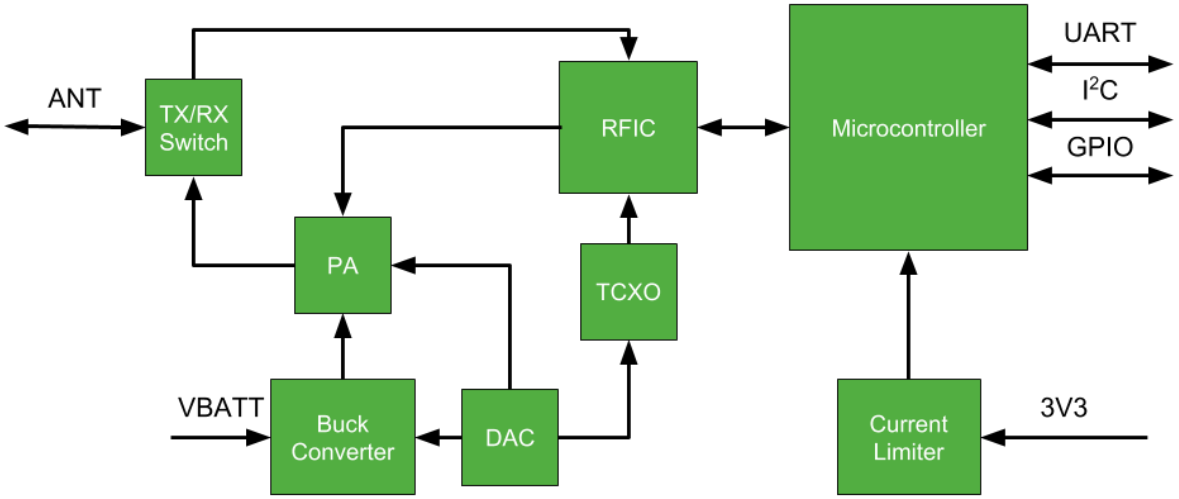
The power amplifier is a high-efficiency Class-E design based on the AFT05MS004NT1 MOSFET. Good efficiency is maintained across a wide range of output power by adjusting the drain voltage .

2.1 Features

- 2FSK / 2GFSK / 4FSK* / 4GFSK* / CW* narrow band transceiver
- Data rates up to 1 Mbps (10 kpbs typical)
- Wide frequency range: 119 MHz - 960 MHz**
- High transmit power: $>$ 3W**
- High efficiency PA: $>$ 65% from under 1W to over 3W**
- Open source hardware, firmware, and example SDR ground station
- RF Protocol Support:
  - Low-overhead custom framing with CRC-16
  - CCSDS 133.0-B-1*
- 3.3V logic supply and unregulated 5 to 20V VBATT supply
- Low RX power consumption: $<$ 25 mA @ 3.3 V
- Multiple interface options:
  - UART (9600 / 38400 / 115200 baud)
  - I^2C slave*
  - SPI slave*
- RF parameters reconfigurable in orbit (within band)*
- Half duplex with single antenna
- SMA antenna connector
- Hardware TX inhibit
- Hardware AFC*
- Hardware AGC*
- Data whitening*
- Integrated single event latch-up mitigation and over-current protection
- Integrated transmit amplifier buck converter
- Industrial temperature range: -40 to +85 C
- Compact module form factor

* Exisiting hardware support, software support in progress.
** Dependent on hardware component selection

2.2 Block Diagram



3.0 Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
Vcc	Logic supply voltage	0	3.6	V
V_{batt}	PA supply voltage	0	42	V
IL	Logic supply current	-	140	mA
P_{in}	RF Input	-	+10	dBm
T_s	Storage Temperature	-40	110	C
T_{op}	Operating Temperature	-30	85	C

4.0 Electrical Characterisitics

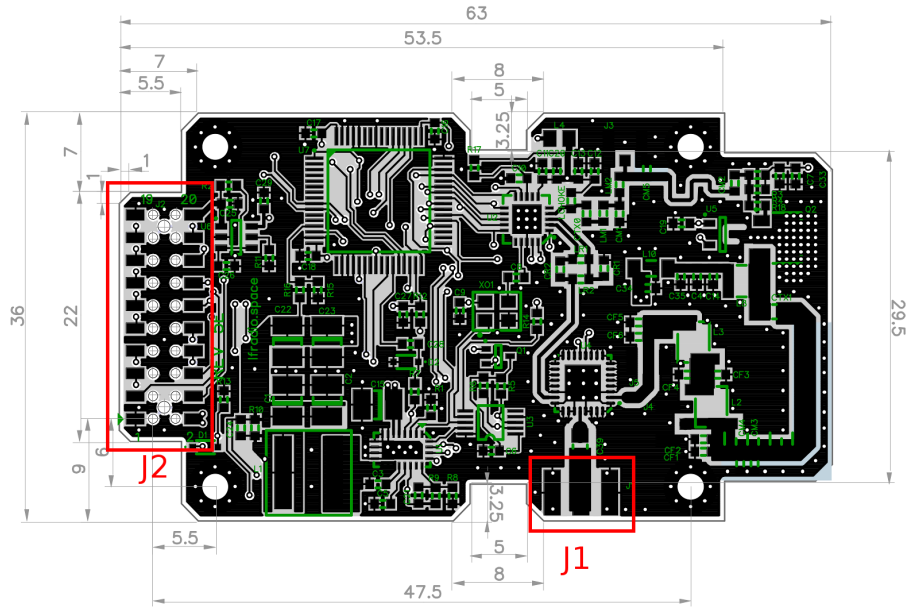
Symbol	Description	Minimum	Typical	Maximum	Unit
Vcc	Logic supply voltage	3.0	3.3	3.6	V
I_{RX}	RX Logic supply current		18		mA
I_{TX}	TX Logic supply current		100		mA
V_{batt}	PA supply voltage	5	8	18	V
I_{PA}	PA VBATT supply current		630*		mA

* $V_{batt} = V_{dd} = 7.0$ V, $P_{out} = 34.77$ dBm, F = 436.5 MHz

5.0 RF Characterisitics

Symbol	Description	Minimum	Typical	Maximum	Unit
P_{Out}	RF Power Out		+30	+35	dBm
F	Frequency	420	430	450	MHz
BR	Bit Rate	100	10000	500000	bps
ΔF	Deviation	TBD	BR/4	TBD	kHz
F_{err}	Frequency stability	2.5	2.5		ppm
P_{RX}	Sensitivity @ 10kbps w/ 5 kHz deviation		-107 (TBV)		dBm

6.0 Connectors and Pinout



6.1 J1 - ANT SMA Connector

J1 is a 50 ohm female SMA connector for the antenna. It acts as both the transmit and receive connection via an integrated RF switch. J1 is an edge mount connector mounted parallel to the board.

6.2 J2 - Main Header Connector

J2 is a female low profile 2 mm header (Sullins NPPN102GFNP-RC) that can be mated to from either the top or the bottom. Compatible mating connectors depend on how LFR is mounted; Samtec MTMM-110-07-G-D-290 works for a good range of configurations.

Pin	Description	Description	Pin
19	Ground	3V3 In	20
17	Debug UART TXD	Debug UART RXD	18
15	External SDA	External SCL	16
13	Radio GPIO2	Radio GPIO3	14

Pin	Description	Description	Pin
11	Radio GPIO0	Radio GPIO1	12
9	MSP430 SBWTCK	MSP430 SBWTDIO	10
7	MSP430 GPIO P2.3	MSP430 GPIO P2.4	8
5	TX Inhibit	TX Active	6
3	CMD UART TXD	CMD UART RXD	4
1	Ground	VBATT In	2

6.3 TPx - Test Points

The board also features test points that can be used to debug communications between the MCU and RFIC. They are aligned to a 100 mil (2.54 mm) grid and are designed to mate with pogo pins.

TP	Description
1	Si4464 Interrupt Request
2	Si4464 SPI Clock
3	Si4464 SPI MISO
4	Si4464 SPI MOSI
5	Si4464 SPI Chip Select (active low)
6	Si4464 Shutdown
7	PA/TCXO DAC I^2C SCL
8	PA V_{dd} (divided)

TP	Description
9	PA I_{mon} output
10	PA V_{dd} PGOOD output

7.0 Interfacing

LFR uses a simple, binary protocol over UART to communicate with the flight computer. Each command to the radio is prefixed with a synchronization word and ended with a checksum to ensure data integrity even in the case of bus errors. Commands to the radio are acknowledged with a reply indicating successful execution of a command or an error condition with error code indicating the source of the error. Received packets and resets result in spontaneous replies being sent over the serial connection. These do not require acknowledgement from the flight computer.

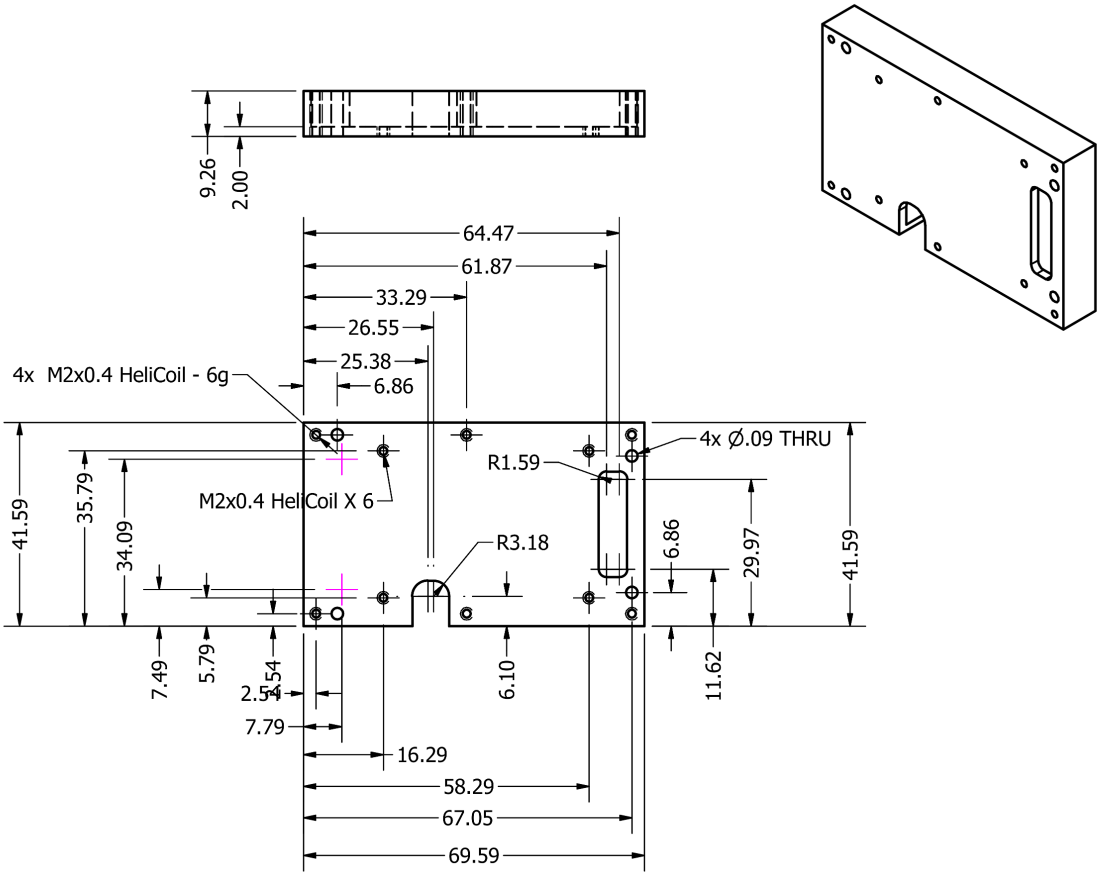
LFR is capable of buffering packets internally. Commanding LFR to transmit adds a packet to this internal buffer. When the buffer is full, attempting to add a packet to the queue results in an error reply indicating the buffer is full.

The UART connection can be run at up to 115200 baud, allowing saturation of the radio channel. LFR hardware also supports the use of I^2C as the command interface. This is pending future firmware support for I^2C.

Further details of the command protocol can be found in the LFR User's Guide.

8.0 Mechanical Drawing

Drawing is preliminary. Use with caution.


9.26
2.00
64.47
61.87
33.29
26.55
25.38
6.86
4x M2x0.4 HeliCoil - 6g
4x Ø.09 THRU
R1.59
M2x0.4 HeliCoil X 6
R3.18
41.59
35.79
34.09
6.86
29.97
41.59
7.49
5.79
2.54
2.54
7.79
6.10
11.62
16.29
58.29
67.05
69.59