Exercise 5.4

5.4.1

For a Cache line size $= \frac{2^4 \text{ bytes}}{4 \text{ bytes/word}} = 4 \text{ words}$

For b Cache line size $= \frac{2^5 \text{ bytes}}{4 \text{ byte/word}} = 8 \text{ words}$

5.4.2

For a. $2^6 = 64$ cache entries

For b. $2^7 = 128$ cache entries

5.4.3

For a.

Data storage bits $= 64 \times 16 \times 8 = 8192$ bits

Tag storage bits $= 64 \times (22+1) = 1472$ bits

ratio $= \frac{8192+1472}{8192} \approx 1.18$

For b.

Data storage bits $= 128 \times 32 \times 8 = 32768$ bits

Tag storage bits $= 128 \times (20+1) = 2688$ bits

ratio $= \frac{32768+2688}{32768} \approx 1.08$

5.4.4.

For a. 1 block replaced

(Address 1024 replaced address 0's block)

For b. 0 block replaced

5.4.5 For a

$$\text{Hit ratio} = \frac{\text{Number of hits}}{\text{Total references}}$$

Hits: Address 4, 30, 140

Hit ratio $= \frac{3}{12} = 0.25 = 25\%$

For b.

Hits: Address 4, 16, 30, 140, 180

Hit ratio $= \frac{5}{12} \simeq 0.417 \simeq 41.7\%$

5.4.6.

For a.

Index 0 : <1, 1, Block containing address 1024>

Index 1 : <1, 0, Block containing address 16>

Index 8 : <8, 0, Block containing address 132>

Index 10 : <10, 0, Block containing address 160>

Index 11 : <11, 0, Block containing address 180>

Index 14 : <14, 0, Block containing address 232>

Index 25 : <25, 3, Block containing address 3100>

Index 29 : <29, 2, Block containing address 2180>

For b:

Index 0 : <0, 0, Block containing address 0, 4, 16, 80>

Index 4 : <4, 0, Block containing address 132, 140>

Index 5 : <5, 0, Block containing address 160, 180>

Index 7 : <7, 0, Block containing address 252>

Index 32 : <32, 0, Block containing address 1024>

Index 68 : <68, 4, Block containing address 218>

Index 96 : <96, 6, Block containing address 3100>

Exercise 5.5

5.5.1

For a.

Buffers between L1 and L2: Write buffer, Read buffer

Buffers between L2 and memory: Write buffer, Read buffer

For b.

Buffers between L1 and L2: Write buffer, Read buffer

Buffers between L2 and memory: Write buffer, Read buffer

5.5.2 ① Detect write miss in L1

② Identify block to evict (if necessary)

③ Write back dirty block to L2 (if dirty)

④ Fetch block from L2 (or main memory)

⑤ Write the block to L1

⑥ Perform the write operation

⑦ Set the dirty bit.

5.5.3 ① Detect write miss in L1
② Fetch Block from L2
③ Identify block to evict (if necessary)
④ Move dirty block to L2 (if dirty and exclusive)
⑤ Replace block in L2
⑥ Write the block to L1
⑦ Perform the write operation
⑧ Set the dirty bit.

5.5.4.

For a.

Minimum read bandwidth = $\frac{32}{1000}$ = 0.032 bytes per cycle

Minimum write bandwidth = $\frac{128}{1000}$ = 1.28 bytes per cycle

For b.

Minimum read bandwidth = $\frac{57.6}{1000}$ = 0.0576 bytes per cycle

Minimum write bandwidth = $\frac{192}{1000}$ = 1.92 bytes per cycle

5.5.5.

For a.

Read bandwidth = $\frac{32}{1000}$ = 0.032 bytes per instruction

Minimum read bandwidth = $\frac{0.032}{2}$ = 0.016 bytes per cycle

Write bandwidth = $\frac{33.28}{1000}$ = 0.03328 bytes per instruction

Minimum write bandwidth = $\frac{0.03328}{2}$ = 0.01664 bytes per cycle

For b.

Read bandwidth = $\frac{57.6}{1000}$ = 0.0576 bytes per instruction

Minimum read bandwidth = $\frac{0.0576}{2}$ = 0.0288 bytes per cycle

Write bandwidth = $\frac{49.92}{1000}$ = 0.04992 bytes per instruction

Minimum write bandwidth = $\frac{0.04992}{2}$ = 0.02496 bytes per cycle

5.5.6

For a.

Minimum read bandwidth = $\frac{0.032}{1.5}$ = 0.02133 bytes per cycle

Minimum write bandwidth = $\frac{0.03328}{1.5}$ = 0.02219 bytes per cycle

For b.

Minimum read bandwidth = $\frac{0.0576}{1.5}$ = 0.0384 bytes per cycle

Minimum write bandwidth = $\frac{0.24992}{1.5}$ = 0.03328 bytes per cycle

Exercise 5.11

5.11.1.

$$\text{Number of PTEs} = \frac{\text{Virtual address space}}{\text{Page size}}$$

Memory Needed = Number of PTEs × PTE size

For a.

$$\text{Number of PTEs} = \frac{2^{32}}{2^{13}} = 2^{19}$$

Memory Needed $= 2^{19} \times 4 \text{ bytes} = 2^{21} \text{ bytes} = 2 \text{ MB}$

For b.

$$\text{Number of PTEs} = \frac{2^{64}}{2^{12}} = 2^{52}$$

Memory Needed $= 2^{52} \times 8 \text{ bytes} = 2^{55} \text{ bytes} = 2^{45} \text{ TB} = 32 \text{ PB}$

5.11.2 For a.

$$\text{Number of entries per table} = \frac{8\text{KB}}{4 \text{ bytes}} = 2^{11}$$

32 bits = Page number bits + offset bits

Page number bits: $32 - 13 = 19$ bits

offset bits: $2^{13} = 8\text{KB}$

Using 2^k levels: $k = \frac{19}{11} = 2$ levels

Total references = 2 (levels) + 1 (data) = 3

So:

Number of levels = 2

Memory references = 3

For b

Number of entries per table = $\frac{4KB}{8bytes} = 512 = 2^9$

64 bits = Page number bits + offset bits

↓ 64 − 12 = 52 bits

↓ $2^{12} = 4KB$

Using 2^k levels: $k = \frac{52}{9} = 6$ levels

Total references = 6 (levels) + 1 (data) = 7

So:

Number of levels = 6

Memory References: 7

5.11.3

Number of frames = $\frac{\text{physical memory}}{\text{page size}}$

For a

Number of frames = $\frac{4GB}{8KB} = 2^{19}$

For b.

Number of frames = $\frac{16GB}{4KB} = 2^{22}$

Common case: 1 memory reference

Worst case: Typically 2-3 memory references.

5.11.4.

① Page Table Update
② Context Switch
③ TLB Shootdown
④ Page Replacement

5.11.5

Write to VA Page 30:

① TLB Miss
② Page Table Look up
③ Update TLB
④ Write to Memory

Software-managed TLB faster when:

① Custom Optimization
② Complex policies
③ Fewer context Switches

5.11.6

TLB Lookup:

①TLB Hit
②.TLB Miss: Page Table Walk; Update TLB; Write to Memory

Protection Check:

① RW(Read-Write): write allowed
② RO(Read-Only): Causes a protection fault