# ISA & Microarchitecture

## Base+offset Addressing Mode in MIPS

- In MIPS, lw and sw use base+offset mode (or base addressing mode)

High-level code

```
A[2] = a;
```

MIPS assembly

```
sw    $s3, 8($s0)
```

Memory[$s0 + 8] ← $s3

Field Values

| op | rs | rt | imm |
|---|---|---|---|
| 43 | 16 | 19 | 8 |

- imm is the 16-bit offset, which is sign-extended to 32 bits

## Immediate Addressing Mode in MIPS

- In MIPS, lui (load upper immediate) loads a 16-bit immediate into the upper half of a register and sets the lower half to 0

ori (OR immediate) performs a bitwise OR between a register and an immediate value.

- It is used to assign 32-bit constants to a register

Followed by `lui` to set the lower 16 bits of the register.

High-level code

```
a = 0x6d5e4f3c;
```

MIPS assembly

```
# $s0 = a
lui   $s0, 0x6d5e
ori   $s0, 0x4f3c
```

# Control Flow Instructions

Allow a program to execute out of sequence.

Conditional branches and unconditional jumps

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Conditional branches are used to make decisions
E.g if-else statement.

Jumps are used to implement
Loops
Function calls

# Conditional Branches in MIPS

- beq (Branch if Equal)

```
beq  $s0, $s1, offset
```


  - 4 = opcode
  - rs, rt = source registers
  - offset = immediate or constant value
  - if rs == rt
    - then PC ← PC† + sign-extend(offset) * 4
  - Variations: beq, bne, blez, bgtz

branch greater than zero

branch not equal

branch less than zero

# The Dataflow Model

Von Neumann Model: An instruction is fetched and executed in control flow order

- As specified by the PC
- Sequential unless explicit control flow instruction

Dataflow model: An instruction is fetched and executed in data flow order

- there is no PC
- Instruction ordering specified by data flow dependence
  - Each instruction specifies "who" should receive the result
  - An instruction can "fire" whenever all operands are received.
- Potentially many instructions can execute at the same time.

# More on Dataflow:

In a dataflow machine, a program consists of dataflow nodes.

A dataflow node fires when all its inputs are ready:

i.e. when all inputs have tokens

## ISA-level Trade-off: PC

Q: Do we want a PC in the ISA?

Yes: control-driven, sequential execution

An instruction is executed when the PC points to it
PC automatically changes sequentially (except for control instructions)

No: Data-driven, parallel execution

An instruction is executed when all its operand values are available → dataflow

# What is Computer Architecture?

ISA + microarchitecture

- **ISA+implementation definition:** The science and art of designing, selecting, and interconnecting hardware components and designing the hardware/software interface to create a computing system that meets functional, performance, energy consumption, cost, and other specific goals.

except for microarchitecture.

- **Traditional (ISA-only) definition:** "The term *architecture* is used here to describe the attributes of a system as seen by the programmer, i.e., the conceptual structure and functional behavior ***as distinct from*** the organization of the dataflow and controls, the logic design, and the physical implementation."

  *Gene Amdahl*, IBM Journal of R&D, April 1964