BVM Engineering College, VV Nagar

Gujarat Technological University

VLSI

SEM 6 PRESENTATION

SR Latch & FFs using NOR Logic

Electronics & Communication Dept.

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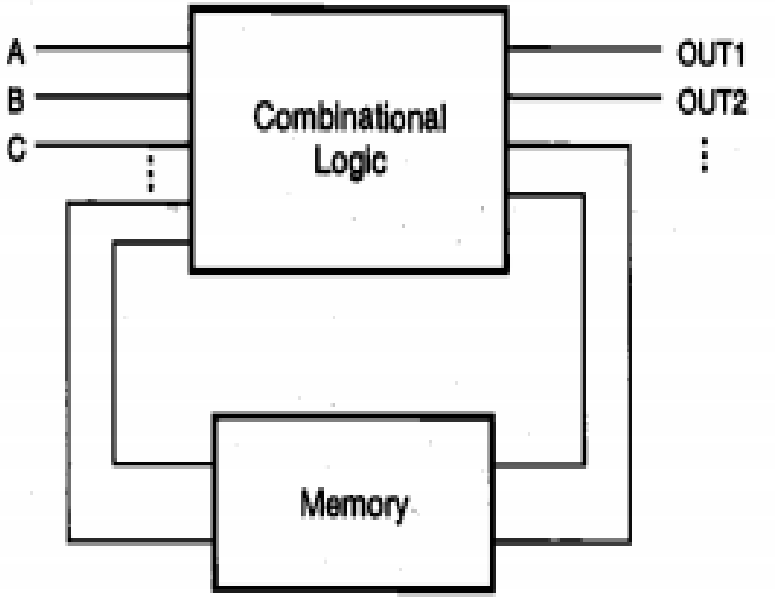
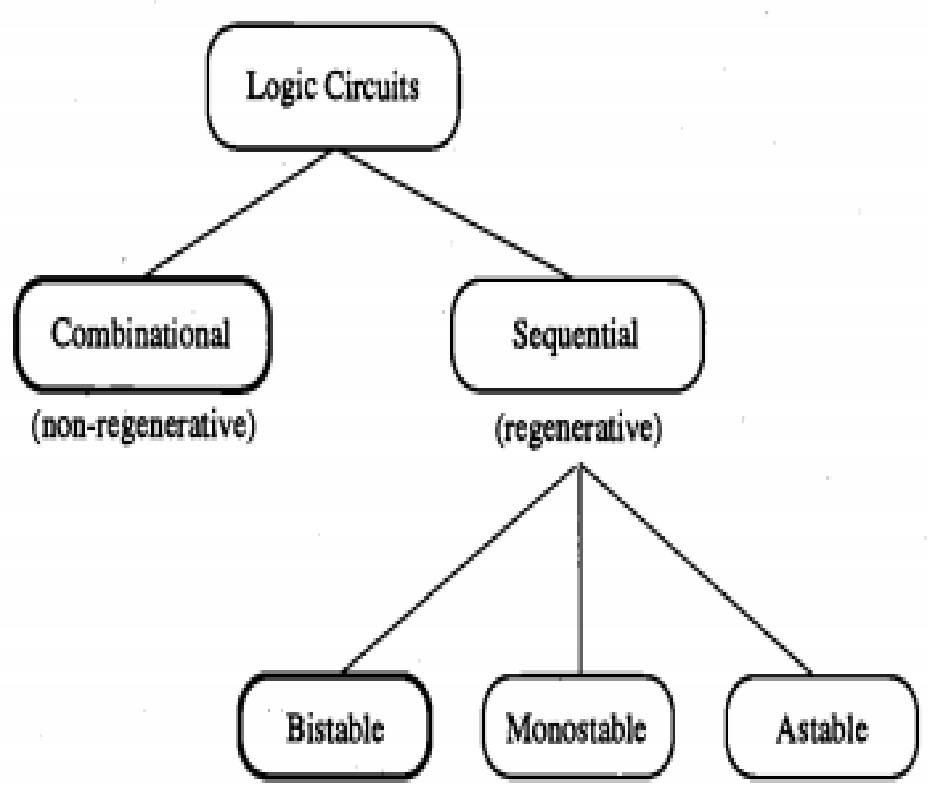
Logic Circuits: Types





Logic Circuits: Sequential Types

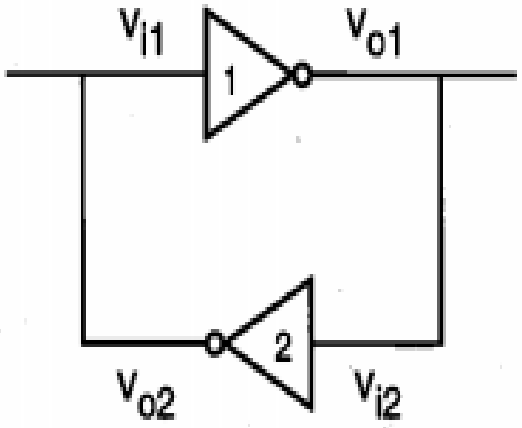
- **BISTABLE:** as their name implies, two stable states or operation modes, each of which can be attained under certain input and output conditions.

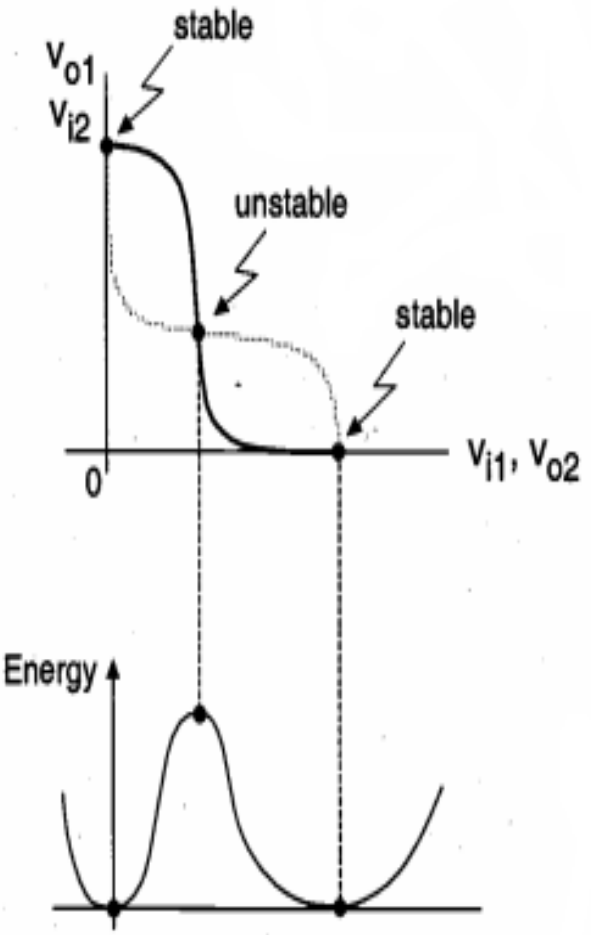
- **MONOSTABLE:** have only one stable operating point (state). Even if the circuit experiences an external perturbation, the output eventually returns to the single stable state after a certain time period.

- **ASTABLE:** there is no stable operating point or state which the circuit can preserve for a certain time period. Consequently, the output of an astable circuit must oscillate without settling into a stable operating mode.

- **NOTE:** Among these three main groups of regenerative circuit types, the bistable circuits are by far the most widely used 'and the most important class. All basic latch and flip-flop circuits, registers, and memory elements used in digital systems fall into this category.

Bistable Elements: Behaviour

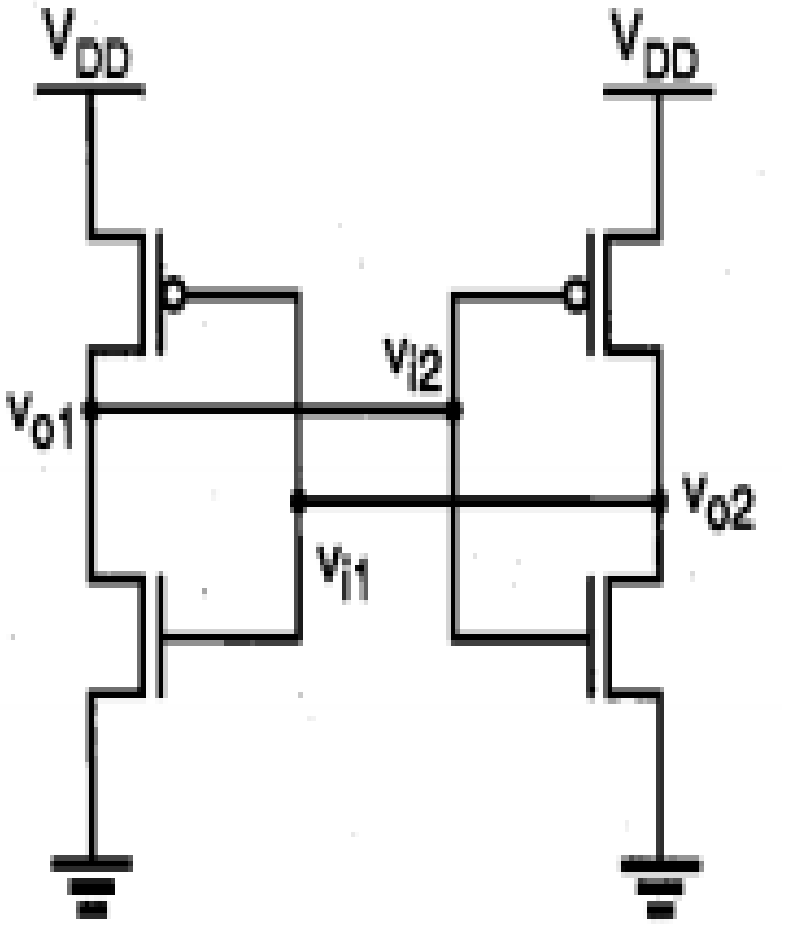


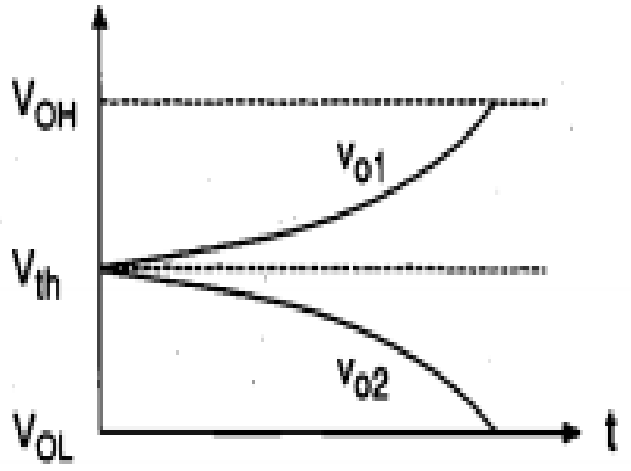


- There are two stable states of bistable elements as shown.
- If the circuit is initially operating at one of the two stable points, it will preserve this state unless it is forced externally to change its state.
- the gain of each inverter circuit, i.e., the slope of the voltage transfer curves, is smaller than unity at the two stable operating points.

Thus, in order to change the state by moving the operating point from one stable point to the other, a sufficiently large external voltage perturbation must be applied so that the voltage gain of the inverter loop becomes larger than unity

Bistable Elements: CMOS Implementation



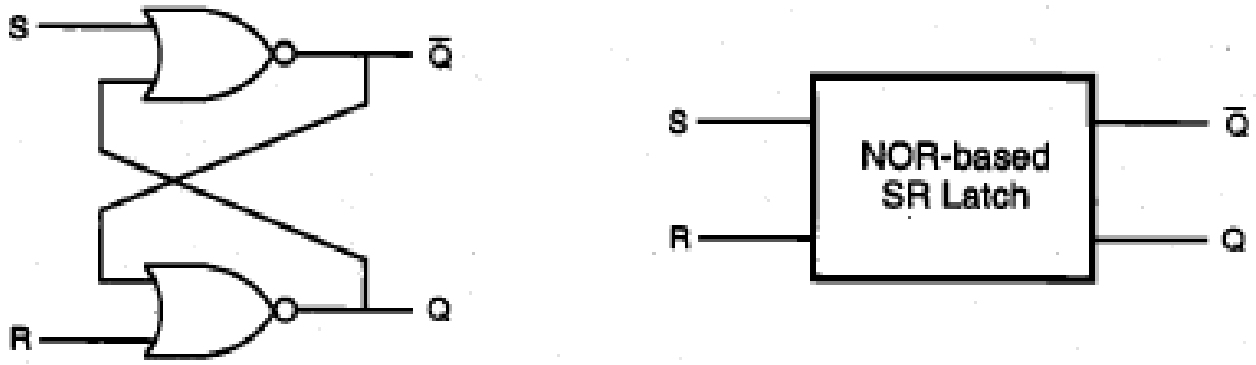


SR Latch

- An SR latch has two such triggering inputs, S (set) and R (reset), with a truth-table as shown:

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	Q_n	$\overline{Q_n}$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

SR Latch: CMOS-NOR2 Implementation



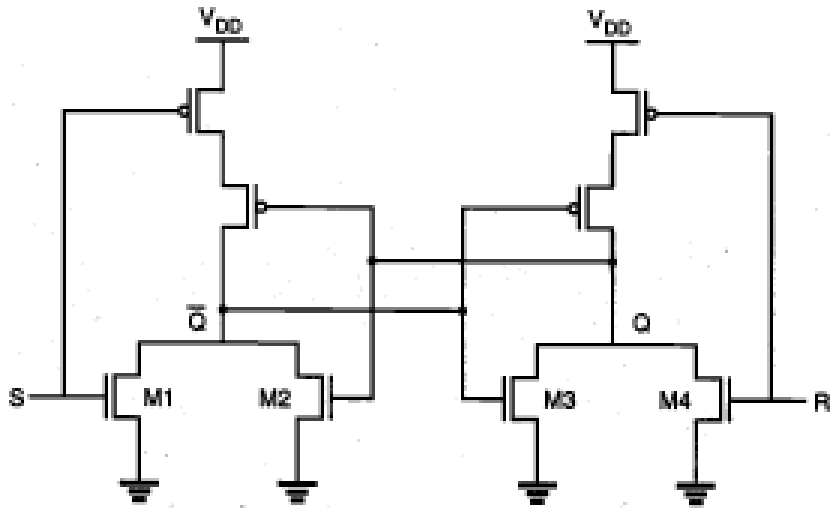
e 8.8. Gate-level schematic and block diagram of the NOR-based SR latch.

- The circuit consists of two CMOS NOR2 gates. One of the input terminals of each NOR gate is used to cross-couple to the output of the other NOR gate, while the second input enables triggering of the circuit.

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	Q_n	$\overline{Q_n}$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

Truth table of the NOR-based SR latch circuit

SR Latch: Operating Modes



.7. CMOS SR latch circuit based on NOR2 gates.

The operation of the CMOS SR latch circuit shown in Fig. 8.7 can be examined in more detail by considering the operating modes of the four nMOS transistors, M1, M2, M3, and M4. If the set input (S) is equal to V_{OH} and the reset input (R) is equal to V_{OL}, both of the parallel-connected transistors M1 and M2 will be on. Consequently, the voltage on node $\overline{Q}$ will assume a logic-low level of $V_{OL} = 0$. At the same time, both M3 and M4 are turned off, which results in a logic-high voltage V_{OH} at node Q. If the reset input (R) is equal to V_{OH} and the set input (S) is equal to V_{OL}, the situation will be reversed (M1 and M2 turned off and M3 and M4 turned on).

When both of the input voltages are equal to V_{OL}, on the other hand, there are two possibilities. Depending on the previous state of the SR latch, either M2 *or* M3 will be on, while both of the trigger transistors M1 and M4 are off. This will generate a logic-low level of $V_{OL} = 0$ at one of the output nodes, while the complementary output node is at V_{OH}. The static operation modes and voltage levels of the NOR-based CMOS SR latch circuit are summarized in the following table. For simplicity, the operating modes of the complementary pMOS transistors are not explicitly listed here.

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
V_{OH}	V_{OL}	V_{OH}	V_{OL}	M1 and M2 on, M3 and M4 off
V_{OL}	V_{OH}	V_{OL}	V_{OH}	M1 and M2 off, M3 and M4 on
V_{OL}	V_{OL}	V_{OH}	V_{OL}	*M*1 and M4 off, M2 on, or
V_{OL}	V_{OL}	V_{OL}	V_{OH}	M1 and M4 off, M3 on

Table 8.2. Operation modes of the transistors in the NOR-based CMOS SR latch circuit.

SR Latch: Lumped Capacitance

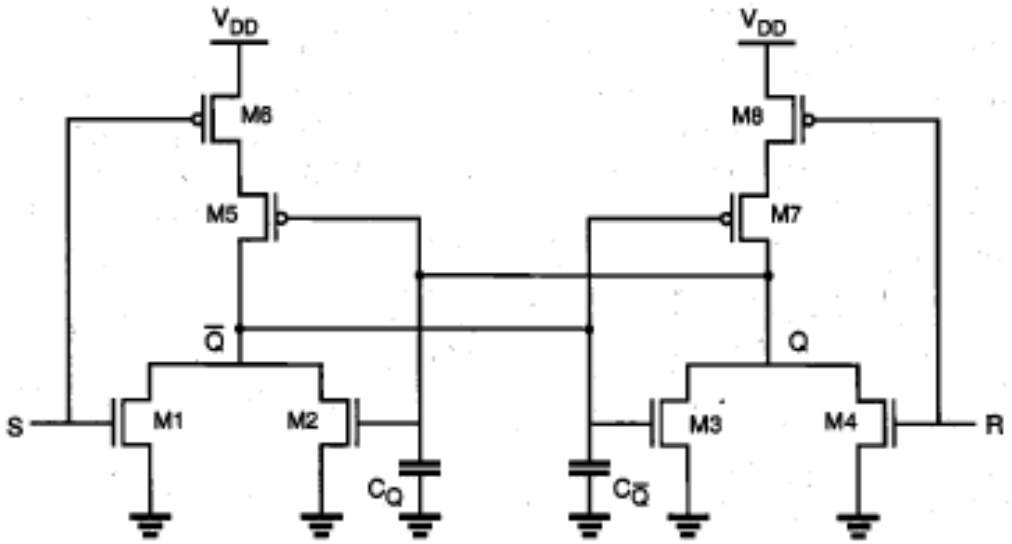


Figure 8.9. Circuit diagram of the CMOS SR latch showing the lumped load capacitances at both output nodes.

Total Lumped Capacitance

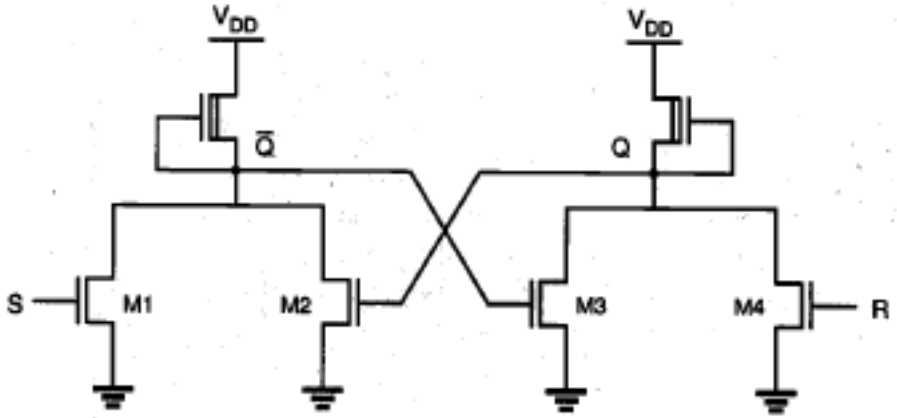
$$C_Q = C_{gb,2} + C_{gb,5} + C_{db,3} + C_{db,4} + C_{db,7} + C_{sb,7} + C_{db,8}$$

$$C_{\overline{Q}} = C_{gb,3} + C_{gb,7} + C_{db,1} + C_{db,2} + C_{db,5} + C_{sb,5} + C_{db,6}$$

Node-Q: Rise Time

$$\tau_{rise,Q}(SR-latch) = \tau_{rise,Q}(\text{NOR2}) + \tau_{fall,\overline{Q}}(\text{NOR2})$$

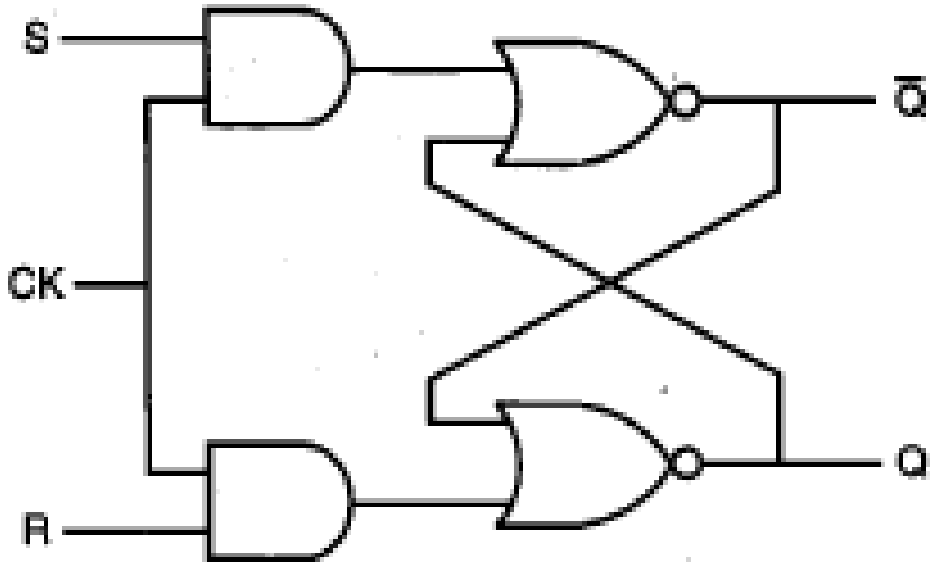
SR Latch: Depletion nMOS Implementation



8.10. Depletion-load nMOS SR latch circuit based on NOR2 gates.

The NOR-based SR latch can also be implemented by using two cross-coupled depletion-load nMOS NOR2 gates, as shown in Fig. 8.10. From the logic point of view, the operation principle of the depletion-load nMOS NOR-based SR latch is identical to that of the CMOS SR latch. In terms of power dissipation and noise margins, however, the CMOS circuit implementation offers a better alternative, since both of the CMOS NOR2 gates dissipate virtually no static power for preserving a state, and since the output voltages can exhibit a full swing between 0 and V_{DD}.

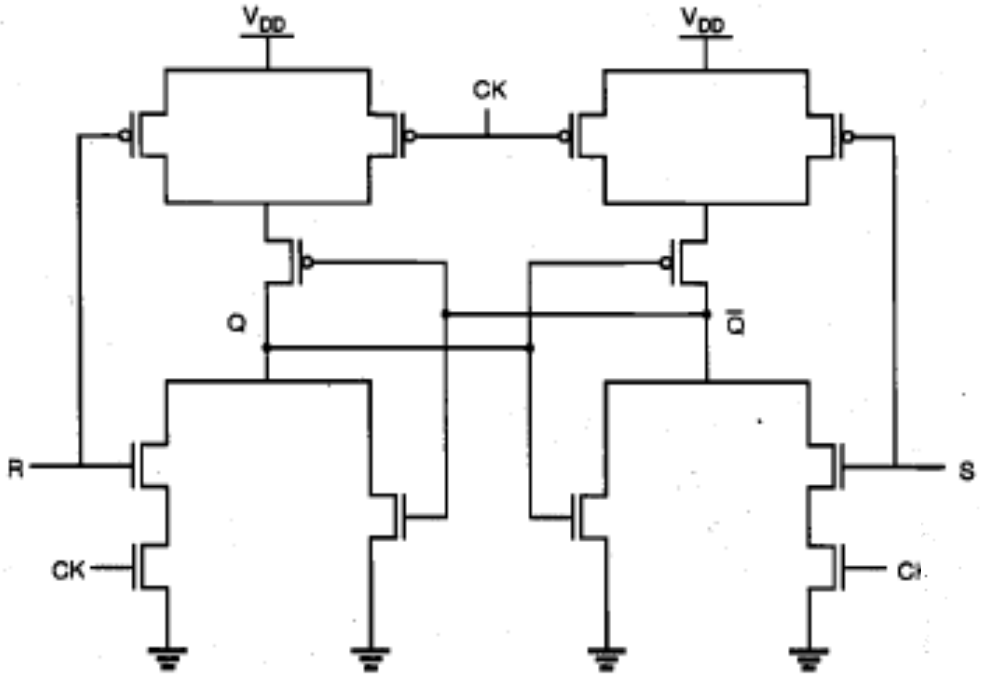
SR Latch: Clocked Circuit



S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	1	1	not allowed
0	1	1	0	set
1	0	0	1	reset
1	1	Q_n	$\overline{Q_n}$	hold

Gate-level schematic of the clocked NOR-based SR latch.

SR Latch: NOR-based FlipFlop



.16. AOI-based implementation of the clocked NOR-based SR latcl

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	1	1	not allowed
0	1	1	0	set
1	0	0	1	reset
1	1	Q_n	$\overline{Q_n}$	hold

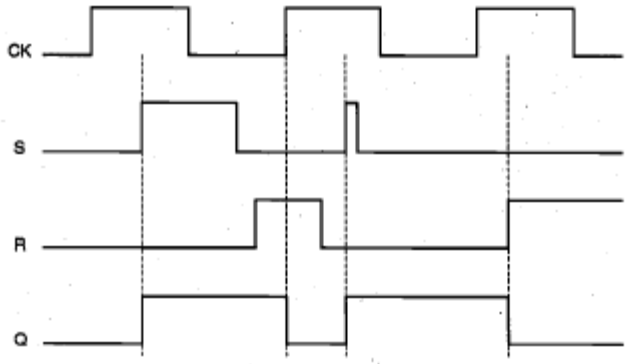


Figure 8.15. Sample input and output waveforms illustrating the operation of the clocked NOR-based SR latch circuit.

THANK YOU !