BVM Engineering College, VV Nagar

Gujarat Technological University

OPTICAL COMMUNICATION

SEM 6 PRESENTATION

SONET

Electronics & Communication Dept.

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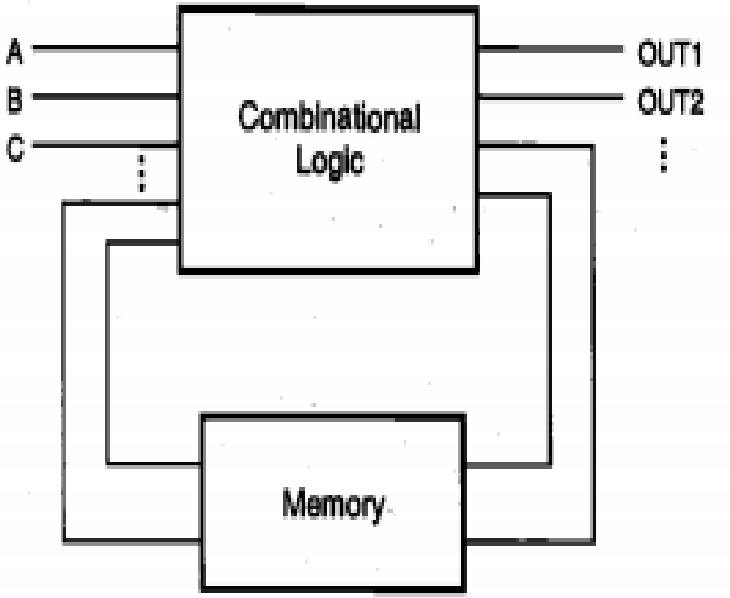
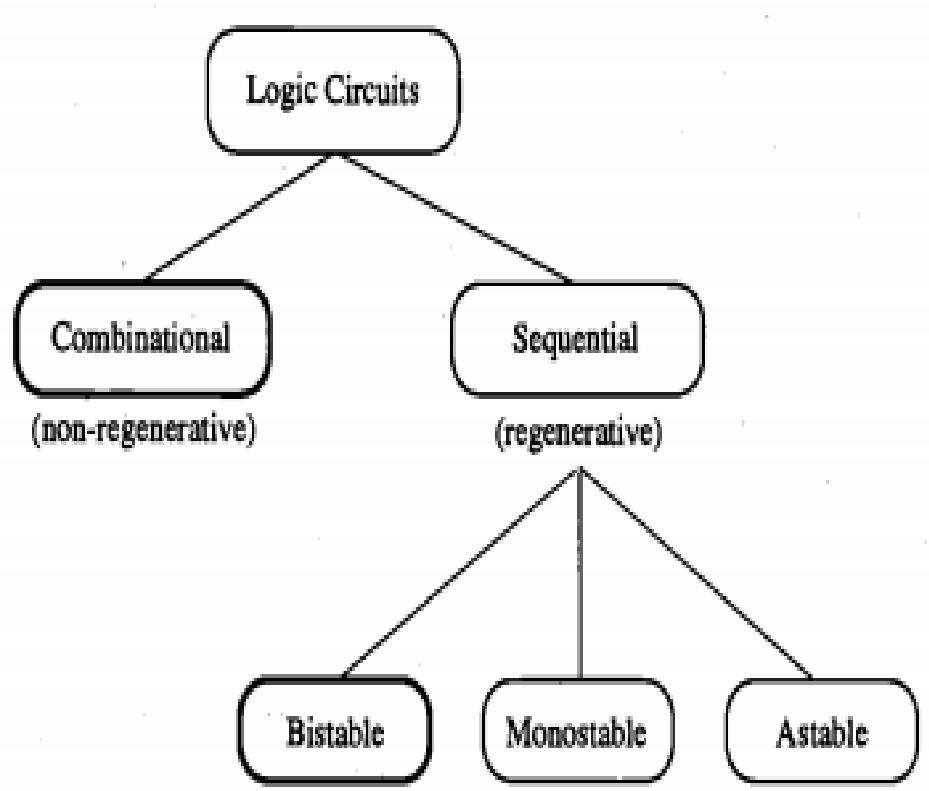
INTRODUCTION





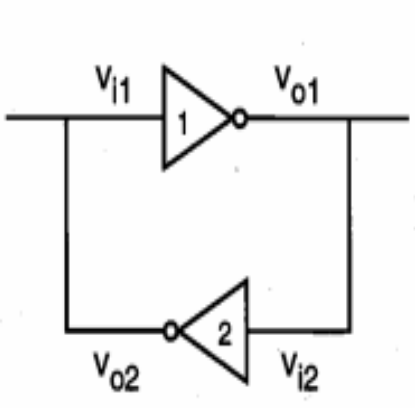
- BISTABLE: as their name implies, two stable states or operation modes, each of which can be attained under certain input and output conditions.

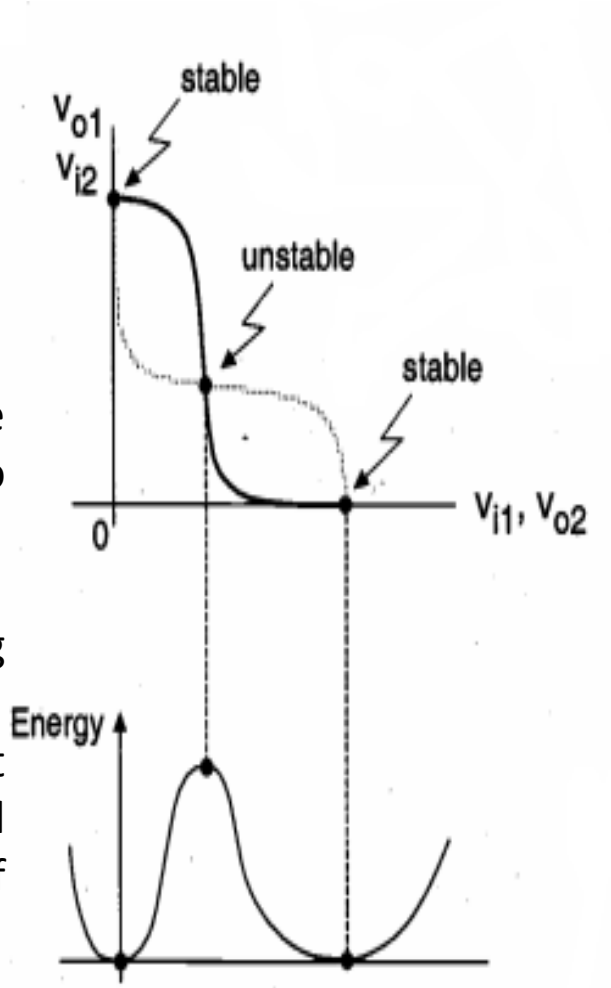
- MONOSTABLE: have only one stable operating point (state). Even if the circuit experiences an external perturbation, the output eventually returns to the single stable state after a certain time period.

- ASTABLE: there is no stable operating point or state which the circuit can preserve for a certain time period. Consequently, the output of an astable circuit must oscillate without settling into a stable operating mode.

- NOTE: Among these three main groups of regenerative circuit types, the bistable circuits are by far the most widely used 'and the most important class. All basic latch and flip-flop circuits, registers, and memory elements used in digital systems fall into this category

Behavior of Bistable Elements

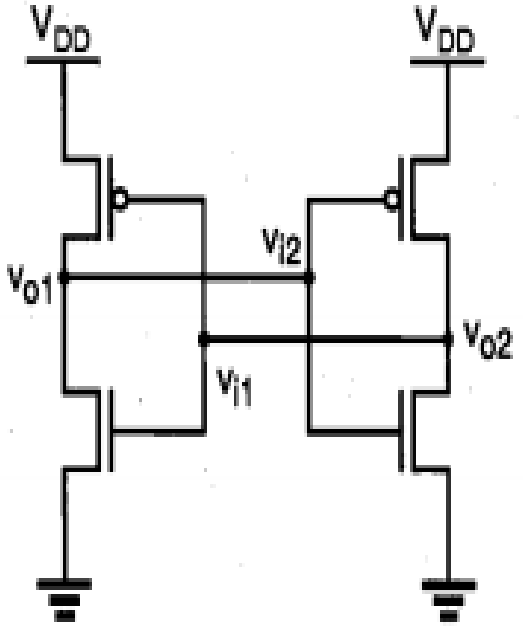


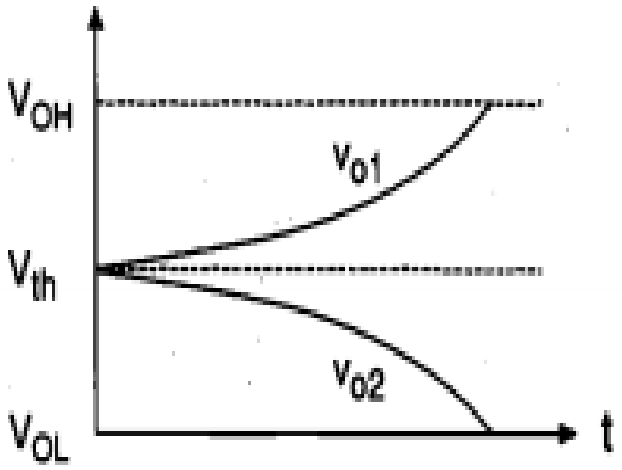


- There are two stable stated of bistable elements as shown.
- If the circuit is initially operating at one of the two stable points, it will preserve this state unless it is forced externally to change its state.
- the gain of each inverter circuit, i.e., the slope of the voltage transfer curves, is smaller than unity at the two stable operating points.

Thus, in order to change the state by moving the operating point from one stable point to the other, a sufficiently large external voltage perturbation must be applied so that the voltage gain of the inverter loop becomes larger than unity

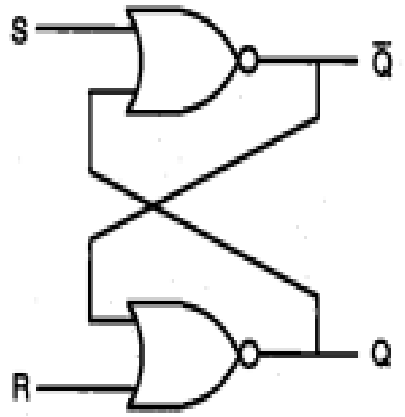
- It is seen that the potential energy is at its minimum at two of the three operating points, since the voltage gains of both inverters are equal to zero. By contrast, the energy attains a maximum at the operating point at which the voltage gains of both inverters are maximum.
- at the unstable operating point of this circuit, all four transistors are in saturation, resulting in maximum loop gain for the circuit. If the initial operating condition is set at this point, any small voltage perturbation will cause significant changes in the operating modes of the transistors.
- Thus, we expect the output voltages of the two inverters to diverge and eventually settle at VOH and VOL, respectively, as illustrated

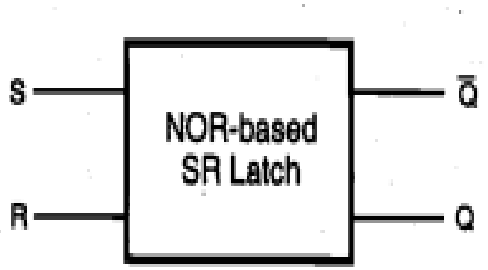




SR Latch Circuit

- the circuit structure of the simple CMOS SR latch, which has two such triggering inputs, S (set) and R (reset).
- the SR latch is also called an SR flip-flop, since two stable states can be switched back and forth.
- The circuit consists of two CMOS NOR2 gates.
- One of the input terminals of each NOR gate is used to cross-couple to the output of the other NOR gate, while the second input enables triggering of the circuit.



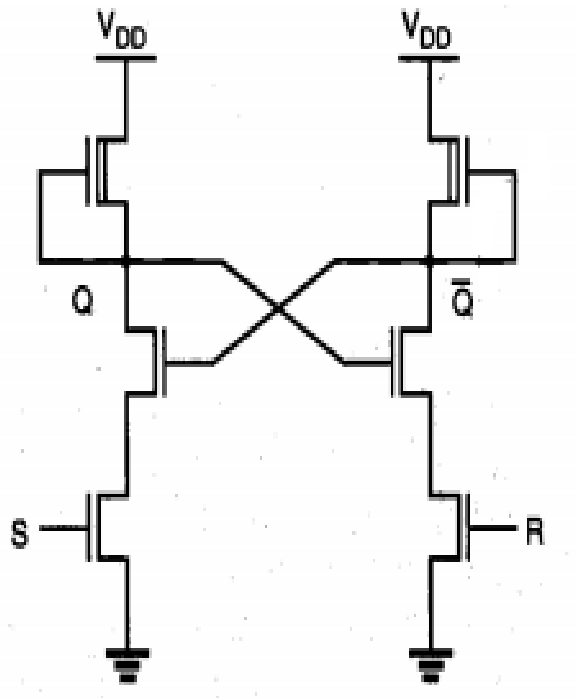


Truth table of NOR based SR latch circuit

S	R	Q_{n+1}	$\overline{Q}_{n+1}$	Operation
0	0	Q_n	$\overline{Q_n}$	Hold
1	0	1	0	Set
0	1	0	1	Reset
1	1	0	0	Not allowed

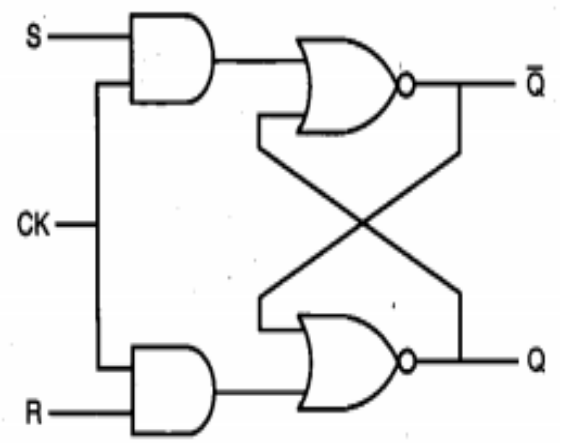
- if S is equal to "0" and R is equal to " 1," then the output node Q will be forced to "0" while Q is forced to "1.“
- Thus, with this input combination, the latch is reset, regardless of its previously held state.
- Finally, consider the case in which both of the inputs S and R are equal to logic “1 .“
- In this case, both output nodes will be forced to logic "0," which conflicts with the complementarity of Q and Q.
- Therefore, this input combination is not permitted during normal operation and is considered to be a not allowed condition.

Depletion load nMOS SR latch



CMOS SR Latch circuit based on NOR2 gate

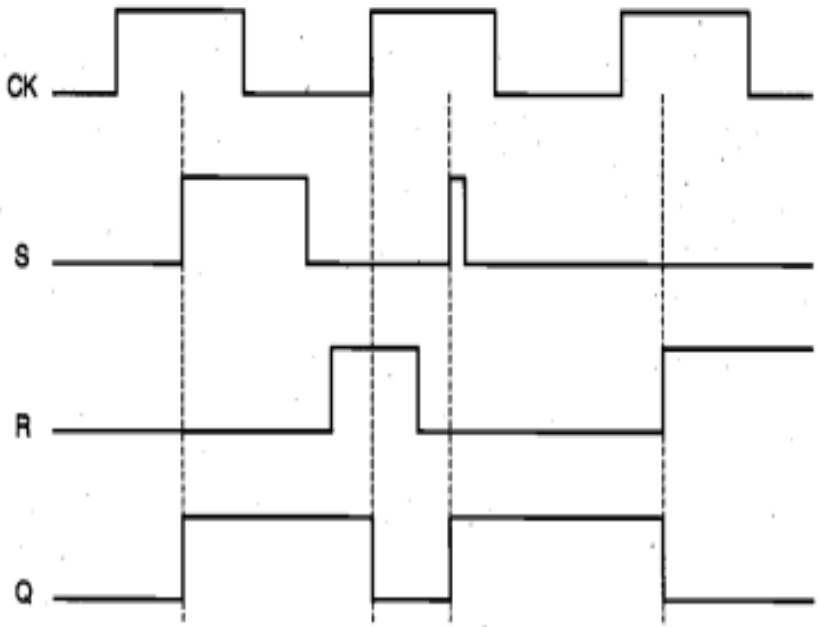
CLOCKED LATCH:FLIPFLOP CIRCUITS

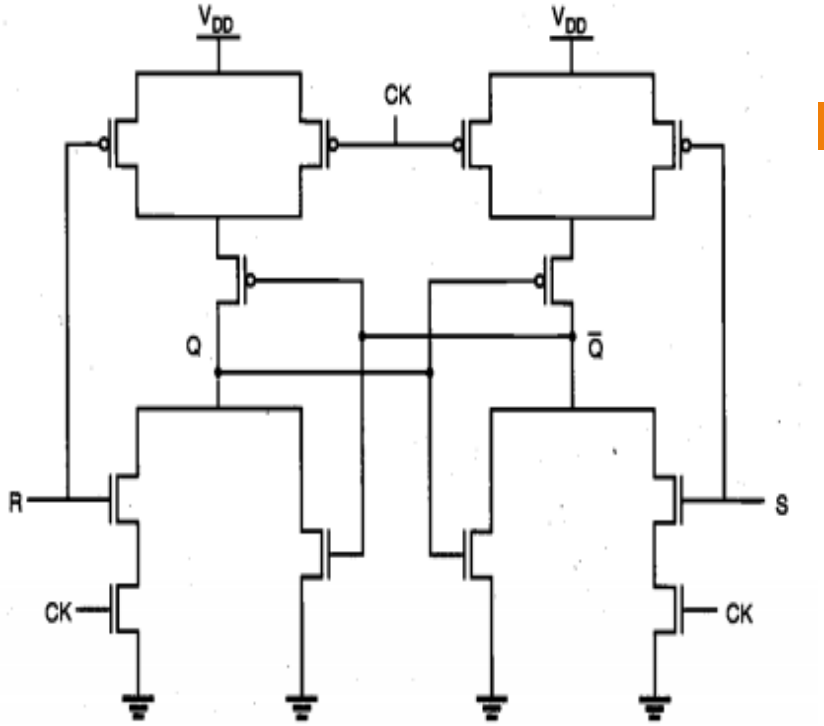


- Asynchronous sequential circuits, which will respond to the changes occurring in input signals at a circuit-delay-time point during their operation.

- To facilitate synchronous operation, the circuit response can be controlled simply by adding a gating clock signal to the circuit, so that the outputs will respond to the input levels only during the active period of a clock pulse.

- It can be seen that if the clock (CK) is equal to logic "0," the input signals have no influence
- When the clock input goes to logic " 1," the logic levels applied to the S and R inputs are pe and possibly change its state.
- the circuit is strictly level-sensitive during active clock phases, i.e., any changes occurring. in th when the CK level is equal to " 1 " will be reflected onto the circuit outputs.





Sample input and output waveforms illustrating the operation of the clocked NOR based SR latch circuit. clocked NOR-based SR latch circuit.

Both input signals S and R as well as the clock signal CK are active low in case of NAND.

Operation modes of the transistors in the NOR-based CMOS SR latch circuit

- If $S=V_{OH}$, $R=V_{OL}$
  - M1, M2 on $\Rightarrow$ node $-Q=V_{OL}=0$
  - M3, M4 off $\Rightarrow$ node $Q=V_{OH}$
- If $S=V_{OH}$, $R=V_{OL}$, the situation will reverse
- If $S=V_{OL}$, $R=V_{OL}$, there are two possibilities
  - Depending on the previous state of the SR latch
  - Either M2 or M3 on (while M1, M4 off)
    - Generating a logic low level of $V_{OL}=0$ at one of the output nodes
    - While the complementary output node is at V_{OH}

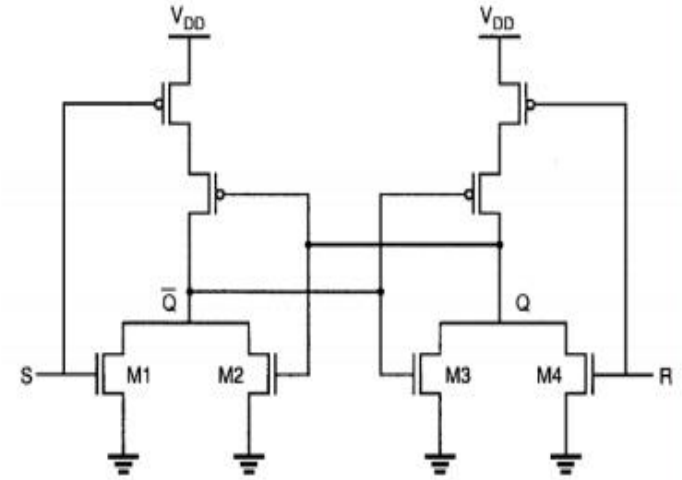


Table 8.2 Operation modes of the transistors in the NOR-based CMOS SR latch circuit

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
V_{OH}	V_{OL}	V_{OH}	V_{OL}	M1 and M2 on, M3 and M4 off
V_{OL}	V_{OH}	V_{OL}	V_{OH}	M1 and M2 off, M3 and M4 on
V_{OL}	V_{OL}	V_{OH}	V_{OL}	M1 and M4 off, M2 on, or
V_{OL}	V_{OL}	V_{OL}	V_{OH}	M1 and M4 off, M3 on

Transient analysis of the SR latch circuit

$$C_Q = C_{gb,2} + C_{gb,5} + C_{db,3} + C_{db,4} + C_{db,7} + C_{SB,7} + C_{db,8}$$

$$C_{\overline{Q}} = C_{gb,3} + C_{gb,7} + C_{db,1} + C_{db,2} + C_{db,5} + C_{SB,5} + C_{db,6}$$

Assuming that the latch is initially reset and that a set operation is being performed by applying S ="1" and R ="0", the rise time associated with node Q can now be estimated as follows

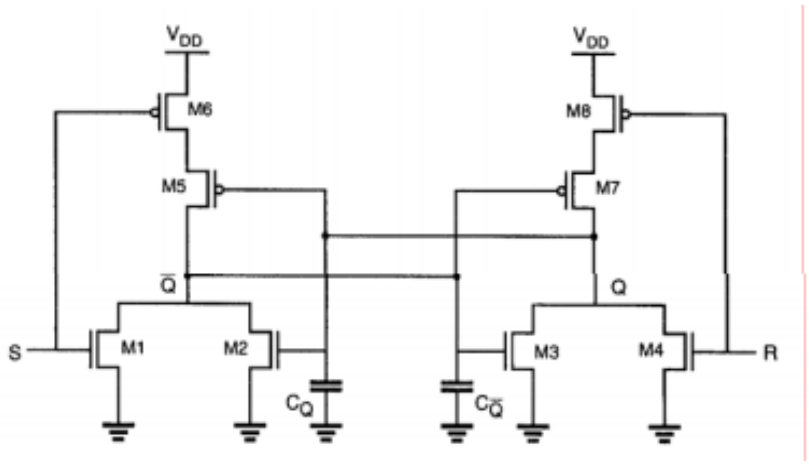
$$\tau_{\text{rise},Q}(\text{SR - latch}) = \tau_{\text{rise},Q}(\text{NOR2}) + \tau_{\text{fall},\overline{Q}}(NOR2)$$

The calculation of the switching time $\tau_{\text{rise},Q}$ requires two separate calculations for the rise and fall times of the NOR2 gates

First, M1 turn on $\Rightarrow \overline{Q}$ falling from high to low; followed M3 turn off $\Rightarrow$ Q rising from low to high

both M2 and M4 can be assumed to be off in this process

(although M2 can be turned on as Q rises)



THANK YOU !