A

PROJECT REPORT ON

MOD-100 COUNTER

DIGITAL ELECTRONICS (2131004)

BACHELOR OF ENGINEERING

In

ELECTRONICS AND COMMUNICATION ENGINEERING

By

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GUJARAT TECHNOLOGICAL UNIVERSITY

VALLABH VIDYANAGAR-388120

Academic Year – 2015/16

CERTIFICATE

This is to certify that the project report entitled **"MOD-100 COUNTER",** submitted by **Chaitanya Tejaswi (140080111013)** in the subject of *Digital Electronics* for the course of *Bachelor of Engineering* in *Electronics and Communication* at *BVM Engineering College, Vallabh Vidyanagar*, affiliated to the *Gujarat Technological University*, is the record of work carried out by him under my supervision and guidance. In my opinion, the submitted work has reached a level required for being accepted for examination.

Under The Guidance Of
Prof. Anish Vahora
Professor
ET Dept, BVM
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I am thankful to *Professor Anish Vahora* for giving me this project, and also the necessary guidance through regular interactions. Also, I thank my parents, friends and family for their continual support.

I would also express my regards for all the dedicated men (and women) in the field of *Digital Logic & Design* for giving us a wide scope of understanding of using binary methods to design practically useful designs and also appreciate the true beauty of discrete systems.

At last, I pay regards to authors whose books I have referred on and off in my study for the subject, for their sincere efforts to present the current level of understanding in the field in the best possible yet straightforward way.

CONTENTS

1
COUNTER

In digital logic and computing, a **counter** is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. The most common type is a sequential digital logic circuit with an input line called the "clock" and multiple output lines. The values on the output lines represent a number in the binary or BCD number system. Each pulse applied to the clock input increments or decrements the number in the counter.

A counter circuit is usually constructed of a number of flip-flops connected in cascade. Counters are a very widely-used component in digital circuits, and are manufactured as separate integrated circuits and also incorporated as parts of larger integrated circuits.

Contents

Electronic Counters

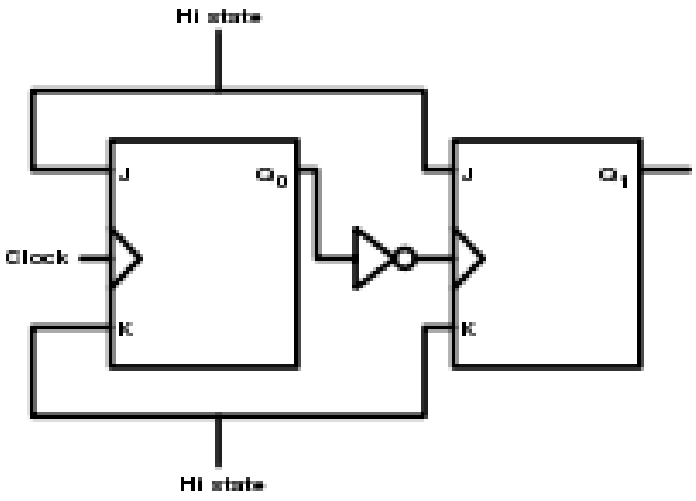
- Asynchronous (ripple) Counter – changing state bits are used as clocks to subsequent state flip-flops
- Synchronous Counter – all state bits change under control of a single clock
- Decade Counter – counts through ten states per stage
- Up/down Counter – counts both up and down, under command of a control input
- Ring Counter – formed by a shift register with feedback connection in a ring

- Johnson Counter – a *twisted* ring counter
- Cascaded Counter
- Modulus Counter

Each is useful for different applications. Usually, counter circuits are digital in nature, and count in natural binary. Many types of counter circuits are available as digital building blocks, for example a number of chips in the 4000 series implement different counters.
Occasionally there are advantages to using a counting sequence other than the natural binary sequence—such as the binary coded decimal counter, a linear feedback shift register counter, or a Gray-code counter.
Counters are useful for digital clocks and timers, and in oven timers, VCR clocks, etc.[1]

Asynchronous Counter

Asynchronous counter created from two JK flip-flops
An asynchronous (ripple) counter is a single d-type flip-flop, with its J (data) input fed from its own inverted output. This circuit can store one bit, and hence can count from zero to one before it overflows (starts over from 0). This counter will increment once for every clock cycle and takes two clock cycles to overflow, so every cycle it will alternate between a transition from 0 to 1 and a transition from 1 to 0. Notice that this creates a new clock with a 50% duty cycle at exactly half the frequency of the input clock. If this output is then used as the clock signal for a similarly arranged D flip-flop (remembering to invert the output to the input), one will get another 1 bit counter that counts half as fast. Putting them together yields a two-bit counter:



Cycle	Q1	Q0	(Q1:Q0)dec
0	0	0	0
1	0	1	1
2	1	0	2
3	1	1	3
4	0	0	0

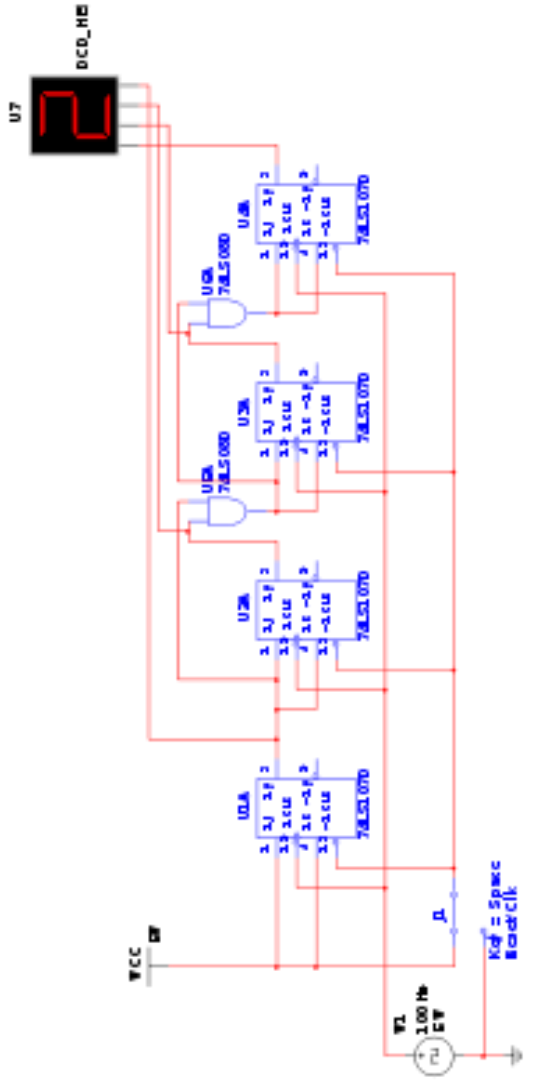
You can continue to add additional flip-flops, always inverting the output to its own input, and using the output from the previous flip-flop as the clock signal. The result is called a ripple counter, which can count to 2n - 1 where n is the number of bits (flip-flop stages) in the counter. Ripple counters suffer from unstable outputs as the overflows "ripple" from stage to stage, but they do find frequent application as dividers for clock signals, where the instantaneous count is unimportant, but the division ratio overall is (to clarify this, a 1-bit counter is exactly equivalent to a divide by two circuit; the output frequency is exactly half that of the input when fed with a regular train of clock pulses).

The use of flip-flop outputs as clocks leads to timing skew between the count data bits, making this ripple technique incompatible with normal synchronous circuit design styles.

Synchronous Counter

In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel). The circuit below is a 4-bit synchronous counter. The J and K inputs of FF0 are connected to HIGH. FF1 has its J and K inputs connected to the output of FF0, and the J and K inputs of FF2 are connected to the output of an AND gate that is fed by the outputs of FF0 and FF1. A simple way of implementing the logic for each bit of an ascending counter (which is what is depicted in the image to the right) is for each bit to toggle when all of the less significant

bits are at a logic high state. For example, bit 1 toggles when bit 0 is logic high; bit 2 toggles when both bit 1 and bit 0 are logic high; bit 3 toggles when bit 2, bit 1 and bit 0 are all high; and so on.



A 4-bit synchronous counter using JK flip-flops

Synchronous counters can also be implemented with hardware finite-state machines, which are more complex but allow for smoother, more stable transitions.

Hardware-based counters are of this type. A simple way of implementing the logic for each bit of an ascending counter (which is what is depicted in the image to the right) is for each bit to toggle when all of the less significant bits are at a logic high state.

Decade Counter

A decade counter is one that counts in decimal digits, rather than binary. A decade counter may have each (that is, it may count in binary-coded decimal, as the 7490 integrated circuit did) or other binary encodings. "A decade counter is a binary counter that is designed to count to 1010b (decimal 10). An ordinary four-stage counter can be easily modified to a decade counter by adding a NAND gate as in the schematic to the right. Notice that FF2 and FF4 provide

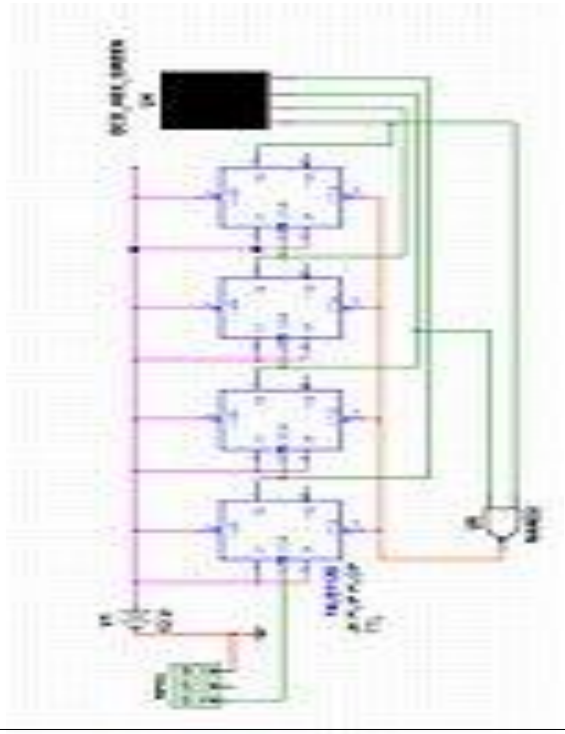
the inputs to the NAND gate. The NAND gate outputs are connected to the CLR input of each of the FFs." A decade counter is one that counts in decimal digits, rather than binary. It counts from 0 to 9 and then resets to zero. The counter output can be set to zero by pulsing the reset line low. The count then increments on each clock pulse until it reaches 1001 (decimal 9). When it increments to 1010 (decimal 10) both inputs of the NAND gate go high. The result is that the NAND output goes low, and resets the counter to zero. D going low can be a CARRY OUT signal, indicating that there has been a count of ten.

Ring Counter

Main article: Ring counter

A ring counter is a circular shift register which is initiated such that only one of its flip-flops is the state one while others are in their zero states.

A ring counter is a Shift Register (a cascade connection of flip-flops) with the output of the last one connected to the input of the first, that is, in a ring. Typically, a pattern consisting of a single bit is circulated so the state repeats every n clock cycles if n flip-flops are used.



A circuit decade counter using JK Flip-flops (74LS112D)

Johnson Counter

A Johnson counter (or switchtail ring counter, twisted-ring counter, walking-ring counter, or Moebius counter) is a modified ring counter, where the output

from the last stage is inverted and fed back as input to the first stage.[2][3][4] The register cycles through a sequence of bit-patterns, whose length is equal to twice the length of the shift register, continuing indefinitely. These counters find specialist applications, including those similar to the decade counter, digital-to-analog conversion, etc. They can be implemented easily using D- or JK-type flip-flops. It is also known as twisted ring counter.

REFERENCES

1. *Synchronous counter", Digital, Play hookey*.
2. *Singh, Arun Kumar (2006). Digital Principles Foundation of Circuit Design and Application. New Age Publishers. ISBN 81-224-1759-0.*
3. *Horowitz, Paul; Hill, Winfield (1989). The Art of Electronics. Cambridge University Press. ISBN 0-521-37095-7.*
4. *Graf, Rudolf F (1999). Modern Dictionary of Electronics. Newnes. ISBN 0-7506-9866-7.*
5. *VR History, Veeder*.

2
DISPLAY DECODER

BCD to 7-Segment Display Decoder

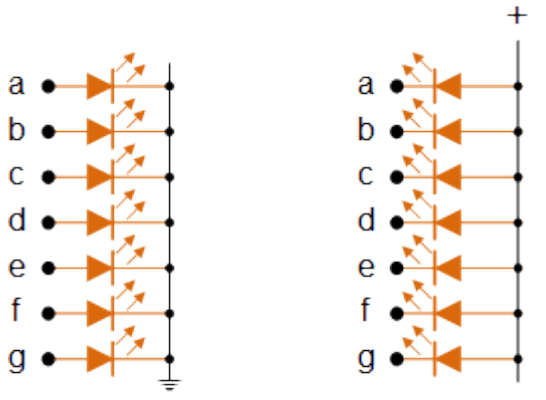
Typically, 7-segment displays consist of seven individual coloured LED's (called the segments), within one single display package. In order to produce the required numbers or HEX characters from 0 to 9 and A to F respective ly, on the display the correct combination of LED segments need to be illuminated and **BCD to 7-segment Display Decoders** such as the 74LS47 do just that.

A standard 7-segment LED display generally has 8 input connections, one for each LED segment and one that acts as a common terminal or connection for all the internal display segments. Some single displays have also have an additional input pin to display a decimal point in their lower right or left hand corner.

In electronics there are two important types of 7-segment LED digital display.

1. The Common Cathode Display (CCD) – In the common cathode display, all the cathode connections of the LED's are joined together to logic "0" or ground. The individual segments are illuminated by application of a "HIGH", logic "1" signal to the individual Anode terminals.

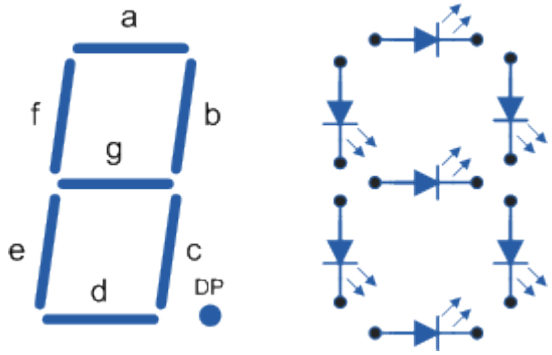
2. The Common Anode Display (CAD) – In the common anode display, all the anode connections of the LED's are joined together to logic "1" and the individual segments are illuminated by connecting the individual Cathode terminals to a "LOW", logic "0" signal.



Common Cathode & Common Anode Format

Electrical connection of the individual diodes for a common cathode display and a common anode display and by illuminating each light emitting diode individually, they can be made to display a variety of numbers or characters.

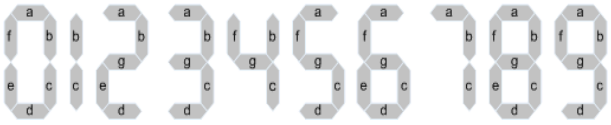
7-Segment Display Format



So in order to display the number 3 for example, segments a, b, c, d and g would need to be illuminated. If we wanted to display a different number or letter then a different set of segments would need to be illuminated. Then for a 7-segment display, we can produce a truth table giving the segments that need to be illuminated in order to produce the required character as shown below.

Individual Segments							Display
a	b	c	d	e	f	g	
×	×	×	×	×	×		0
	×	×					1
×	×		×	×		×	2
×	×	×	×			×	3
	×	×			×	×	4
×		×	×		×	×	5
×		×	×	×	×	×	6
×	×	×					7

Individual Segments							Display
a	b	c	d	e	f	g	
×	×	×	×	×	×	×	8
×	×	×	×		×	×	9
×	×	×		×	×	×	A
		×	×	×	×	×	b
×			×	×	×		C
	×	×	×	×		×	d
×			×	×	×	×	E
×				×	×	×	F



7-Segment Display Elements for all Numbers.

It can be seen that to display any single digit number from 0 to 9 in binary or letters from A to F in hexadecimal, we would require 7 separate segment connections plus one additional connection for the LED's "common" connection.

Also as the segments are basically a standard light emitting diode, the driving circuit would need to produce up to 20mA of current to illuminate each individual segment and to display the number 8, all 7 segments would need to be lit resulting a total current of nearly 140mA, (8 x 20mA).

Obviously, the use of so many connections and power consumption is impractical for some electronic or microprocessor based circuits and so in order to reduce the number of signal lines required to drive just one single display, display decoders such as the BCD to 7-Segment Display Decoder and Driver IC's are used instead.

Binary Coded Decimal

Binary Coded Decimal (BCD or "8421" BCD) numbers are made up using just 4 data bits (a nibble or half a byte) similar to the **Hexadecimal** numbers we saw in the binary tutorial, but unlike hexadecimal numbers that range in full from 0 through to F, BCD numbers only range

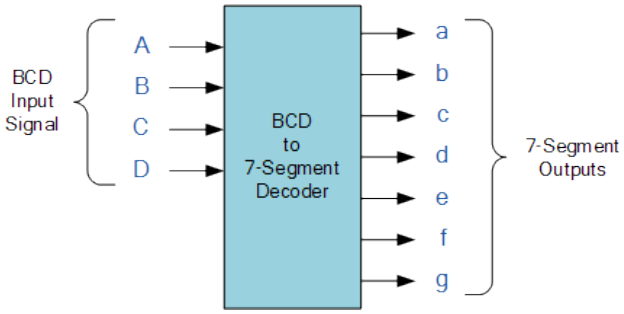
from 0 to 9, with the binary number patterns of 1010 through to 1111 (A to F) being invalid inputs for this type of display and so are not used as shown below.

BCD to 7-Segment Display Decoders

A binary coded decimal (BCD) to 7-segment display decoder such as the TTL 74LS47 or 74LS48, have 4 BCD inputs and 7 output lines, one for each LED segment. This allows a smaller 4-bit binary number (half a byte) to be used to display all the denary numbers from 0 to 9 and by adding two displays together, a full range of numbers from 00 to 99 can be displayed with just a single byte of 8 data bits.

Decimal	Binary Pattern				BCD
	8	4	2	1	
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7

Decimal	Binary Pattern				BCD
	8	4	2	1	
8	1	0	0	0	8
9	1	0	0	1	9
10	1	0	1	0	Invalid
11	1	0	1	1	Invalid
12	1	1	0	0	Invalid
13	1	1	0	1	Invalid
14	1	1	1	0	Invalid
15	1	1	1	1	Invalid

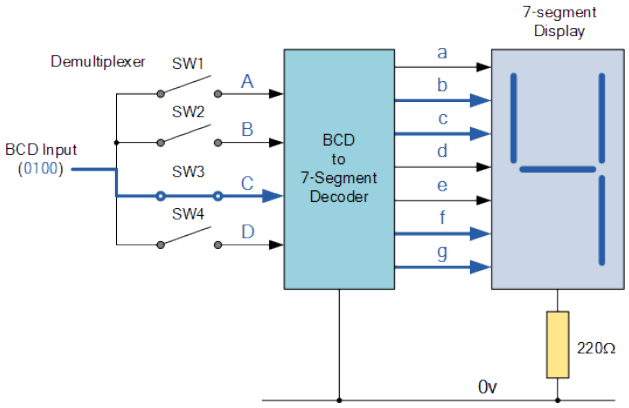


BCD to 7-Segment Decoder

The use of **packed** BCD allows two BCD digits to be stored within a single byte (8-bits) of data, allowing a single data byte to hold a BCD number in the range of 00 to 99.

An example of the 4-bit BCD input (0100) representing the number 4 is given below.

Display Decoder Example No1



In practice current limiting resistors of about 150Ω to 220Ω would be connected in series between the decoder/driver chip and each LED display segment to limit the maximum current flow. Different display decoders or drivers are available for the different types of display available, e.g. 74LS48 for common-cathode LED types, 74LS47 for common-anode LED types, or the CMOS CD4543 for liquid crystal display (LCD) types.

Liquid crystal displays (LCD´s) have one major advantage over similar LED types in that they consume much less power and nowadays, both LCD and LED displays are combined together to form larger Dot-Matrix Alphanumeric type displays which can show letters and characters as well as numbers in standard Red or Tri-colour outputs.

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised September 1998

DM7490A
Decade and Binary Counter

General Description

The DM7490A monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The counter has a gated zero reset and also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

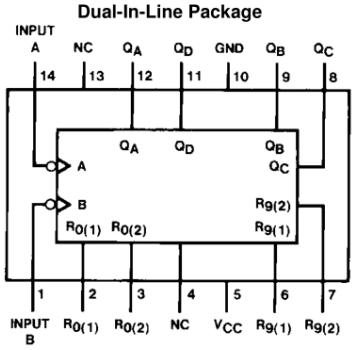
- Typical power dissipation
  - —90A 145 mW
- Count frequency 42 MHz

Ordering Code:

Order Number	Package Number	Package Description
DM7490AN	N14A	14-Lead Plastic Dual-In-Line Package, JECEC MS-001, 0.300" Wide

Connection Diagram

Dual-In-Line Package



Function Tables (Note 1)

BCD Count Sequence (Note 2)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BCD Bi-Quinary (5-2) (Note 3)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Reset/Count Function Table

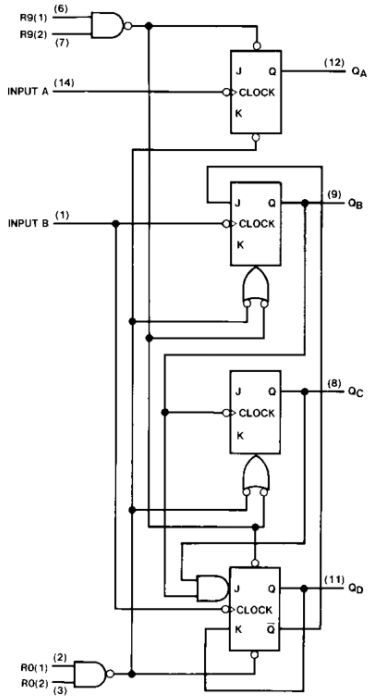
Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L		COUNT		
L	X	L	X		COUNT		
L	X	X	L		COUNT		
X	L	L	X		COUNT		

Note 1: H = High Level, L = Low Level, X = Don't Care.

Note 2: Output Q_A is connected to input B for BCD count.

Note 3: Output Q_D is connected to input A for bi-quinary count.

Logic Diagram



The J and K inputs shown without connection are for reference only and are functionally at a high level.

Absolute Maximum Ratings(Note 4)

Supply Voltage	7V	Operating Free Air Temperature Range	0°C to +70°C
Input Voltage	5.5V	Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.8	mA
I_{OL}	Low Level Output Current				16	mA
f_{CLK}	Clock Frequency	A	0		32	MHz
	(Note 5)	B	0		16	
t_W	Pulse Width	A	15			ns
	(Note 5)	B	30			
		Reset	15			
t_{REL}	Reset Release Time (Note 5)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 4: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: $T_A = 25°C$ and $V_{CC} = 5V$.

DC Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max (Note 7)			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	A			80	μA
			Reset			40	
			B			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A			−3.2	mA
			Reset			−1.6	
			B			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 8)	DM54	-20		-57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 9)			29	42	mA

Note 6: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 7: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

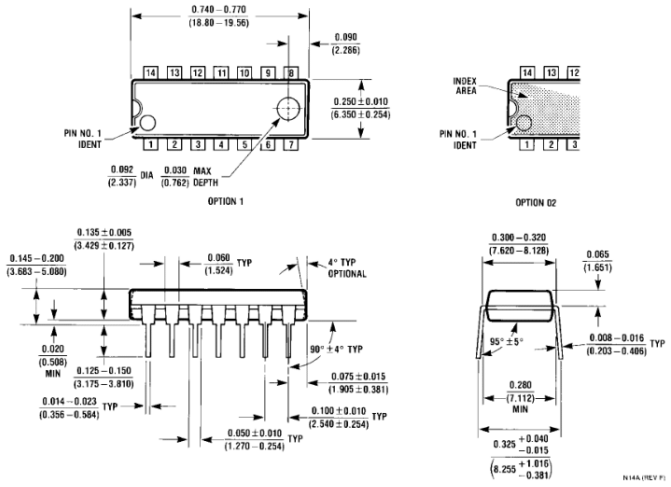
Note 8: Not more than one output should be shorted at a time.

Note 9: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

AC Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		MHz
		B to Q_B	16		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 Any Q		40	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package, JEDEC MS-001, 0.300" Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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MOTOROLA

SN54/74LS247
SN54/74LS248
SN54/74LS249

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

LOW POWER SCHOTTKY

The SN54/74LS247 thru SN54/74LS249 are BCD-to-Seven-Segment Decoder/Drivers.

The LS247 and LS248 are functionally and electrically identical to the LS47 and LS48 with the same pinout configuration. The LS249 is a 16-pin version of the 14-pin LS49 and includes full functional capability for lamp test and ripple blanking which was not available in the LS49.

The composition of all characters, except the 6 and 9 are identical between the LS247, 248, 249 and the LS47, 48 and 49. The LS47 thru 49 compose the 6 and 9 without tails, the LS247 thru 249 compose the 6 and 9 with the tails. The LS247 has active-low outputs for direct drive of indicators. The LS248 and 249 have active-high outputs for driving lamp buffers.

All types feature a lamp test input and have full ripple-blanking input/output controls. On all types an automatic leading and/or trailing-edge zero-blanking control (RBI and RBO) is incorporated and an overriding blanking input (BI) is contained which may be used to control the lamp intensity by pulsing or to inhibit the output's lamp test may be performed at any time when the BI/RBO node is at high level. Segment identification and resultant displays are shown below. Display pattern for BCD input counts above 9 are unique symbols to authenticate input conditions.

LS247

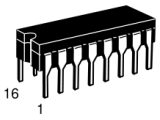
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

LS248

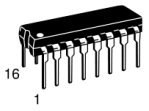
- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

LS249

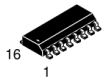
- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression



J SUFFIX
CERAMIC
CASE 620-09



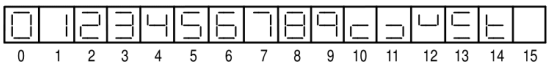
N SUFFIX
PLASTIC
CASE 648-08



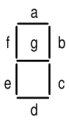
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC

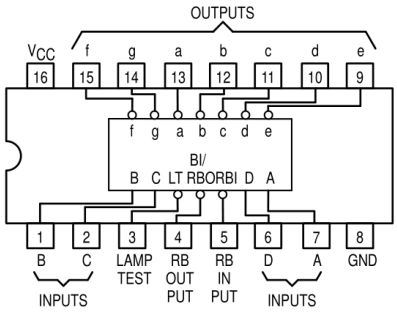


NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

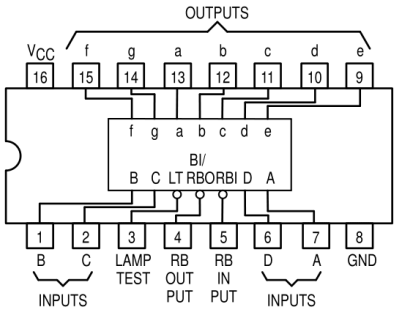


SEGMENT IDENTIFICATION

SN54/74LS247
(TOP VIEW)



SN54/74LS248
SN54/74LS259
(TOP VIEW)

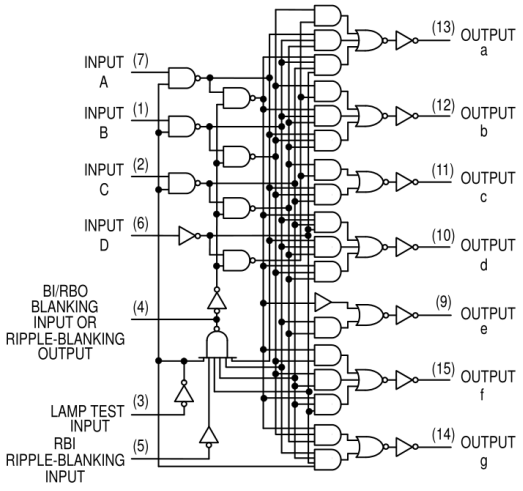


ALL CIRCUIT TYPES FEATURE LAMP INTENSITY MODULATION CAPABILITY

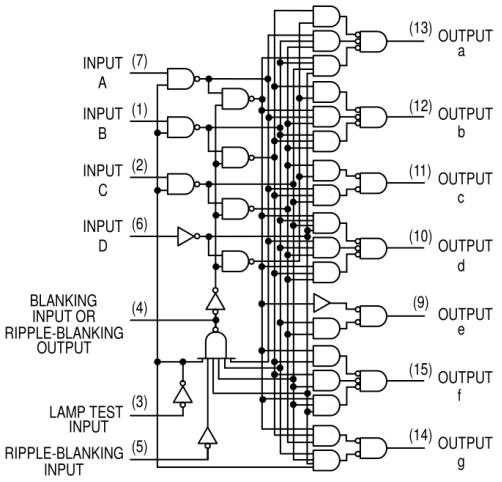
TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE	
SN54LS247	low	open-collector	12 mA	15 V	35 mW
SN54LS248	high	2.0 kΩ pull-up	2.0 mA	5.5 V	125 mW
SN54LS249	high	open-collector	4.0 mA	5.5 V	40 mW
SN74LS247	low	open-collector	24 mA	15 V	35 mW
SN74LS248	high	2.0 kΩ pull-up	6.0 mA	5.5 V	125 mW
SN74LS249	high	open-collector	8.0 mA	5.5 V	40 mW

LOGIC DIAGRAM

LS247



LS248, LS249



LS247
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	1
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

LS248, LS249
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	H	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	1
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	H	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = HIGH Level, L = LOW Level, X = Irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

† BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High BI/RBO	54, 74			−50	μA
I_{OL}	Output Current — Low BI/RBO	54 74			1.6 3.2	mA
$V_{O(off)}$	Off-State Output Voltage a−g	54, 74			15	V
$I_{O(on)}$	On-State Output Current a−g a−g	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage BI/RBO	54	2.4	4.2		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	4.2		V		
V_{OL}	Output LOW Voltage BI/RBO	54, 74		0.25	0.4	V	I_{OL} = 1.6 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 3.2 mA	
$I_{O(off)}$	Off-State Output Current a−g	54, 74			250	μA	V_{CC} = MAX, V_{IH} = 2.0 V, $V_{O(off)}$ = 15 V, V_{IL} = MAX	
$V_{O(on)}$	On-State Output Voltage a−g	54, 74		0.25	0.4	V	$I_{O(on)}$ = 12 mA	V_{CC} = MIN, V_{IH} = 2.0 V, V_{IL} per Truth Table
		74		0.35	0.5	V	$I_{O(on)}$ = 24 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Any Input, except BI/RBO				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	BI/RBO				−1.2			
I_{OS}	Short Circuit Current BI/RBO (Note 1)		−0.3		−2.0	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			7.0	13	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH} t_{PHL}	Turn-Off Time from A Input Turn-On Time from A Input			100 100	ns	C_L = 15 pF, R_L = 665 Ω
t_{PHL} t_{PLH}	Turn-Off Time from RBI Input Turn-On Time from RBI Input			100 100	ns	

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High BI/RBO	54, 74			−50	μA
	a−g	54, 74			−100	
I_{OL}	Output Current — Low BI/RBO BI/RBO	54 74			1.6 3.2	mA
	a−g a−g	54 74			2.0 6.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage a−g and BI/RBO	54	2.4	4.2		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	4.2		V		
I_{OH}	Output Current a−g	54, 74	−1.3	−2.0		mA	V_{CC} = MIN, V_O = 0.85 V, Input Conditions as for V_{OH}	
V_{OL}	Output LOW Voltage a−g	54, 74		0.25	0.4	V	I_{OL} = 2.0 mA	V_{CC} = MIN, V_{IH} = 2.0 V, V_{IL} = per Truth Table
		74		0.35	0.5		I_{OL} = 6.0 mA	
	BI/RBO	54, 74		0.25	0.4	V	I_{OL} = 1.6 mA	
		74		0.35	0.5		I_{OL} = 3.2 mA	
I_{IH}	Input HIGH Current Any Input, except BI/RBO				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Any Input, except BI/RBO				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	BI/RBO				−1.2			
I_{OS}	Short Circuit Current BI/RBO (Note 1)		−0.3		−2.0	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			25	38	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{PLH} t_{PHL}	Propagation Delay Time, High-to-Low-Level Output from A Input Propagation Delay Time, Low-to-High-Level Output from A Input			100 100	ns	C_L = 15 pF R_L = 4.0 kΩ
t_{PHL} t_{PLH}	Propagation Delay Time, High-to-Low-Level Output from RBI Input Propagation Delay Time, Low-to-High-Level Output from RBI Input			100 100	ns	C_L = 15 pF R_L = 6.0 kΩ

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High BI/RBO	54, 74			−50	μA
I_{OL}	Output Current — Low BI/RBO BI/RBO	54 74			1.6 3.2	mA
V_{OH}	Output Voltage — High a−g	54, 74			5.5	V
I_{OL}	Output Current — Low a−g a−g	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage BI/RBO	54	2.4	4.2		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	4.2		V		
I_{OH}	Output HIGH Current a−g	54, 74			250	μA	V_{CC} = MIN, V_{IH} = 2.0 V, V_{OH} = 5.5 V, V_{IL} = MAX	
V_{OL}	Output LOW Voltage BI/RBO	54, 74		0.25	0.4	V	I_{OL} = 1.6 mA	V_{CC} = MIN, V_{IH} = 2.0 V, V_{IL} = per Truth Table
		74		0.35	0.5		I_{OL} = 3.2 mA	
	a−g	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	
		74		0.35	0.5		I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Any Input, except BI/RBO				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Any Input, except BI/RBO				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	BI/RBO				−1.2			
I_{OS}	Short Circuit Current BI/RBO (Note 1)		−0.3		−2.0	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			8.0	15	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PHL} t_{PLH}	Propagation Delay Time, High-to-Low-Level Output from A Input Propagation Delay Time, Low-to-High-Level Output from A Input			100 100	ns	C_L = 15 pF, R_L = 2.0 Ω
t_{PHL} t_{PLH}	Propagation Delay Time, High-to-Low-Level Output from RBI Input Propagation Delay Time, Low-to-High-Level Output from RBI Input			100 100	ns	C_L = 15 pF, R_L = 6.0 Ω

5
NOTES On Project

- The project is a really straightforward application of the concept of counters, where the only challenge is perhaps to solder the PCB with accuracy, as, given my workshop skills, nine out of ten of my PCBs result in damage.
- One more thing, as the BCD Decoder IC is IC 74248, the input fed to the 7-segment display should be "*Common Anode"* as the IC is *"Active High"*.

7.7.1 IC 7490 (Decade Binary Counter)

IC 7490 is a decade binary counter. It consists of four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide by five.

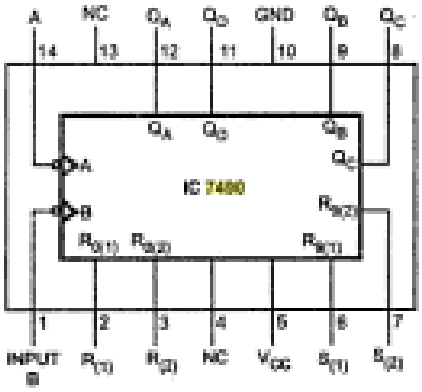


Fig. 7.48 Connection diagram for 7490

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

1. BCD Decade (8421) Counter :

The B input must be externally connected to the Q_A output and A input receives the incoming count and a BCD count sequence is produced.

2. Symmetrical Bi-quinary Divide-by-Ten Counter :

The Q_D output must be externally connected to the A input. The input count is then applied to the B input and a divide-by-ten square wave is obtained at output Q_A.

3. Divide-by-Two and Divide-by-Five Counter :

No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (A as the input and Q_A as the output). The B input is used to obtain binary divide-by-five operation at the Q_D output.

Table 7.8 shows function tables and Fig. 7.49 shows logic diagram for IC7490.

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Table 7.8 (a) BCD count sequences (Note 1)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Table 7.8 (b) BCD Bi-quinary (5-2) (Note 2)

Example 7.22 : *Design a divide-by-96 counter using 7490 ICs.*

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide by 100 counter. To get a divide-by-96 counter, the counter is reset as soon as it becomes 1001 0110. The diagram is shown in Fig. 7.52.

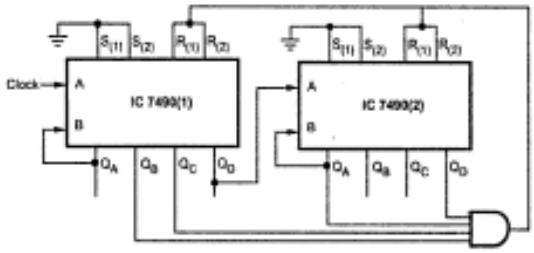


Fig. 7.52 Divide-by-96 counter

Example 7.23 : *Design divide-by-93 counter using the same IC.*

Solution : IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide-by-100 counter. To get a divide-by-93 counter, the counter is reset as soon as it becomes 1001 0011. The diagram is shown in the Fig. 7.53.

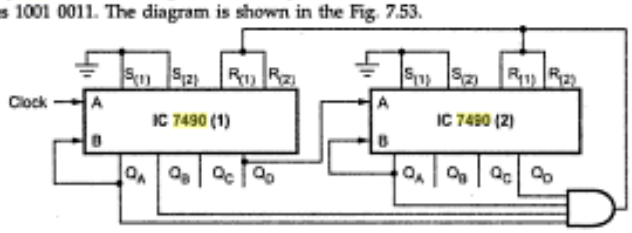


Fig. 7.53 Divide-by-93 counter

- As is seen from the above examples, a MOD Counter is RESET only when it reaches the respective MOD value, which in my case is $(\mathbf{100})_{\mathbf{10}} = (\mathbf{1010\ 1010})_{\boldsymbol{BCD}}$ but since the counters used are "decade counters", the values need not be reset as the counters are reset at every 10×10 cycle. So, I have grounded all the RESET terminals, viz, $\boldsymbol{R_{01}, R_{02}, R_{91}, R_{92}}$.
- However, a better way to make the modulo counter is to keep arbitrary pin connections to $\boldsymbol{Q_A, Q_B, Q_C, Q_D}$ of both the 7490 ICs. This will enable us to make a counter of desirable modulo with the same circuitry. (Obviously, MOD values lie within the range of 0-100)
- So, a manual or automatic switching of the pin connection enables us to make a seconds' clock (MOD 60) and other suitable applications whose upper limit of measurement lies in this range

BIBLIOGRAPHY

- The textual material for this report has been reprinted from :

  http://www.wikipedia.org

  http://www.electronics-tutorials.ws/counter

- IC Datasheets have been taken up from the following :

  Fairchild Semiconductor
  http://www.fairchildsemi.com

  Motorala Semiconductor
  http://www.motorola.com