1.DESIGN AND ANALYSIS OF BJT COMMON EMITTER AMPLIFIER CONFIGURATION

1.1 OBJECTIVE

1. To design a single stage CE amplifier Circuit for the given specifications.
2. To perform the transient analysis and determine the phase difference between input and output signals.
3. To measure the voltage gain of the amplifier over a range of frequencies and plot the frequency response curve.
4. To determine the values of lower and upper 3-dB frequencies and 3-dB bandwidth.

1.2 HARDWARE REQUIRED

a.	Power supply	:	Variable regulated low voltage DC source(0-30V, 0-2A)
b.	Equipments	:	AFO(0.3Hz-3MHz), CRO(0-30MHz)
c.	Resistors	:	To be calculated.
d.	Capacitors	:	To be calculated.
e.	Semiconductors	:	BC 107 (or equivalent)
f.	Miscellaneous	:	Breadboard and wires.

1.3 THEORY

Amplifier is an electronic circuit that is used to raise the strength of a weak signal. The process of raising the strength of a weak signal is known as amplification. One importance requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. The transistor is used for amplification. When a transistor is used as an amplifier, the first step is to choose a proper configuration in which device is to be used. Then the transistor is biased to get the desired *Q-point*. The signal is applied to the amplifier input and gain is achieved.

1.3.1 CE amplifier operation

Consider a CE amplifier circuit as shown in fig. 1-1

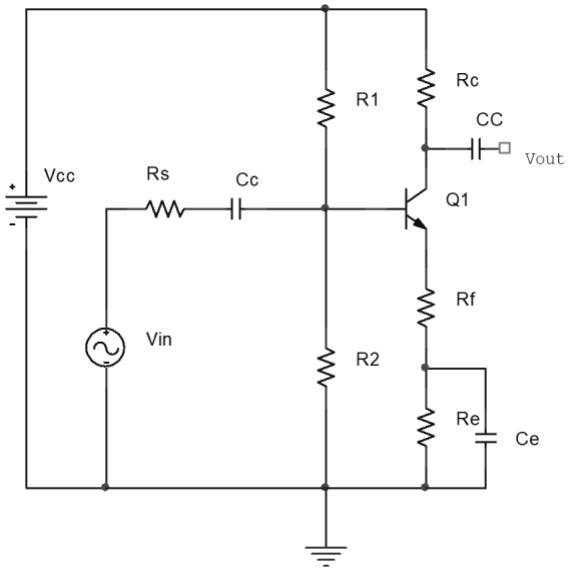


Fig 1.1 CE Amplifier

When the capacitors are regarded as ac short circuits, it is seen that the circuit input terminals are the transistor base and emitter, and the output terminals are the collector and the emitter. So, the emitter terminal is common to both input and output, and the circuit configuration is termed *Common –Emitter (CE).*

1.3.2 Transient Analysis

Transient analysis is nothing but taking voltages and current at different instants.It is seen that there is a 180^o phase shift between the input and output waveforms (Figure 2.4(a&b)). This can be understood by considering the effect of a positive going input signal. When V_S increases in a positive direction, it increases the transistor V_{BE}. The increase in V_{BE} raises the level of I_C, thereby increasing the drop across Rc, and thus reducing the level of the V_C. The changing level of V_C is capacitor-coupled to the circuit output to produce the ac output voltage, V_O. As V_S increases in a positive direction, V_O goes in a negative direction. Similarly, When V_S changes in a negative direction, the resultant decrease in V_{BE} reduces the I_C level, thereby reducing V_{RC}, and producing a positive going output.

1.3.3 CE amplifier circuit elements and their functions

(i) ***Biasing circuit:*** The resistances R_1, R_2 and R_E form the biasing and stabilization circuit. The biasing circuit must establish a proper operating point, otherwise a part of the negative half-cycle of the signal may be cut-off in the output.

(ii) ***Input capacitor, C_1*****:** An electrolyte capacitor C_1 is used to couple the signal to the base of the transistor. If it is not used, the signal source resistance, R_s will come across R_2 and thus change the bias. C_1 allows only ac signal to flow but isolates the signal source from R_2.

(iii) ***Emitter bypass capacitor, C_e***: An Emitter bypass capacitor, C_e is used parallel with R_E to provide low reactance path to the amplified ac signal. If it is not used, then amplified ac signal flowing through R_E will cause a voltage drop across it, thereby reducing the output voltage.

(iv) ***Coupling capacitor, C_c***: The coupling capacitor, C_c couples one stage of amplification to the next stage. If it is not used, the bias conditions of the next stage will be drastically changed due to the shunting effect of R_C. This is because R_C will come in parallel with the upper resistance R_1 of the biasing network of the next stage, thereby altering the biasing conditions of the latter. In short, the coupling capacitor C_2 isolates the dc of one stage from the next stage, but allows the passage of ac signal.

1.3.4 CE amplifier circuit currents

(i) Base current

$i_B = I_B + i_b$

Where I_B = dc base current when no signal is applied

i_b = ac base when ac signal is applied

and i_B = total base current

(ii) Collector current

$i_C = I_C + i_c$

Where I_C = zero signal collector current

i_c = ac collector current when ac signal is applied

and i_C = total collector current

(iii) Emitter Current

$i_E = I_E + ie$

Where I_E = Zero signal emitter current

Ie = ac emitter current when ac signal is applied

and i_E = total emitter current

It is useful to keep in mind that

$I_E = I_B + I_C$

and $i_e = i_b + i_c$

Also, $I_E \approx I_C$ and $i_e \approx i_c$

1.3.5 CE amplifier frequency response

The voltage gain of an amplifier varies with signal frequency. It is because reactance's of the capacitors in the circuit changes with signal frequency and hence affects the output voltage. The curve between voltage gain and signal frequency of an amplifier is known a *frequency response*. Figure 1.5

It is clear that the voltage gain drops off at low ($< f_L$) and high ($> f_H$) frequencies whereas it is uniform over mid-frequency range (f_L to f_H).

(i) ***At low frequencies ($< f_L$),*** the reactance of coupling capacitor is quite high and hence very small part of signal will pass from amplifier stage to the load. Moreover, C_E cannot shunt the R_E effectively because of its large reactance at low frequencies. These two factors cause a falling of voltage gain at low frequencies.

(ii) ***At high frequencies ($> f_H$),*** the reactance of C_c is very small and it behaves as a short circuit. This increases the loading effect of amplifier stage and serves to reduce the voltage gain. Moreover, at high frequency, capacitive reactance of base-emitters junction is low which increases the base current. These reduce the current amplification factor β. Due to these two reasons, the voltage gain drops off at high frequency.

(iii) ***At mid frequencies (f_L to f_H),*** the voltage gain of the amplifier is constant. The effect of coupling capacitor Cc in this frequency range is such as to maintain a uniform voltage gain. Thus, as the frequency increases in this range, reactance of C_C decreases which tend to increase the gain.

1.3.6 CE amplifier analysis

The first step in AC analysis of CE amplifier circuit is to draw ac equivalent circuit by reducing all dc sources to zero and shorting all the capacitors. Fig 1.2 shows the ac equivalent circuit.

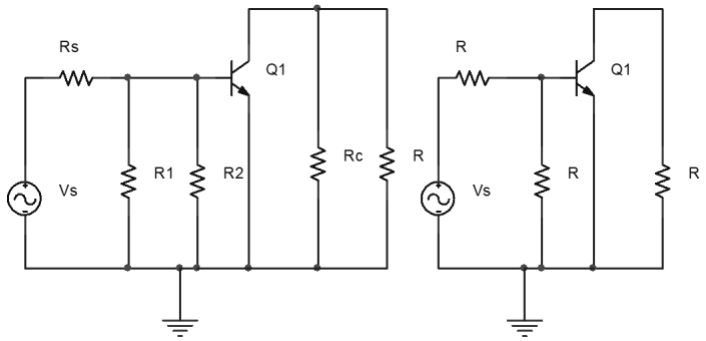


Fig 1.2: Equivalent Circuit of CE

The next step in the ac analysis is to draw h-parameter circuit by replacing the transistor in the ac equivalent circuit with its h-parameter model. Fig. 1.3 shows the h-parameter equivalent circuit for CE circuit.

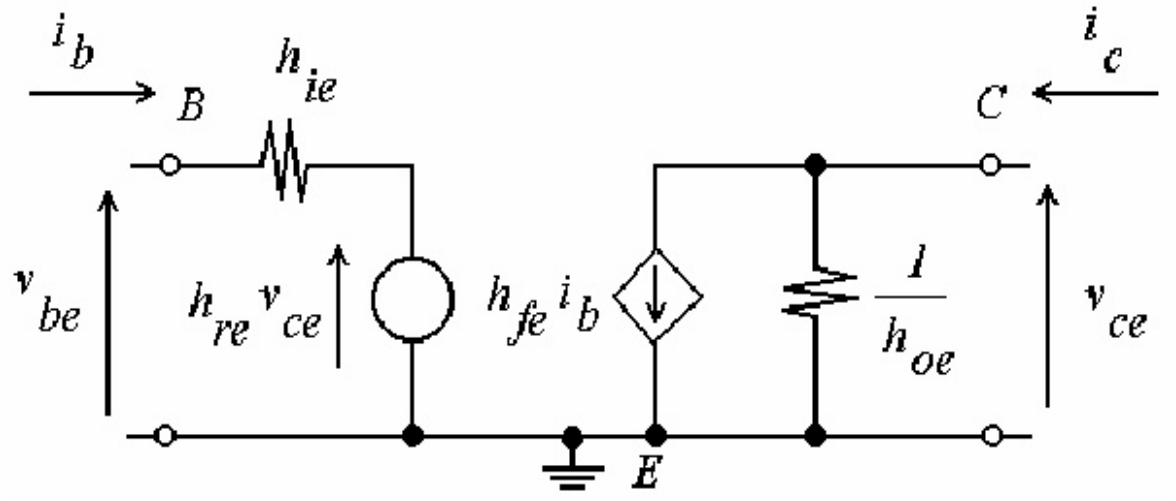


Fig 1.3: h- Parameter Equivalent Circuit

The typical CE circuit performance is summarized below:

Device input impedance, $Z_b = h_{ie}$

Circuit input impedance, $Z_i = R_1 || R_2 || Z_b$

Device output impedance, $Z_C = \frac{1}{h_{oe}}$

Circuit output impedance, $Z_O = R_C \| Z_C \approx R_C$

Circuit voltage gain, $A_V = -\frac{h_{fe}}{h_{ie}}(R_C \| R_L)$

Circuit current gain, $A_i = \frac{h_{fe} R_C R_B}{(R_C + R_L)(R_C + h_{ie})}$

Circuit power gain, $A_P = A_V \times A_i$

1.4 MODEL GRAPH

1.4.1 Transient Analysis

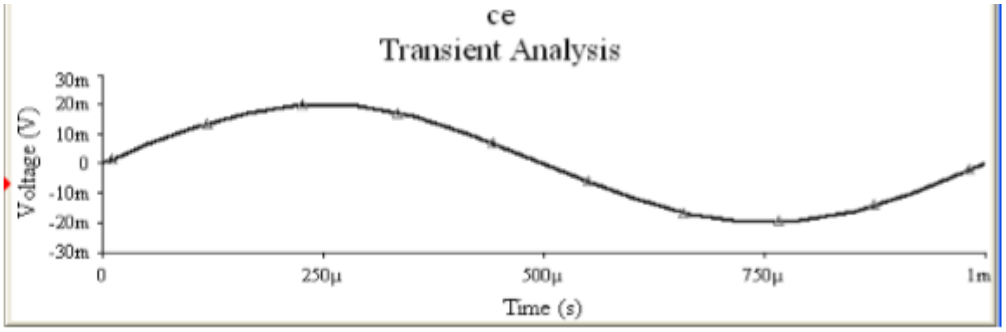


Fig 1.4(a) Input Voltage Waveform

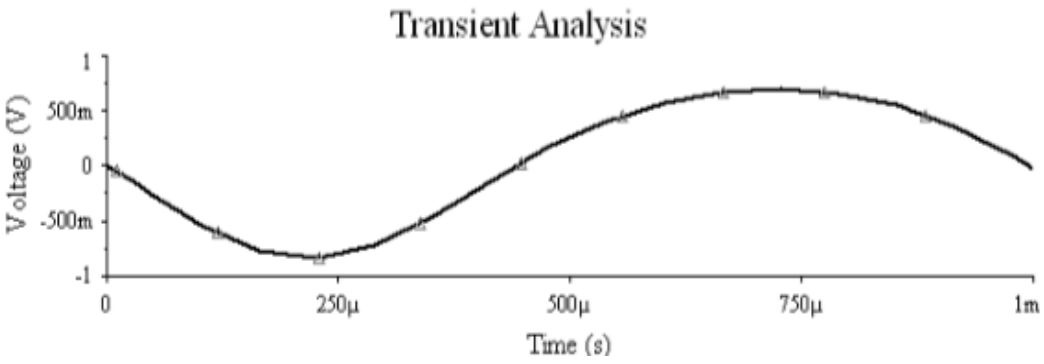


Fig 1.4(b) Output Voltage Waveform

1.4.2 Frequency Response

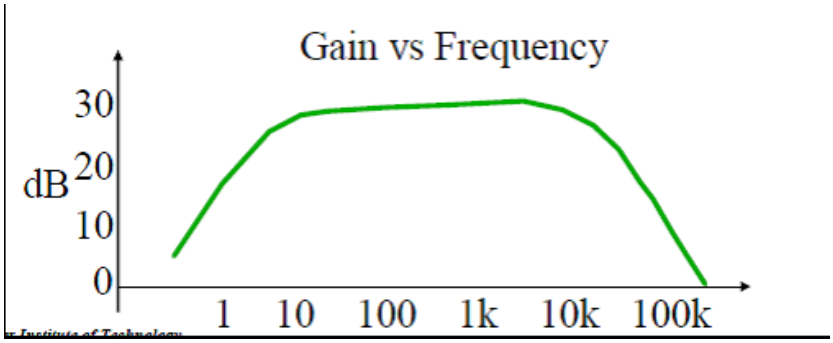


Fig 1.5 Frequency Response

1.5 CE AMPLIFIER CIRCUIT DESIGN

Design of CE circuit normally commences with a specification of supply voltage, minimum voltage gain, frequency response, signal source impedance load impedance, stability factor and the Q-point.

Selection of I_C, R_C and R_E

$$A_V = -\frac{h_{fe}}{h_{ie}}(R_C \| R_L)$$

- For satisfactory transistor operation, Ic should not be less than 500µA. A good minimum Ic to aim for is 1mA.
- The V_{CE} should typically be around 3v to ensure that the transistor operates linearly and to allow a collector voltage swing of ±1v which is usually adequate for small-signal amplifier
  - ***Note:*** R_C should normally be very much larger than R_L, so that R_L has little effect on voltage gain.
- Select V_E = 5v for good bias stability in most circumstances.
  - ***Note:*** When $V_E >> V_{BE}$, V_E will be only slightly affected by any variation in V_{BE} (due to temperature change or other effects)
- Once V_E, V_{CE} and Ic are selected, V_{RC} is determined as $V_{RC} = V_{CC} - V_{CE} - V_E$

  Then, R_C and R_E are calculated as $R_C = \frac{V_{RC}}{I_C}$ and $R_E = \frac{V_E}{I_C}$

Selection of bias resistors

As discussed in lab-1, experiment-1.1, section-1.1, selection of voltage divider current (I_2) as $I_C/10$ gives good bias stability and reasonably high input resistance. The bias resistors are calculated as

$$R_2 = \frac{V_B}{I_2} \text{ and } R_1 = \frac{V_{CC} - V_B}{I_2}$$

Selecting $R_2 = 10R_E$ gives $I_2 = I_C/10$ the precise level of I_2 can be calculated as $I_2 = V_B/R_2$ and this can be used in the equation for R_1.

Selection of bypass capacitor, CE

Basically the capacitor values are calculated at the lowest signal frequency that the circuit is required to amplify. This frequency is the *lower cut-off frequency, f_L.*

Choose $X_{CE} = \frac{h_{ie}}{1+h_{fe}}$ at f_L for C_E calculation to give the smallest value for the bypass capacitor.

Selection of coupling capacitors, C_1 and C_2

The coupling capacitors C_1 and C_2 should have a negligible effect on the frequency response of the circuit. To minimize the effects of C_1 and C_2, the reactance of each coupling capacitor is selected to be approximately equal to one-tenth of the impedance in series with it at the lowest operating frequency of the circuit (f_L).

$$X_{C1} = \frac{Z_i + r_s}{10}$$

$$X_{C3} = \frac{Z_O + R_L}{10}$$

Usually, $R_L >> Z_O$ and often $Z_i >> r_S$, so that Z_O and r_S can be omitted in the above equations.

1.6 DESIGN PROBLEM

(i) Design a single stage CE transistor amplifier using BC107 transistor with Vcc = 15V, V_{CEQ} = 5V, V_E = 3V, R_L = 47KΩ and f_L = 100Hz.

(ii) Determine Z_i, Z_O, A_V, A_i and A_P for the CE circuit designed in problem (i).

Procedure

Given V_{CC} = 15V, V_{CE} = 5V, V_E = 3V, R_L = 47kΩ and f_L = 100Hz.

The data sheet of BC107 transistor shows:

h_{ie} = 3kΩ and h_{FE}=190

Selection of R_C

$R_C << R_L$ so that R_L will have little effect on the circuit voltage gain.

Select $R_C = \frac{R_L}{10} = \frac{47K}{10} = 4.7K\Omega$ (Standard value)

Selection of R_E

$$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C}$$

Where $I_C = \frac{V_{RC}}{R_C} = \frac{V_{CC} - V_{CE} - V_E}{R_C} = \frac{(15-5-3)V}{4.7K} = 1.4mA$

$\therefore R_E = \frac{3V}{1.4mA} = 2.14K\Omega$ (use a standard 2.2 kΩ)

Selection of R_1 and R_2

Selection of voltage divider current I_2 as $I_C/10$ gives good bias stability and reasonably high input resistance

Selecting $R_2 = 10\ R_E$ gives $I_2 = I_C/10$

i.e., $R_2 = 10 \times 2K\Omega = 22K\Omega$ (standard value)

and $I_2 = \frac{I_C}{10} = \frac{1.4mA}{10} = 140\mu A$

$\therefore R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{15 - (V_{BE} + V_E)}{140\mu 4} = \frac{15 - (0.7+5)}{140\mu 4} = 66.43K\Omega$ (use standard 68kΩ)

Selection of C_1 and C_2

The coupling capacitors C_1 and C_2 should have negligible effect on the frequency response of the circuit. So, the reactance of each coupling capacitor is selected to be approximately equal to $1/10^{th}$ of the impedance in series with it at the lowest operating frequency for the circuit.

$$X_{C1} \approx \frac{Z_i}{10} = \frac{R_1 \| R_2 \| h_{ie}}{10} = \frac{68K \| 22K \| 3K}{10} = 254\Omega \qquad \therefore$$

$$C_1 = \frac{1}{2\pi\pi_L X_{C1}} = \frac{1}{2 \times \pi \times 100 \times 254} = 6\mu F$$

(Standard value 10μF)

$$X_{C2} \approx \frac{R_L}{10} = \frac{47K}{10} = 4.7K\Omega \therefore \qquad C_2 = \frac{1}{2\pi\pi_L X_{C2}} = \frac{1}{2 \times \pi \times 100 \times 4.7K} = 0.34\mu F$$

(use a standard 0.47μf)

C_1 = $C_C$in Input Side

C_2 = C_C in Output Side

Selection of C_E

$$X_{CE} = \frac{h_{ie}}{1 + h_{fe}} = \frac{3K\Omega}{1 + 190} = 15.71$$

$$\therefore \qquad C_E = \frac{1}{2\pi\pi_L X_{CE}} = \frac{1}{2 \times \pi \times 100 \times 15.71} = 101.36\mu F$$ (use a standard 100μf)

Neglect source resistance R_S and feedback resistor R_f

Calculation of Z_i, Z_O, A_V, A_i and A_P

Input impedance, $Z_i = R_1 || R_2 || h_{ie}$ = 68k||22k||3K

= 2.54KΩ

Output impedance, $Z_O = R_C$ = 4.7kΩ

Voltage gain, $$A_V = -\frac{h_{fe}}{h_{ie}}(R_C \| R_L) = -\frac{190}{3K}(4.7K \| 47K) = 270.61$$

Current gain, $$A_i = \frac{h_{fe} R_C R_B}{(R_C + R_L)(R_C + h_{ie})} = \frac{190 \times 4.7K \times (68K \| 22K)}{(4.7K + 47K)(4.7K + 3K)} = 37.23$$

Power gain, $A_P = A_V$ x A_i = 270.61 X 37.23 = 10K

1.6.1 Design Constraints

If $I_C > V_{CC}/2(R_E+R_C)$ and $V_{CE} < V_{CC}/2$ is not satisfied, then thermal runaway will occur.

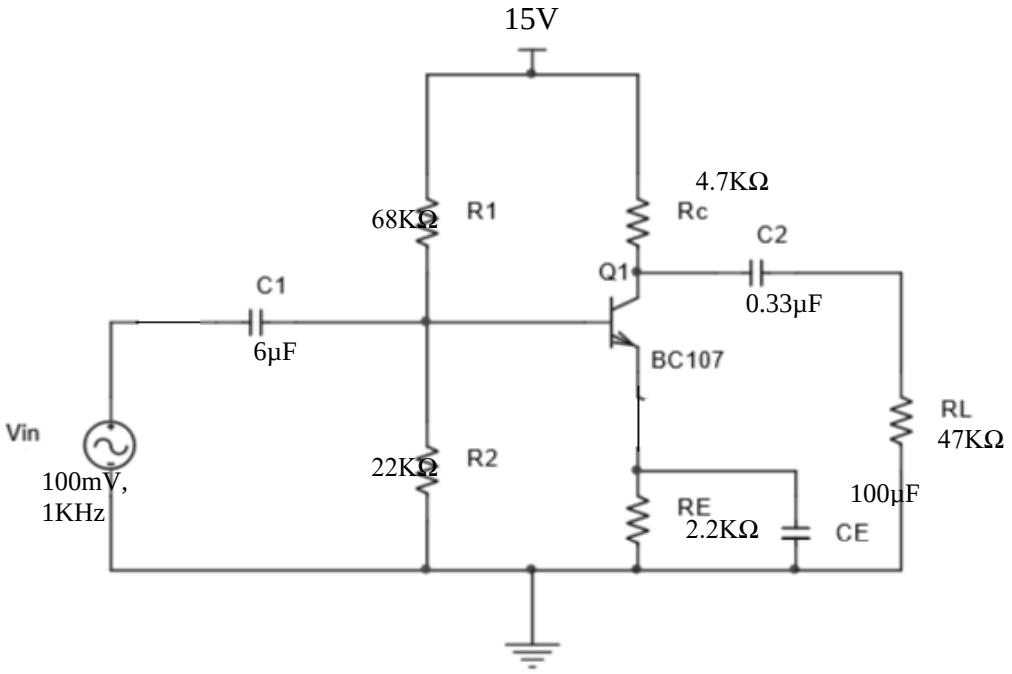


Fig 1.6 Designed Circuit for CE

1.7 PROCEDURE

Transient and Frequency response curve measurements

a. Feed 100mV (peak-to-peak) sinusoidal signal at 1KHz frequency as the input signal (Vs) to the CE circuit.

b. Observe the input and output voltages simultaneously on a CRO. Note down the amplitude, frequency and phase difference between the two voltages in the table.

c. In the above assembled circuit, keep the magnitude of the source same, ie., 100mv and vary the frequency from 50 Hz to 10 MHz and measure the voltage gain of the amplifier at each frequency across R_L. Take atleast 10 readings and tabulate the reading in Table. Plot on a semi log graph sheet the frequency response (voltage gain Vs frequency) curve using the above measurements.

d. From the plot, determine the values of (a) Mid band voltage gain, Av(mid), (b) Lower Cut-off frequency,(c) upper cut-off frequency and (d) Bandwidth.

1.8 TABULATION

Transient Analysis

	Amplitude	Frequency	Phase difference
Input signal	50 mV	1kHz	
Output signal			

(a)

Frequency Response **Vi = 50mV**

Frequency (Hz)	Output Voltage (Vo) (V)	Gain (Av)	Gain in db Av = 20 log(Vo/Vi)
20			
30			

(b)

1.9 PRELAB QUESTIONS

1. Define Biasing.
2. Identify the type of biasing circuit used in the amplifier and justify its selection over other biasing circuits.
3. How the bypass and coupling capacitances affect the low frequency response of the amplifier?
4. What are the different h-parameters of CE amplifier.
5. What are the main applications of CE amplifier.

1.10 POSTLAB QUESTIONS

1. How do coupling capacitors C_1 and C_2 affect the frequency response? Why?
2. What is the effect on the amplifier performance of omitting R_E?
3. What is the effect on input impedance of removing bypass capacitor C_E?
4. (a) What is the phase relationship between the input and output signals of a C_E amplifier? (b) Was this relationship confirmed by the results of your experiments? Explain how.
5. Is the output impedance of a Common emitter amplifier a fixed quantity? Confirm your answer by referring specifically to any substantiating data in this experiment.
6. From a measurement of the rise time of the output pulse of an amplifier, whose input is a small amplitude square wave, one can estimate the _____ parameter of the amplifier.
7. What is the effect found when $V_{CE}>V_{CC}/2$?

1.11 RESULT

a. The phase difference between the input and output voltage waveform is _____

b. The Mid-band voltage gain =

c. The Lower cutoff frequency =

d. The Upper cutoff frequency =

e. Bandwidth =

2. PSPICE SIMULATION OF MOSFET AMPLIFIER CONFIGURATIONS

2.1 OBJECTIVE

1. To design and implement a common source MOSFET Amplifier to
   a. measure DC currents and voltages developed in the circuits.
   b. plot the transient signal voltage of the input and output of the circuit and measure the voltage gain.
   c. plot the frequency response of the circuit and measure the bandwidth.
2. To modify the CS amplifier circuit for current-series feedback and measure the given parameters.
3. To modify the CS amplifier circuit for voltage-series feedback and measure the given parameters.

2.2 SOFTWARE REQUIRED

PSPICE – OrCAD 9.2 lite

2.3 BACKGROUND

SPICE is software that simulates electronic circuits. SPICE can perform various analyses such as DC analysis, Transient analysis, AC analysis and operating point measurements. SPICE contains model for common circuit elements active as well as passive and it is possible of simulating most electronic circuits. The abbreviation of SPICE is **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

2.4 THEORY

A common-source amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law. However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent

voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics.

2.5 CIRCUIT DIAGRAM

COMMON SOURCE AMPLIFIER :-

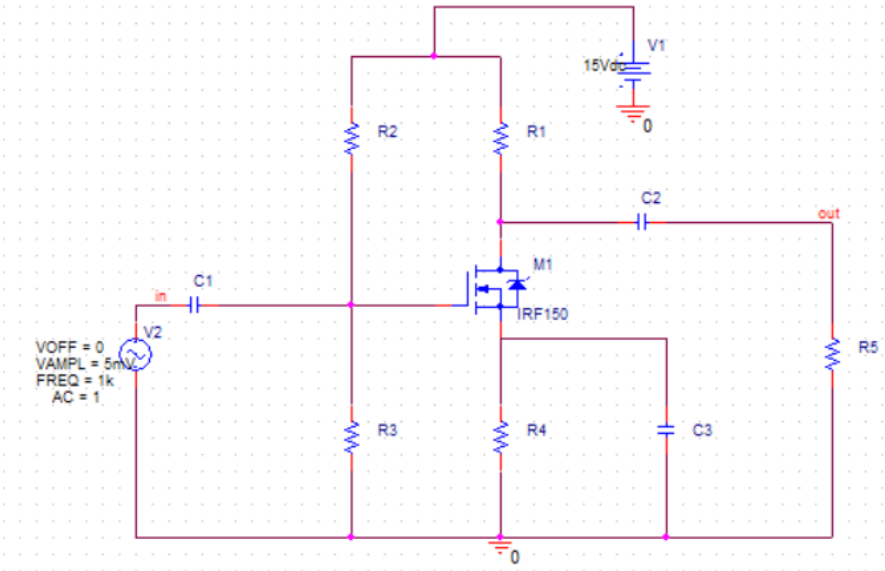


Fig 2.1 Schematic Diagram of Common Source Amplifier using PSPICE

DESIGN SPECIFICATIONS :-

V_{DD}=15V , V_{TH}=1V , K_n=6.5mA/V^2 , I_{DMAX}=1mA , f_l=100k Hz , g_m=Y_{fs}=10ms

DESIGN PROCEDURE :-

Let V_{ds}= $\frac{VDD}{3} = \frac{15V}{3}$ = 5V R_L>>R_D

and I_d= $\frac{ID(\max)}{3} = \frac{1mA}{3}$ = 0.333mA Let R_L=10R_D=150k

Using KVL around drain-source loop,

$R_D+R_s=\frac{Vdd-Vds}{Id} = \frac{15-5}{0.33m}$ = 30k

If R_D =R_s , then R_D=R_s= 15k .

The drain current expression for the MOSFET operating in the saturation region is given by

$I_D= K_n(V_{gs}-V_{th})^2$

from which , $V_{GS} = \sqrt{\frac{Id}{Kn}} +1 = \sqrt{\frac{0.33m}{6.5m}} +1$ = 1.23V

Using KVL around the gate-source loop ,

$V_G=V_{GS}+I_DR_S = 1.23 + (0.33m \text{ X } 15k) = 6.2V$

Also, V_G can be expressed by voltage divider rule as

$V_G=V_{DD}X\frac{R2}{R1+R2}$

from which $\frac{R1}{R2}=\frac{Vdd}{Vg}-1 = \frac{15V}{6.2V} -1 =1.42$ V

Let R2=1M

∴ R1= R2 X 1.42 = 1.42M

CALCULATION OF C_1, C_2 AND C_S :-

Let $X_{c1} = \frac{Zi+Rs}{10}$ at $f_L= \frac{R1\ ||R2+0}{10}$=58.68k

So, $C_1=\frac{1}{2\Pi flXc1}$=0.03uF

Let $X_{c2} = \frac{Zo+Rl}{10}$ at $f_L= \frac{Rd+Rl}{10}= \frac{15k+150k}{10}$ = 16.5k

So, $C_1=\frac{1}{2\Pi flXc2}$=0.1uF

Let $X_{cs} = \frac{1}{Yfs}$ at $f_L=\frac{1}{10ms}$= 100

So, $C_s=\frac{1}{2\Pi flXcs}$ = 16uF

CS MOSFET AMPLIFIER WITH CURRENT-SERIES FEEDBACK :-

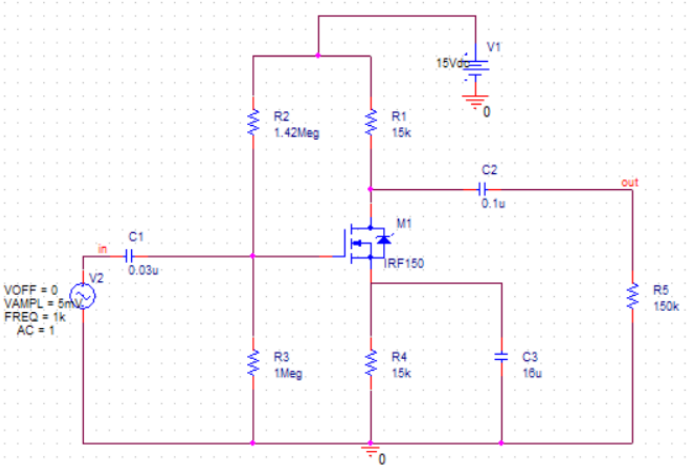


Fig 2.2 Schematic Diagram of CS Amplifier with current series feedback

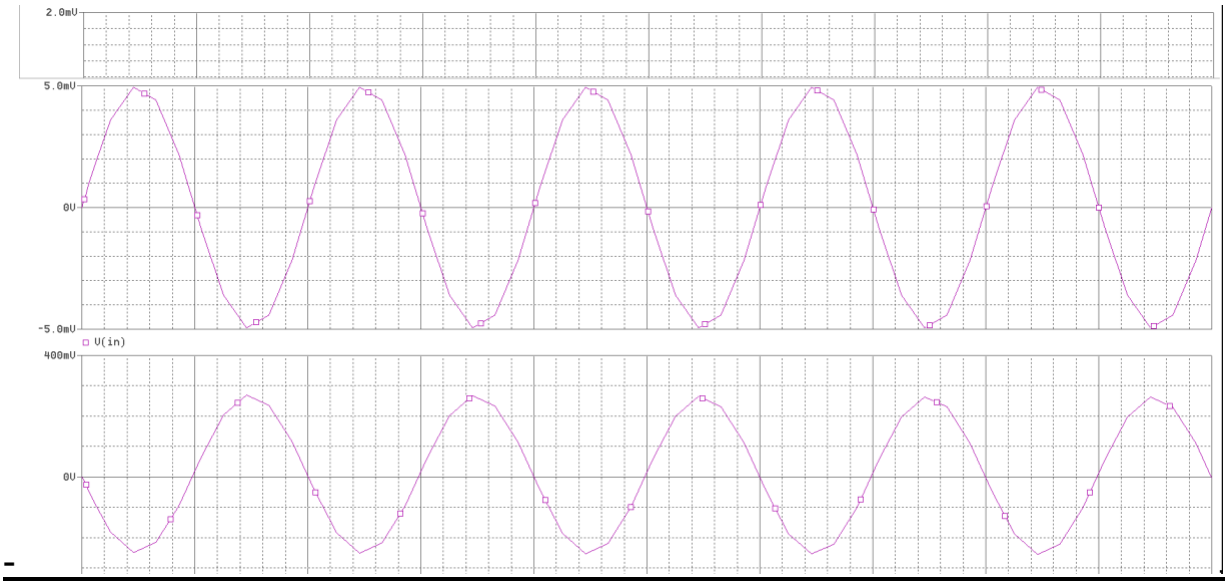


Fig 2.3 Input and Output Voltages of current series feedback MOSFET Amplifier

CS MOSFET AMPLIFIER WITH VOLTAGE-SERIES FEEDBACK :-

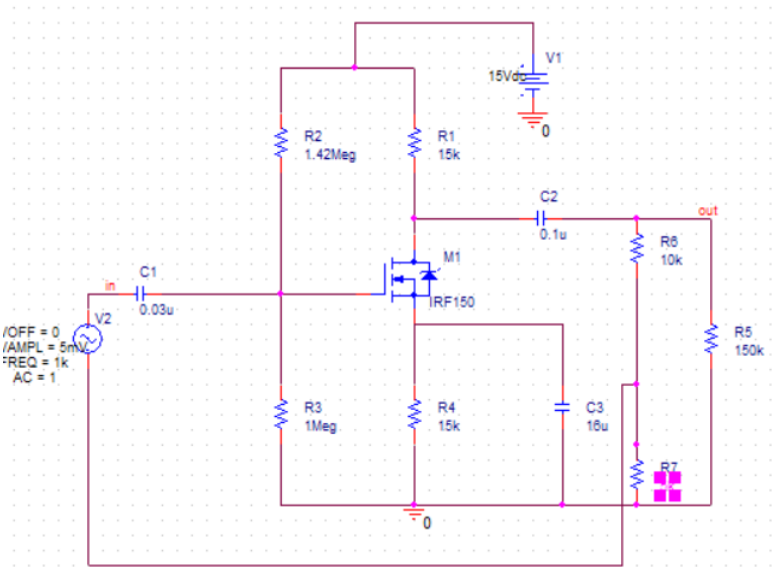


Fig 2.4 Schematic Diagram of CS MOSFET Amplifier with voltage series feedback

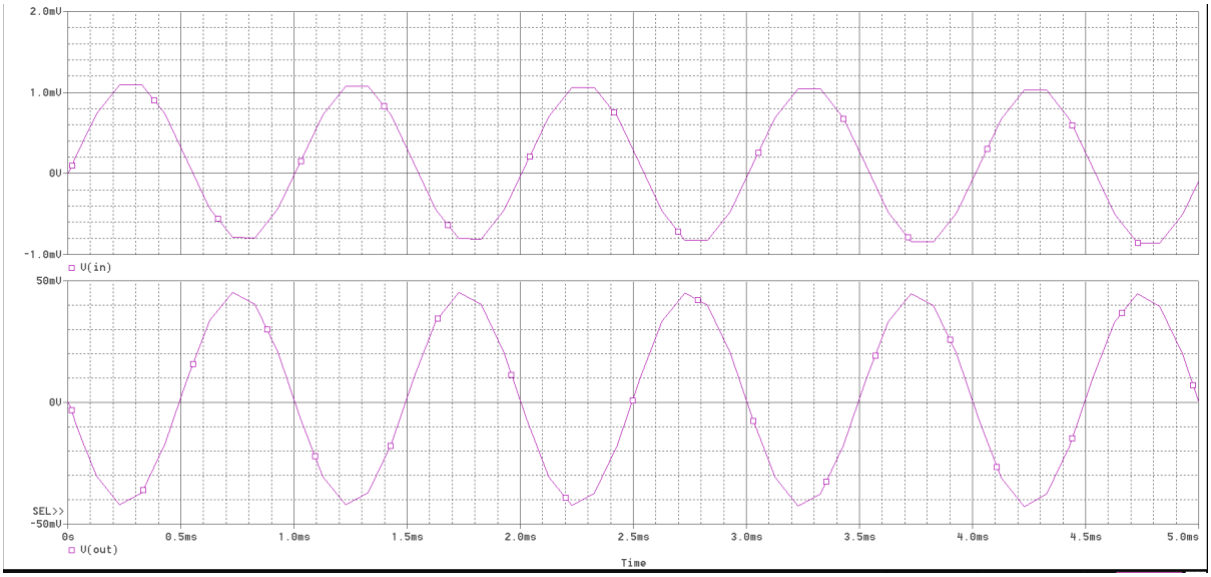


Fig 2.5 Input and Output Voltages of Voltage series feedback MOSFET Amplifier

2.6 PROCEDURE

1. Open Capture Lite Edition.
2. Go to the File menu and select New Project. Select Analog or Mixed A/D
3. Create a blank project and then click OK.
4. Select ‘Place’ option from tool bar. Pick and place all the required circuit components by just clicking on the elements.
5. Connect the components as per circuit diagram using ‘place wire’ button that is available in tool bar.
6. Click on each components to give the parameter values as per design.Save the schematic.
7. Create a new simulation profile. Mention the type of analysis and simulate the circuit.
8. Measure the voltages and currents at different points and tabulate the readings.

2.7 TABULATION

CS MOSFET AMPLIFIER WITH CURRENT-SERIES FEEDBACK :-

Transient Analysis

	Amplitude	Frequency	Phase difference
Input signal			
Output signal			

(a)

Frequency Response **Vi = 100mV**

Frequency	Output Voltage (Vo)	Gain	Gain in db Av = 20 log(Vo/Vi)

(b)

CS MOSFET AMPLIFIER WITH VOLTAGE-SERIES FEEDBACK :-

Transient Analysis

	Amplitude	Frequency	Phase difference
Input signal			
Output signal			

(c)

Frequency Response **Vi = 100mV**

Frequency	Output Voltage (Vo)	Gain	Gain in db Av = 20 log(Vo/Vi)

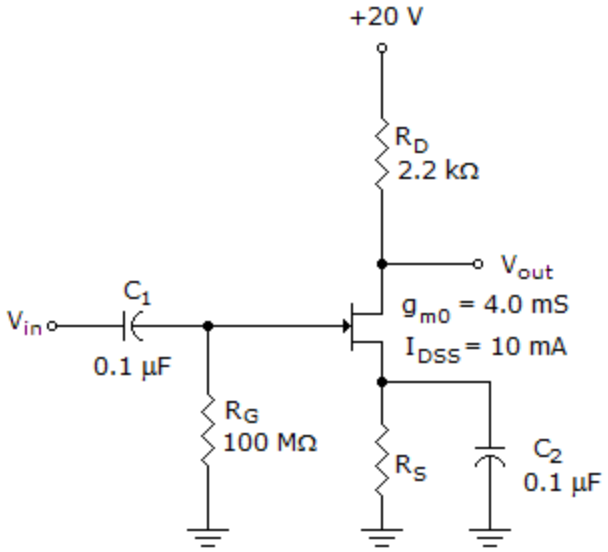
(d)

2.8 PRE LAB QUESTIONS

1. What is the maximum allowed gate current? What happens if this current is exceeded?
2. What is the impedance of FET?
3. A common-source amplifier is similar in configuration to which BJT amplifier?
4. What is (are) the function(s) of the coupling capacitors in an FET circuit?

2.9 POST LAB QUESTIONS

1. What are the advantages of FET?
2. Why the common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier**?**
3. Refer to this figure. Find the value of V_D.



4. Calculate g_m for a JFET having I_{DSS} = 10 mA, V_P = –5 V, and V_{GSQ} = –2.5 V.

2.10 RESULT:

1. The current series and voltage series feedback amplifier were designed, simulated and its frequency response was plotted.
2. The following parameters were observed.

CS MOSFET Amplifier		**Mid Band Voltage Gain**	**Bandwidth**
Current Series Amplifier	**With Feedback**		
	Without Feedback		
Voltage Series Amplifier	**With Feedback**		
	Without Feedback		

3. DESIGN AND ANALYSIS OF MULTISTAGE AMPLIFIER CONFIGURATIONS

3.1 OBJECTIVE

a) To design a Cascode Amplifier Circuit for the given specifications.
b) To perform the transient analysis and determine the phase difference between input and output signals.
c) To measure the voltage gain of the amplifier over a range of frequencies and plot the frequency response curve.
d) To determine the values of lower and upper 3-dB frequencies and 3-dB bandwidth.

3.2 HARDWARE REQUIRED

a)	Power supply	:	Variable regulated low voltage DC source(0-30V, 0- 2A)
b)	Equipments	:	AFO(0.3Hz-3MHz), CRO(0-30MHz)
c)	Resistors	:	To be calculated.
d)	Capacitors	:	To be calculated.
e)	Semiconductors	:	BC 107 (or equivalent)
f)	Miscellaneous	:	Breadboard and wires.

3.3 THEORY

A two transistor amplifier used to obtain simultaneously:

a) Reasonably high input impedance Low output impedance.
b) Reasonable voltage gain.
c) Wide bandwidth.

None of the conventional single transistor designs will meet all of the criteria above. The **cascode** amplifier will meet all of these criteria. The **cascode** is a two-stage amplifier that consists of a common emitter stage feeding into a common base stage. While the C-B (common-base) amplifier is known for wider bandwidth than the C-E

(common-emitter) configuration, the low input impedance of CB is a limitation for many applications. The solution is to precede the CB stage by a low gain CE stage which has moderately high input impedance. The stages are in a cascode configuration, stacked in series, as opposed to cascaded for a standard amplifier chain.

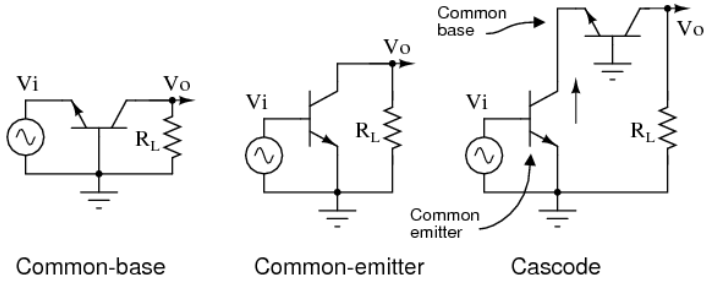


Fig 3. 1 : Equivalent circuit CE CB cascode amplifier

3.3.1 Cascode amplifier operation

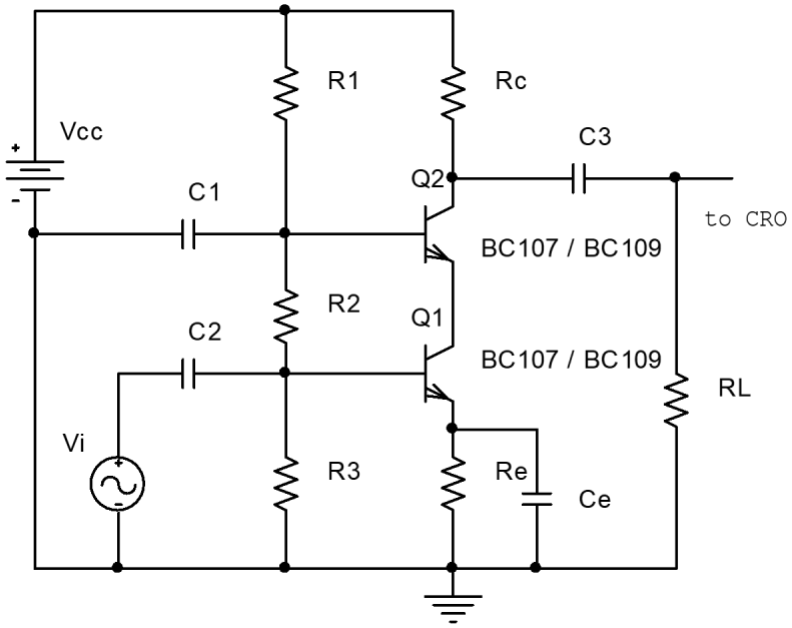


Fig 3. 2: Cascode Amplifier Circuit

3.3.2 Transient Analysis

Transient analysis is nothing but taking voltages and current at different instants. It is seen that there is a 180^o phase shift between the input and output waveforms (Fig. 3.4, 3.5). This is because the CE configuration has 180^o phase shift and CB configuration

has 0^o or 360^o phase shift. As result the phase shift between the input and output waveform is 180^o.

3.3.3 Cascode amplifier circuit elements and their functions

a) R_1, R_2, R_3, and R_C set the bias levels for both Q_1 and Q_2.
b) R_E for the desired voltage gain.
c) C_1, C_2 and C_3 are to act as "open circuits" at dc and act as "short circuits" at all operating frequencies of interest, i.e. $f>f_L$.

3.3.4 Cascode amplifier frequency response

The voltage gain of an amplifier varies with input signal frequency. It is because reactance's of the capacitors in the circuit changes with frequency and hence affects the output voltage. The curve between voltage gain and signal frequency of an amplifier is known a *frequency response*. Fig. 3.6

It is clear that the voltage gain drops off at low ($< f_L$) and high ($> f_H$) frequencies whereas it is uniform over mid-frequency range (f_L to f_H).

a) *At low frequencies ($< f_L$),* the reactance of coupling capacitor is quite high and hence very small part of signal will pass from amplifier stage to the load.
b) *At high frequencies ($> f_H$),* the upper cutoff frequency is much higher than a CE Amplifier due to the reduced *Ceq.*
c) *At mid frequencies (f_L to f_H),* the voltage gain of the amplifier is constant. The effect of coupling capacitor Cc in this frequency range is such as to maintain a uniform voltage gain. Thus, as the frequency increases in this range, reactance of C_C decreases which tend to increase the gain.

3.4 CASCODE AMPLIFIER ANALYSIS

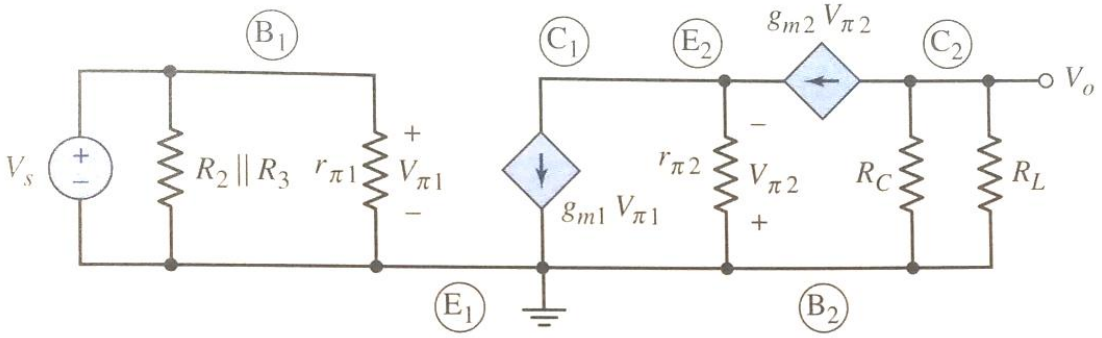


Fig 3. 3: Small signal equivalent circuit of the Cascode Configuration

a. The emitter current of the CB stage is the collector current of the CE stage. (This also holds for the dc bias current.)

$i_{e1}=i_{c2}$

b. The base current of the CB stage is:

$i_{b1}= i_{e1} = i_{c2}/ (\beta+1)$

c. Hence, both stages have about same collector current $i_{c1}\approx i_{c2}$ and same g_m.

$g_{m1}=g_{m2}=g_m$

The input resistance $R_{in1}$to the CB stage is the small-signal "R_C" for the CE stage

$i_{b1}= i_{e1} = i_{c2}/ (\beta+1)$

The CE output voltage, the voltage drop from Q2 collector to ground, is:

$v_{cg2} = v_{eg1}= - r_{\pi1} i_{b1}= - r_{\pi1}\, i_{e1}/ (\beta+1) = - r_{\pi1}\, i_{c2}/ (\beta+1)$

Therefore, the CB Stage input resistance is:

$R_{in1}= v_{eg1} / (-i_{e1}) = r_{\pi1}/(\beta+1) = r_{e1}$

$A_{vCE\_Stage} = v_{cg2}/ v_{sig} \approx - R_{in1}/ R_E = - r_{e1} / R_E<1$

Now, find the CE collector current in terms of the input voltage Vsig:

$i_{b2} \approx v_{sig} / (R_{sig} \| R_B + r_{\pi2} + (\beta+1) R_E)$

$i_{c2}=\beta i_{b2} \approx \beta\, v_{sig} / (R_{sig} \| R_B + r_{\pi2} + (\beta+1) R_E) \approx \beta v_{sig} / ((\beta+1) R_E)$

for bias insensitivity: $(\beta+1) R_E \gg R_{sig} \| R_B + r_{\pi2}$

$i_{c2} \approx v_{sig}/R_E$

$V_o = -i_{c2} R_c$

$A_v = V_{out}/V_{sig} = -R_c/R_E$

3.5 MODEL GRAPH

3.5.1 Transient Analysis

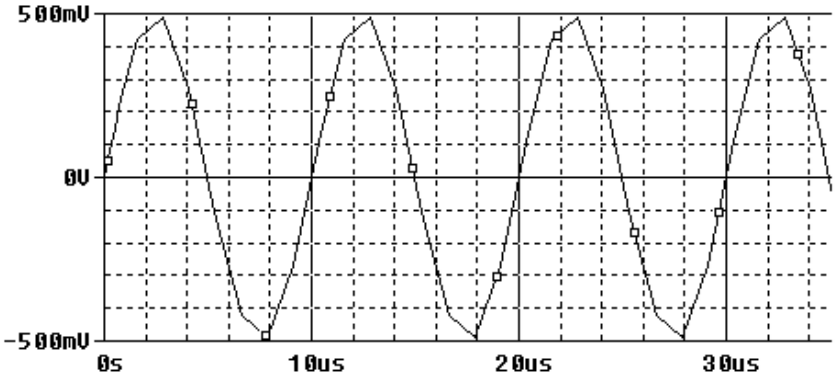


Fig 3. 4: Input Voltage Waveform

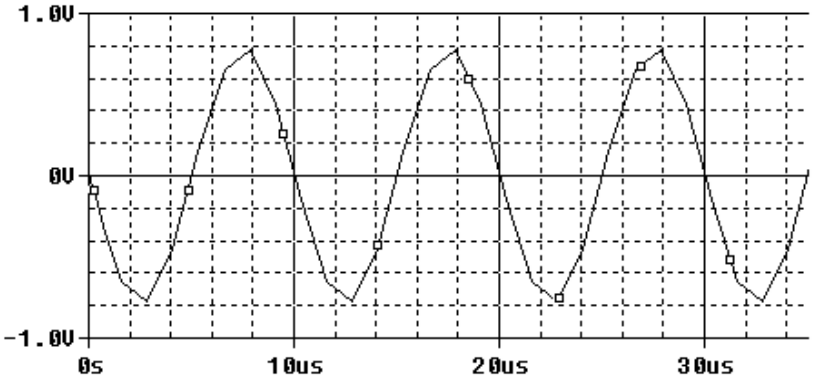


Fig 3. 5: Output Voltage Waveform

3.5.2 Frequency Response

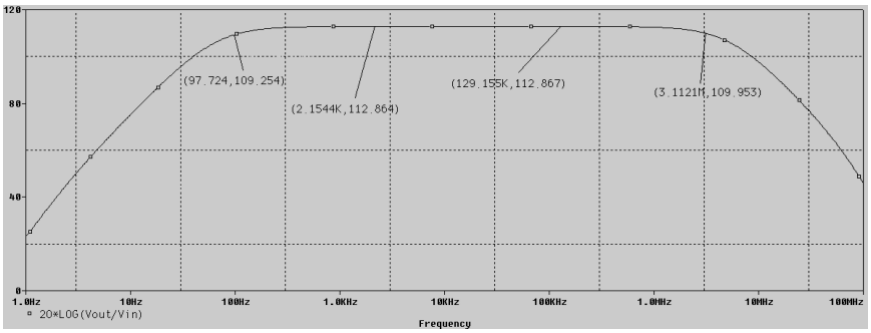


Fig 3. 6: Frequency Response

3.6 DESIGN PROBLEM

(iii) Design a Cascode amplifier using BC107 transistor with Vcc = 20V, $V_{CE1(min)} = V_{CE2(min)} = 3V$, $V_E = 5V$, $R_L = 90K\Omega$ and $f_L = 100Hz$.

Procedure

Given $V_{CC} = 20V$,

$V_{CE1(min)} = V_{CE2(min)} = 3V$,

$V_E = 5V$,

$R_L = 90k\Omega$ and $f_L = 100Hz$.

The data sheet of BC107 transistor shows:

$h_{ie} = 3k\Omega$ and $h_{FE}=190$

Selection of R_C

$R_C << R_L$ so that R_L will have little effect on the circuit voltage gain.

Select $R_c = R_L/10 = 9K\Omega$ (8.2KΩ Standard value)

Selection of R_E

$V_{RC} = V_{CC}-V_{CE1}-V_{CE2}-V_E$

$=20 – 3 – 3 – 5 = 9V$

$IC = V_{RC} / R_C$

$= 9 / 8.2K = 1.1mA$

$R_E \approx V_E / I_C$

$= 5 / 1.1m = 4.5K\Omega$ (4.7KΩ Standard value)

$R_3 = 10\ R_E$

= 10 x 4.7K = 47KΩ

Selection of R_1 and R_2

$V_{B1}=V_E+V_{BE}$

= 5 + 0.7 = 5.7V

$I_3 = V_{B1} / R_3$

= 5.7 / 47k =121μA

$V_{B2} = V_E + V_{CE1} + V_{BE2}$

=5 + 3 + 0.7 = 8.7V

$V_{R2} = V_{B2} – V_{B1}$

= 8.7 – 5.7 = 3V

$R_2= V_{R2} / I_3 = 3 / 121μ$

= 24.8kΩ (22kΩ + 2.7kΩ Standard value)

$R_1= (V_{CC} – V_{B2}) / I_3$

=(20 – 8.2) / 121μ =93.4k (47kΩ + 47kΩ Standard value)

Selection of C_1 , C_2 and C_E

The coupling capacitors C_1 and C_2 should have negligible effect on the frequency response of the circuit. So, the reactance of each coupling capacitor is selected to be approximately equal to $1/10^{th}$ of the impedance in series with it at the lowest operating frequency for the circuit.

Zi = hie || R3 || R2

= 3k || 47K || 24.8K = 2.53 k

$C_1=1 / 2\pi f_L(Z_i / 10)$

= 1 / 2 π 100 (2.53k / 10) = 6.29 μF (3.3μF standard Value)

$C_2 = 1 / 2\pi f_L(h_{ie2} / 10)$

= 1 / 2π 100 (3k / 10) = 5.3 μF (3.3μF standard Value)

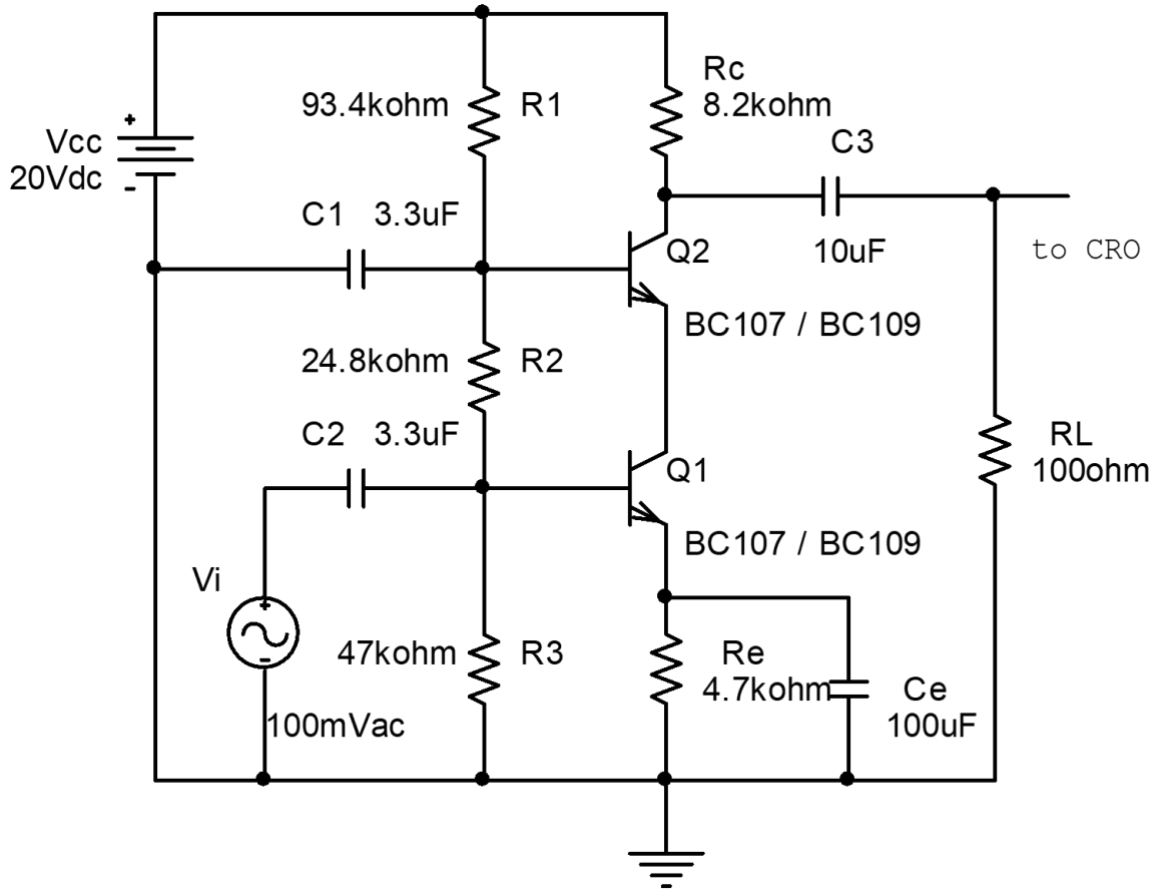


Fig 3. 7: Designed Circuit

3.7 PROCEDURE

Transient and Frequency response curve measurements

a. Feed 100mV (peak-to-peak) sinusoidal signal at 1KHz frequency as the input signal (Vs) to the CE circuit.

b. Observe the input and output voltages simultaneously on a CRO. Note down the amplitude,

frequency and phase difference between the two voltages in the table.

c. In the above assembled circuit, keep the magnitude of the source same, ie., 100mv and vary

the frequency from 50 Hz to 10 MHz and measure the voltage gain of the amplifier at each

frequency across R_L. Take atleast 10 readings and tabulate the reading in Table. Plot on a

semi log graph sheet the frequency response (voltage gain Vs frequency) curve using the above measurements.

d. From the plot, determine the values of (a) Mid band voltage gain, Av(mid), (b) Lower cut-off frequency,(c) upper cut-off frequency and (d) Bandwidth.

3.8 TABULATION

Transient Analysis

	Amplitude	Frequency	Phase difference
Input signal			
Output signal after 1st transistor			
Output signal after 1st transistor			

Frequency Response **V_i = _____V**

Frequency	Output Voltage (Vo)	Gain	Gain in db $A_v = 20 \log(Vo/Vi)$

3.9 PRELAB QUESTIONS

1. In what ways the Cascode amplifier has advantage over CE amplifier?
2. Why the analysis of Transistor circuit is split in to AC while keeping all the DC source equal to zero and DC while keeping all the AC source equal to zero.
3. What does the term small signal imply?
4. Discuss the construction of Cascode amplifier.
5. What are the physical meaning of hybrid π parameters r_π , r_o.

3.10 POSTLAB QUESTIONS

1. Compare the AC characteristics of CE amplifier and cascade amplifier.
2. Discuss the general conditions under which the cascade amplifier would be used.
3. Compare the transient characteristics of input signal and output signal.

3.11 RESULT

a. The phase difference between the input and output voltage waveform is _____

b. The Mid-band voltage gain =

c. The Lower cutoff frequency =

d. The Upper cutoff frequency =

e. Bandwidth=

4. RC PHASE SHIFT OSCILLATOR

4.1 OBJECTIVE

To design and construct the RC phase shift Oscillator to generate a sine wave of output frequency is 1.5 KHz.

4.2 HARDWARE REQUIRED

a.	Power supply	:	Dual variable regulated low voltage DC source (0-30V, 0-2A)
b.	Equipments	:	CRO (0-30MHz)
c.	Resistors	:	R1=68kΩ, R2=22kΩ, Rc=3.3kΩ, Re=2.2kΩ, R=3.3kΩ
d.	Capacitor	:	Co=1µf, C=0.01µf, Ce=100µf
e.	Semiconductor	:	BC107 or BC109
f.	Miscellaneous	:	Bread board and wires

4.3 THEORY

Definition: An Oscillator is an amplifier, which uses positive feedback and without any external input signal, generates an output waveform by energizing the DC signal. An Oscillator is a source of AC voltage. Oscillations are produced in the circuit when Barkhausen Criterion is satisfied.Barkhausen Criterion

(1)The total phase shift in the closed loop is $0^{\bullet}$ or $360^{\bullet}$.

(2)The magnitude of the loop gain of the amplifier (A) and the feedback factor β is unity.

$$A\beta = \angle 0^{\bullet}$$

The frequency of Oscillation is determined by the frequency selective feedback network (R-C, L-C). In the RC phase shift Oscillator, the cascaded RC networks determine the frequency. It is an Audio frequency Oscillator capable ofGenerating signals from 15Hz to 20 KHz. The frequency of Oscillations can be varied over a wide range by ganged tuning the capacitor.

The frequency of oscillation is given by the relation

$$f_0 = f_{TH} = \frac{1}{(2\pi RCv(6 + \left(\frac{4RC}{R}\right))}$$

Where R = value of resistor in the phase shift network C = value of capacitor in the phase shift network. For the loop gain to be greater than unity, the current gain of the transistor,

$h_{femin} > 23 + 29 (R/R_C) + 4 (R_C/R)$.

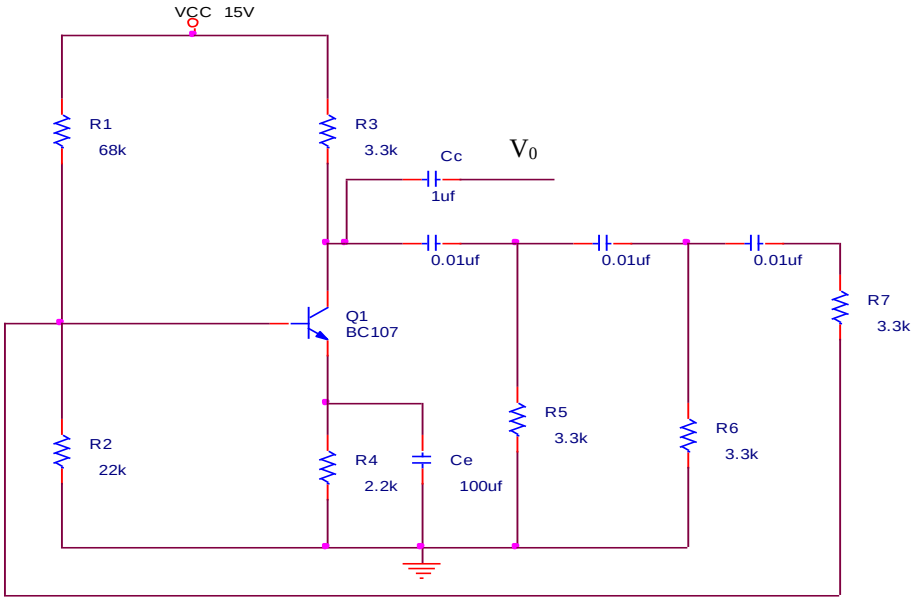


Fig 4.1 Circuit Diagram

4.4 MODEL GRAPH

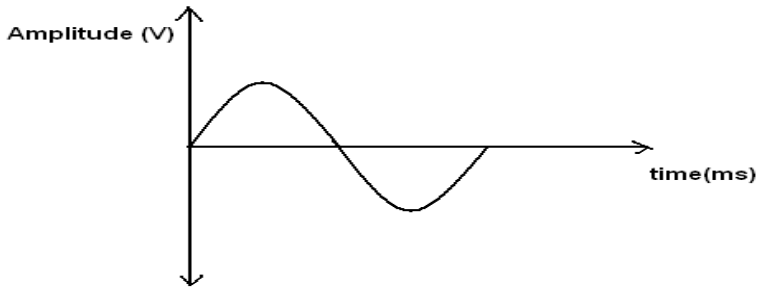


Fig 4.2 Model Graph

4.5 DESIGN PROBLEM

Let us consider, f = 1.5 KHz, Active Load R_L=47K ohm,Vcc=15 volt, C_{out}=1µf and h_{fe}=500

As h_{fe}= 500 considered above from data sheet of transistor h_{ie}=3kΩ.

Feedback circuit design

Since R = R_C/ 10

R_C = R*10 = **33KΩ (use a standard 3.3KΩ ohm)**

$$I_c = \frac{V_{cc} - V_{ce} - V_e}{R_c} = \frac{(15 - 5 - 3)}{33k} = 1.4m$$

$R_e = \frac{V_e}{I_c} = \frac{3}{1.4} = \mathbf{2.14K}$ (use a standard 2.2 Kohm)

Selection of R_1& R_2:

R_2=10Re gives I_2=Ic/10

R_2=10 x 2 KΩ **= 22 KΩ**

R_1 = (Vcc-Vb) /I_2

= 15- (Vbe+Ve) / 140µA = 15-(0.7+3)/140µA = **66.43KΩ** (use standard 68 KΩ)

Selection of Ce:

$$X_{ce} = \frac{h_{ie}}{(1 + h_{fe})} = \frac{3K}{(1 + 500)} = 15.71$$

$$C_e = \frac{1}{(2\pi f X_{ce})}$$

Ce= 101.36µf (use standard 100 µf)

Frequency of oscillation ,

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

Assume ,C = 0.01 µF

$$1.5KHz = \frac{1}{2\pi R * 0.1\mu F * \sqrt{6}}$$

R = 3.3 KΩ

4.5.1 Design Constraints

1. Frequency of oscillation is proportional to $f = \frac{1}{2\pi RC\sqrt{2N}}$, where N is the number of stages. Thus RC phase shift oscillator at higher frequencies have high phase noise which results in instability in frequency as number of stages increases.

2. It requires very small resistor value which is difficult to realize on chip.

4.6 PROCEDURE

1. Connections are made as shown in the circuit diagram.
2. The DC power supply is switched ON.
3. The output waveform is displayed on the CRO.
4. The peak to peak Amplitude and time period of the sine wave is noted.
5. The graph of output waveform is drawn.

4.7 TABULATION

	Amplitude (Volts)	**Time period(sec)**	**Frequency (Hz)**
Practical value			
Theoretical value			

4.8 PRE LAB QUESTIONS

1. What is Phase shift oscillator?
2. What is the difference between RC phase shift oscillator and LC oscillator?
3. What is the condition for sustained oscillation in RC phase shift oscillator?
4. What is the equation for RC phase shift oscillator?
5. What are the applications of RC phase shift oscillators?

4.9 POST LAB QUESTIONS

1. Why we need a phase shift between input and output signal?
2. Why RC oscillators cannot generate high frequency oscillations?

3. What difference will the number of sections(R&C) in the oscillator circuit make?
4. How is phase angle determined in RC phase shift oscillator?
5. How can we get a maximum phase angle of 90˚ in RC phase shift oscillator?
6. What is the maximum frequency for which a RC phase shift oscillator can be designed without any distortion in phase?

4.10 RESULT

Thus an RC phase shift oscillator is designed, constructed and tested. Frequency of oscillationTheoretical f_T= , Practical f_P=

5. PSPICE SIMULATION OF CLASS C POWER AMPLIFIER

5.1 OBJECTIVE

To study the characteristics of Class C Power amplifier.

5.2 SOFTWARE REQUIRED

PSPICE – OrCAD 9.2 lite

5.3 BACKGROUND

SPICE is software that simulates electronic circuits. SPICE can perform various analyses such as DC analysis, Transient analysis, AC analysis and operating point measurements. SPICE contains model for common circuit elements active as well as passive and it is possible of simulating most electronic circuits. The abbreviation of SPICE is **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

5.4 THEORY

An amplifier receives a signal from some pickup transducer or other input source. This signal isgenerally small and needs to be amplified sufficiently to operate an output device. At first, theinput voltage level is improved using voltage amplifier and this is then fed to power amplifier toobtain sufficient power at the output.In fact, a power amplifier does not amplify power. It only takes power from the dc power supplyconnected to the output circuit and converts it into useful ac signal power.Depending upon the amount of the output signal variation over one cycle of operation for a fullcycle of input signal, power amplifiers are grouped into various classes like Class A, Class B,Class AB, Class C, Class D, etc. In class A power amplifier, the transistor conducts for theentire cycle of the input signal and hence the output signal varies for a full 360° of the cycle.Class B power amplifier circuit provides an output signal varying over one half the input cycle.For class C operation, the transistor conducts for an interval shorter than a half cycle. The result is periodically pulsating current waveform. To obtain a sinusoidal output voltage, this current is passed through a parallel LC circuit. This circuit acts as band pass filter and provides an outputvoltage proportional to the amplitude of the fundamental component

in the Fourier seriesrepresentation of the current waveform. The resonant frequency of the LC combination is

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

where, L and C are the inductance and capacitance respectively of the LC combination.The

Quality Factor

$$Q = \frac{X_L}{R_L}$$

of the tank circuit is assumed to be high. Voltage gain at resonantfrequency is a maximum while it drops on either side of resonance

5.5 CIRCUIT DIAGRAM

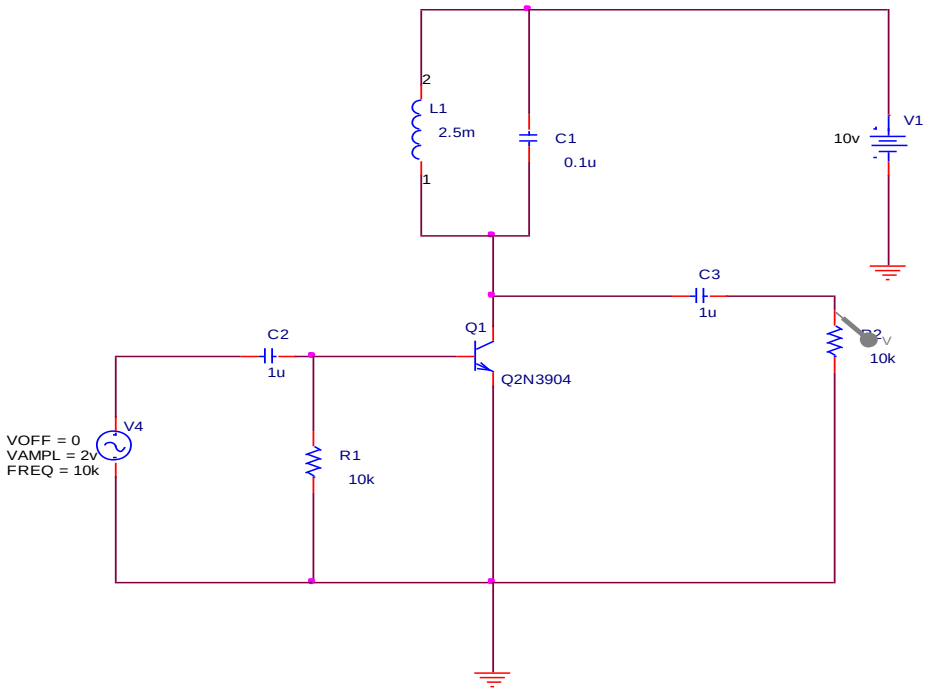


Fig 9.3 Schematic Diagram using PSPICE

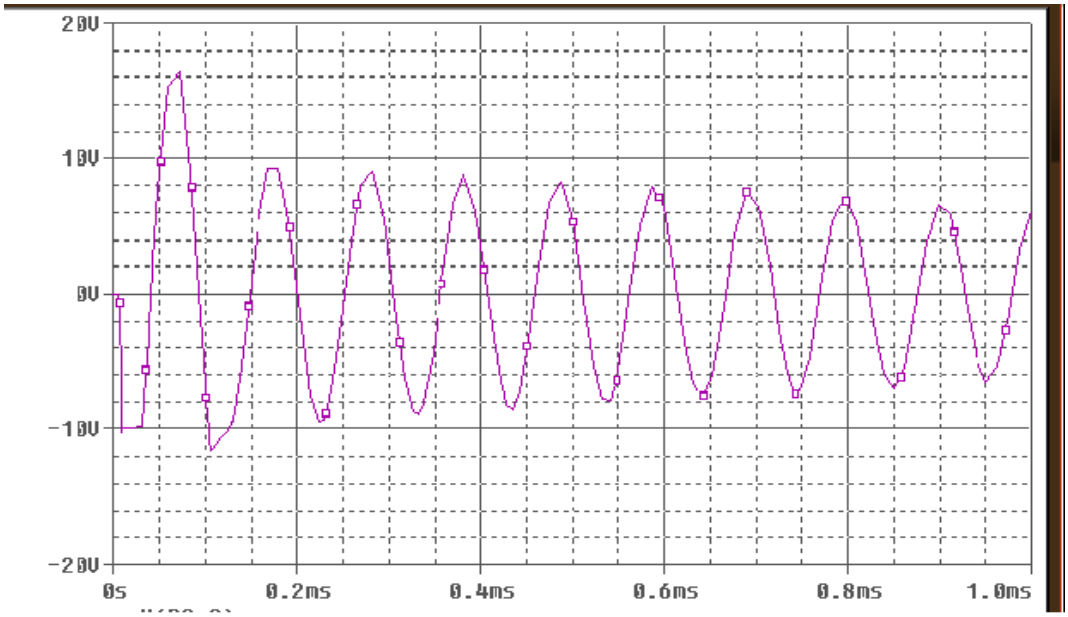
5.6 PROCEDURE

9. Open Capture Lite Edition.
10. Go to the File menu and select New Project. Select Analog or Mixed A/D
11. Create a blank project and then click OK.
12. Select ‘Place’ option from tool bar. Pick and place all the required circuit components by just clicking on the elements.

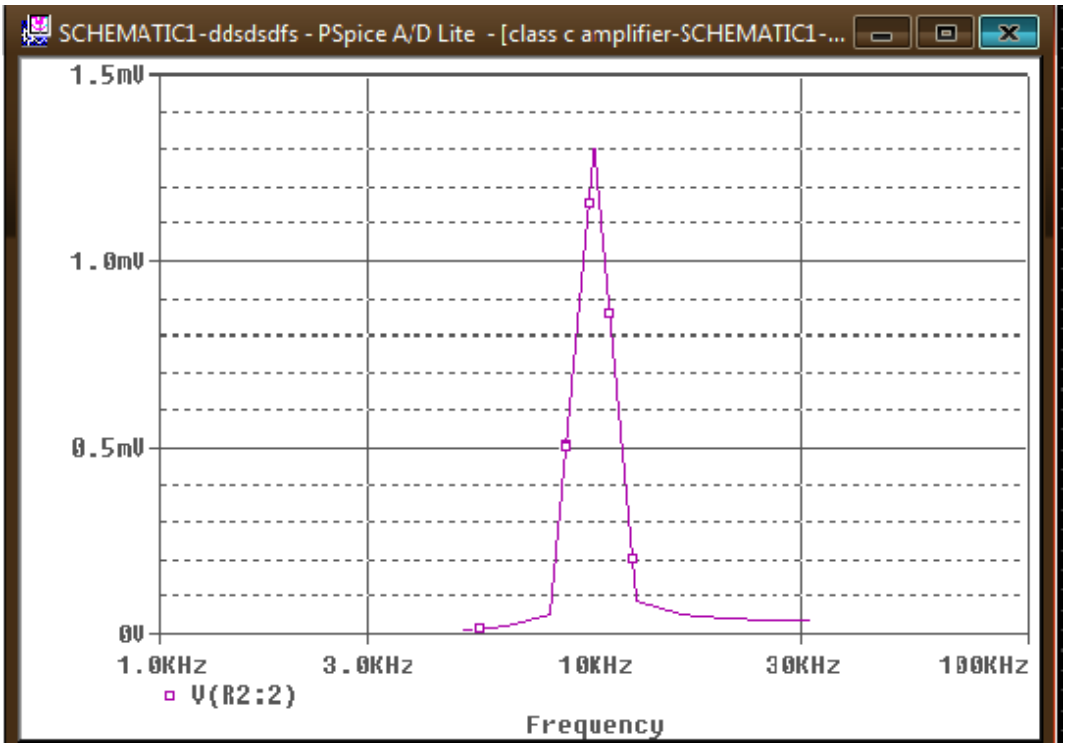
13. Connect the components as per circuit diagram using ‘place wire’ button that is available in tool bar.
14. Click on each components to give the parameter values as per design.Save the schematic.
15. Create a new simulation profile. Mention the type of analysis and simulate the circuit.
16. Measure the voltages and currents at different points and tabulate the readings.

5.7 PSPICE OUTPUT

5.7.1. Transient Response



5.7.2. Frequency Response



5.8 PRELAB

1. What is meant by a large signal amplifier? State its types.
2. Which type of power amplifier is biased for operation at less than 180º of the cycle?
3. Calculate the resonant frequency of the LC collector tuned circuit.

5.9 POST LAB

1. State the practical applications of Class C amplifiers.
2. Define conversion efficiency of a power amplifier. What is its value for class C power amplifier?

5.10 RESULT:

Thus the transient and frequency response of Class C Power amplifier is studied.

6. DESIGN AND ANALYSIS OF BASIC BJT DIFFERENTIAL PAIRS

6.1 OBJECTIVE

1. To design a Differential Amplifier for the given specifications.
2. To determine the dc collector current of individual transistors and also to calculate Common mode rejection ratio.

6.2 HARDWARE REQUIRED

a.	Regulated Power supply		:Variable regulated low voltage DC source (0-30V, 0-2A)
b.	Equipments	:	Signal Generator (0.3Hz-3MHz), CRO (0-30MHz)
c.	Resistors	:	To be calculated
d.	Semiconductors	:	BC 109 (or equivalent)
e.	Miscellaneous	:	Breadboard and wires.

6.3 THEORY

As the name indicates **Differential Amplifier** is a dc-coupled amplifier that amplifies the difference between two input signals. It is the building block of analog integrated circuits and operational amplifiers (op-amp). One of the important feature of differential amplifier is that it tends to reject or nullify the part of input signals which is common to both inputs.

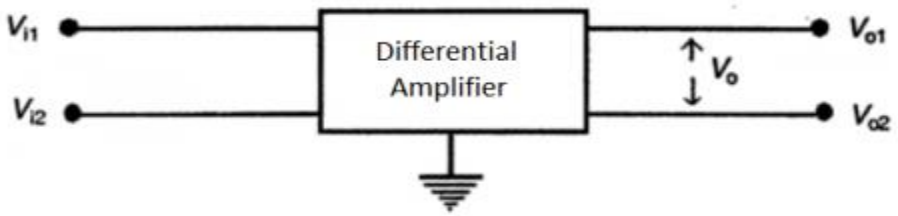


Fig 6.1 Block Diagram

V_{i1} and V_{i2} are input terminals and V_{o1} and V_{o2} are output terminals with respect to ground. We can feed two input signals at the same time or one at a time. In the former case it is called dual input otherwise it is single input. Similarly there are two ways to take output also. If the output is taken from one terminal with respect to ground, it is unbalanced output or if the output is taken between two output terminals, it is balanced output.

Working of a Differential Amplifier

When a differential amplifier is driven at one of the inputs, the output appears at both the collector outputs. This is explained with a diagram below.

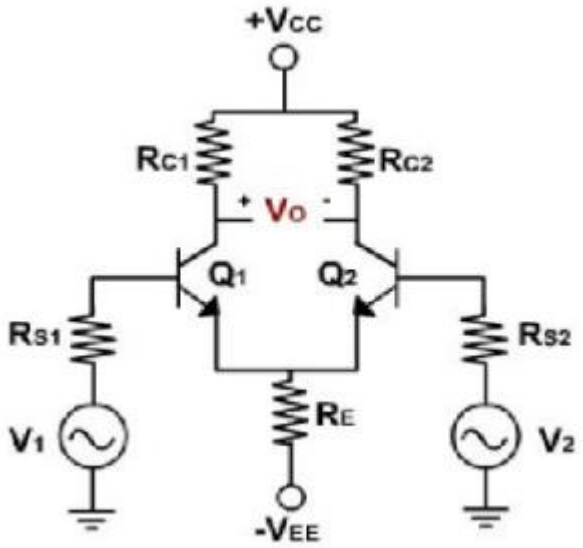


Fig 6.2 Circuit Diagram

When input signal $V_1$is applied to the transistor Q_1, there will be a high voltage drop across the collector resistance R_{C1}, and thus the collector of Q_1 will be less positive. When input V_1 is negative Q_1 is turned OFF, and the voltage drop across R_{C1} becomes very low and thus the collector of Q_1 will be more positive. Thus we can conclude than an inserted output appears at Q_1's collector for applying signal at V_1.

When Q_1 is turned ON by the positive value of V_1 , the current through the emitter resistance R_E increases as the emitter current is almost equal to the collector current (I_EI_C). Thus the voltage drop across R_E increases and makes the emitter of both transistors going in a positive direction. Making Q_2's emitter positive is the same as making the base of Q_2 negative. In such a condition

the transistor Q_2 will conduct less current which in turn will cause less voltage drop in R_{C2} and thus the collector of Q_2 will go in a positive direction for positive input signal. Thus we can conclude that the non-inverting output appears at the collector of transistor Q_2 for input at base of Q_1.

Configuration

Based on the methods of providing input and taking output, differential amplifiers can have four different configurations as below

1. Single Input Unbalanced Output
2. Single Input Balanced Output
3. Dual Input Unbalanced Output
4. Dual Input Balanced Output

6.3.1 Single Input Unbalanced Output

In this case, only one input signal is given and the output is taken from only one of the two collectors with respect to ground as shown below.

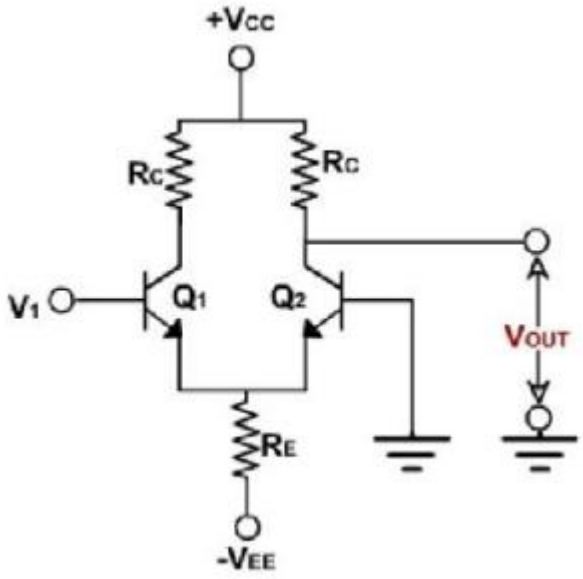


Fig 6.3 Single Input Unbalanced Output

When input signal V_{in1} is applied to the transistor Q1, it's amplified and inverted voltage gets generated at the collector of the transistor Q1. At the same time it's amplified and non-inverted

voltage gets generated at the collector of the transistor Q2 as shown in the above diagram. Unbalanced output will contain unnecessary dc content as it is a dc coupled amplifier therefore this configuration should follow by a level translator circuit.

6.3.2 Single Input Balanced Output

As above only one input signal is given even though the output is taken from both collectors.

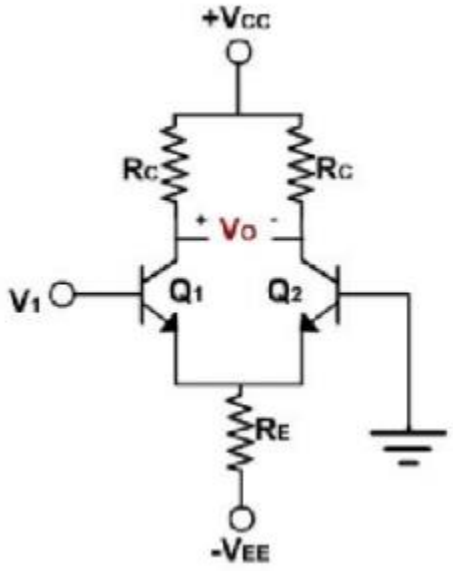


Fig 6.4 Single Input Balanced Output

This will give us more amplified version of output as it is combining the effect of both transistors. There won't be any unnecessary dc content in balanced output as the dc contents in both outputs gets canceled each other.

Vo = Vo1 – Vo2

6.3.3 Dual Input Unbalanced Output

Both inputs are given in this case ie, differential input but the output is taken from only one of the two collectors with respect to ground as shown below.

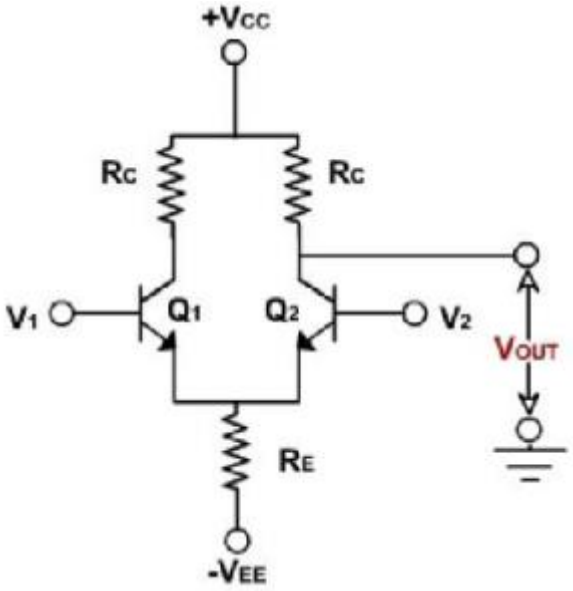


Fig 6.5 Dual Input Unbalanced Output

Amplified version of difference in both signals will be available at the output. The voltage gain is half the gain of the dual input, balanced output differential amplifier. Unbalanced output will contain unnecessary dc content as it is a dc coupled amplifier therefore this configuration should follow by a level translator circuit.

6.3.4 Dual Input Balanced Output

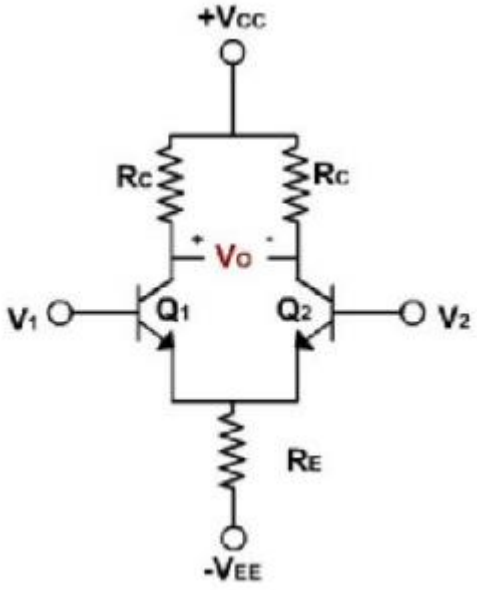


Fig 6.6 Dual Input Balanced Output

Above circuit consists of two identical transistors Q1 and Q2 with its emitters coupled together. Collectors are connected to main supply V_{CC} through collector resistor Rc. Magnitude of power supplies V_{CC} and $-V_{EE}$ will be same.

$$Vo = Ad(V_{in1} - V_{in2})$$

Where Ad = differential gain

V_{in1}, V_{in2} = input voltages

When $V_{in1} = V_{in2}$, obviously the output will be zero. ie, differential amplifier suppresses common mode signals.For effective operation, components on either sides should be match properly. Input signals are applied at base of each transistor and output is taken from both collector terminals. There won't be any unnecessary dc content in balanced output as the dc contents in both outputs gets canceled each other.

Common Mode Rejection Ratio:

Dual input balanced output differential amplifier should suppress the common signals present at its inputs. A differential amplifier is said to be in common mode when same signal is applied to both inputs and the expected output will be zero, ie ideally common mode gain is zero.Effectiveness of rejection depends on the matching of two common – emitter stages used. The ability of a differential amplifier to reject common mode signal is called Common Mode Rejection Ratio (CMRR).

$$CMRR = |differential\ gain/common\ mode\ gain|$$

$$= |Ad/Ac|$$

$$CMRR = 20log|Ad/Ac|$$

As mentioned earlier, ideally output will be zero in common mode which implies infinite CMRR.

6.4 DESIGN PROBLEM

Design differential amplifier if Q_1, Q_2=BC109, V_{CC}=10V, β=100, $-V_{EE}$ = -10 V, β_{dc} =100 and V_{BE} = 0.7V,h_{ie}=1.4kΩ ,h_{fe}=60, C1=1µf and c2=0.47µf and R_L =70kΩ

$R_{C2} << R_i$

$R_{c2} \approx R_L/10 \approx 7k\Omega$(use standard 5.6kΩ)

Select $V_{CE(min)}$=3v

$V_{RC2}=V_{CC}+V_{BE}+V_{CE(min)}=10=0.7-3=7.7v$

$I_C=V_{RC2}/R_C=7.7/6.8=1.13mA$

$R_E=(V_{EE}-V_{BE})/I_E \approx 4.1k\Omega$ (use standard 4.7kΩ)

$R_B=V_{BE}/10I_{B(max)}=V_{BE}/10(I_C/h_{fe})=3.8k\Omega$

$R_{B1}=R_{B2}=3.8k\Omega$(use standard 3.9kΩ)

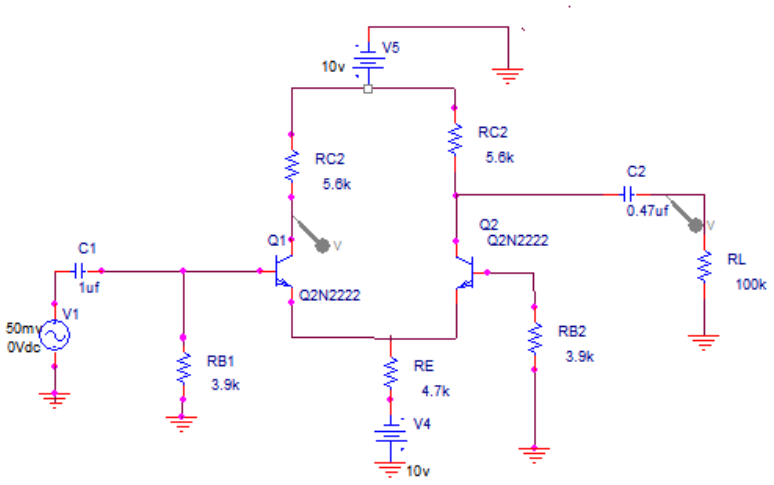


Fig 6.7 Circuit Diagram

Design Constraints

It is important to design R_C such that v_{out} never drops so low so as to force Q_1 or Q_2 into saturation.It is assumed that components are matched sufficiently such that bias current I_O is split evenly between the left and right-hand legs

Node E will take a voltage value such that

$I_{C1} = I_{C2} = I_O/2$ when $V_1 = V_2 = 0$

6.5 PROCEDURE

1. Connect the components as per the circuit diagram
2. Make the circuit quiescent (no signal) by connecting both bases to ground.
3. Measure dc values of V_{C1}, V_{C2}, I_{B1}, I_{B2} and I_E.
4. Measure the differential gain A_d (only one input used) from each input, and the common mode gainA_c(both input connected to the same source by applying 1KHz sinusoidal input voltages as shown in table(1)
5. Sketch all waveforms(V_{in1},V_{in2},V_{C1} and V_{C2}) for each input condition.

6. Calculate the common mode rejection ratio CMRR=A_d/A_c.

1.6 TABULATION

Input and Output Voltage Signal Measurements

Mode	**Input Voltage**	**Output Voltage**	**Frequency**	**Voltage Gain**	**Phase Difference**
Differential Mode	V_{in1} = 50mV V_{in2} = 0V	V_{01} = V_{02} = $V_0 = V_{01} - V_{02}$ =	1KHz		
Common Mode	V_{in1} = 50mV V_{in2} = 50mV	V_{01} = V_{02} = $V_0 = V_{01} - V_{02}$ =	1KHz		

$$\boldsymbol{CMRR = \frac{Differential\ Mode\ Gain}{Common\ Mode\ Gain} =}$$

Frequency Response **Vi = 50mV**

Frequency	Output Voltage (Vo)	Gain	Gain in db Av = 20 log(Vo/Vi)

1.7 PRE LAB QUESTIONS

1. What is a differential amplifier
2. What is common mode and differential mode inputs in a differential amplifier?
3. Define CMRR.
4. What is common mode signal?
5. Write some applications of differential amplifier.

6.8 POSTLAB QUESTIONS

1. Why differential amplifier is invariably used in the input stage of OPAMP.

2. A differential amplifier has inputs Vs1=10mV, Vs2 = 9mV. It has a differential mode gain of 60 dB and CMRR is 80 dB. Find the percentage error in the output voltage.

3. A differential amplifier has a differential gain of 20,000. CMRR=80 dB. Determine the common mode gain.

4. A change in the value of the emitter resistance R_E in a differential amplifier

(a) affects the difference mode gain A_d (b) affects the common mode gain A_c

(c) affects both A_d and A_c (d) does not affect either A_d and A_c

5. Find the CMRR if differential voltage gain and common mode voltage gain of a differential amplifier are 48db and 2 db respectively.

6.9 RESULT

Thus the differential amplifier was constructed and dc collector current for the individual transistor is determined. The CMRR is calculated as_____

7. DESIGN AND ANALYSIS OF CURRENT SERIES FEEDBACK

AMPLIFIER

7.1 OBJECTIVE

1. To design and analyze a current series feedback amplifier for the given specifications and to measure its frequency response.
2. To measure the effect of negative feedback on the frequency response.

7.2 HARDWARE REQUIRED

g.	Power supply	:	Variable regulated low voltage DC source(0-30V, 0-2A)
h.	Equipments	:	AFO(0.3Hz-3MHz), CRO(0-30MHz)
i.	Resistors	:	To be calculated.
j.	Capacitors	:	To be calculated.
k.	Semiconductors	:	BC 107 (or equivalent)
l.	Miscellaneous	:	Breadboard and wires.

7.3 THEORY

The circuit diagram of CE Amplifier with current series feedback is shown below. The resistor R_F in emitter is the feedback element. The voltage drop V_f across R_F constitutes the feedback signal while the current I_c forms the sampled signal. Hence, this forms a current series feedback. Due to negative feedback, though the voltage gain of the amplifier is decreased, it improves stability and increases the bandwidth. This is the advantage of negative feedback. Using h-parameter model for ac analysis the amplifier parameters such as the voltage gain, bandwidth can be calculated. For this, following steps have to be followed.

i) To find the input circuit, set $I_0=0$, ie open the output loop. Hence R_E appears in input side.

ii) To find the output circuit set $I_1=0$, i.e. open the input loop. Hence R_E appears in output loop.

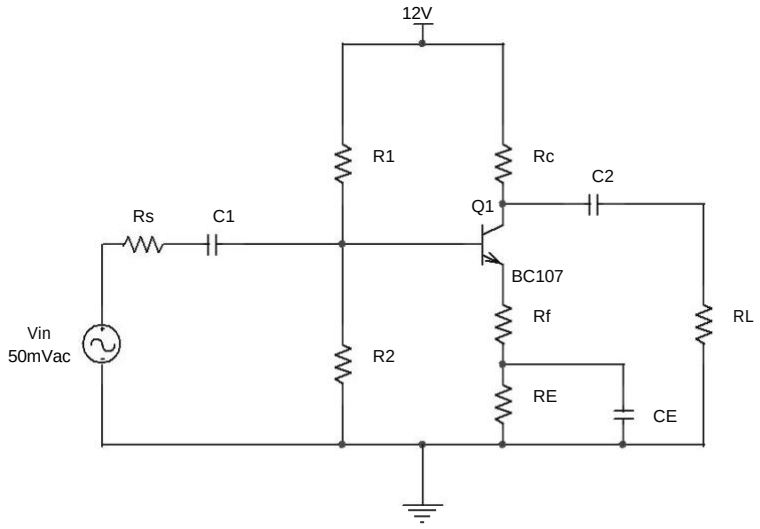
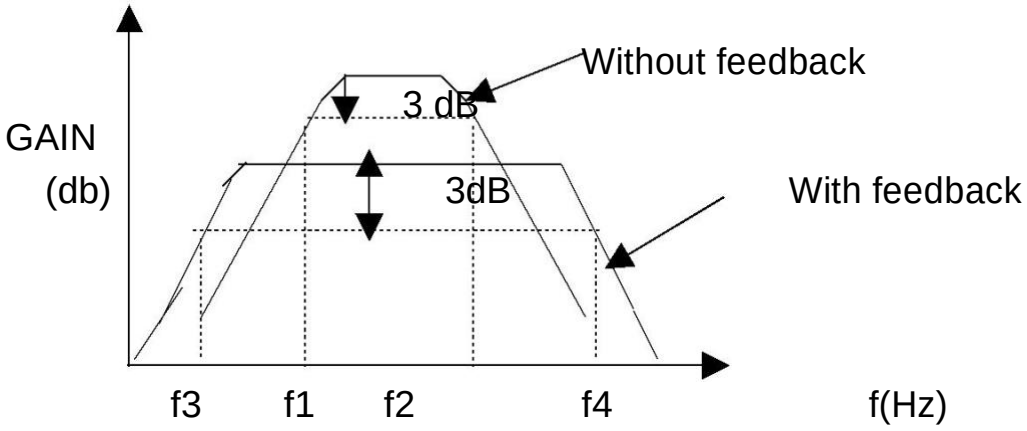


Fig 7.1 Circuit Diagram of Current-Series Feedback Amplifier

7.4 MODEL GRAPH WITH & WITHOUT FEEDBACK



f2 – f1 = Bandwidth of without feedback circuit
f4 – f3 = Bandwidth of with feedback circuit

Fig 7.2 Model Graph

7.5 DESIGN PROBLEM

Design a current series feedback amplifier using BC107 transistor with Vcc = 15V, V_{CEQ} = 5V, V_E = 3V, R_L = 47KΩ, R_f = 470Ω and f_L = 100Hz.

Procedure

Given V_{CC} = 15V, V_{CE} = 5V, V_E = 3V, R_L = 47kΩ and f_L = 100Hz.

The data sheet of BC107 transistor shows:

h_{ie} = 3kΩ and h_{FE}=190

Selection of R_C

R_C<< R_L so that R_L will have little effect on the circuit voltage gain.

Select $R_C = \frac{R_L}{10} = \frac{47K}{10} = 4.7K\Omega$ (Standard value)

Selection of R_E

$$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C}$$

Where $I_C = \frac{V_{RC}}{R_C} = \frac{V_{CC} - V_{CE} - V_E}{R_C} = \frac{(15-5-3)V}{4.7K} = 1.4mA$

$\therefore R_E = \frac{3V}{1.4mA} = 2.14K\Omega$ (use a standard 2.2 kΩ)

Given that R_f = 470Ω

$R_f + R_{E1} = R_E$

$R_{E1} = R_E - R_f$ Which Yields R_E = 1.7K (Use 1.2K and 470Ω in Series).

Selection of R_1 and R_2

Selection of voltage divider current I_2 as I_C/10 gives good bias stability and reasonably high input resistance

Selecting R_2 = 10 R_E gives $I_2 = I_C/10$

i.e., $R_2 = 10 \times 2K\Omega = 22K\Omega$ (standard value)

and $I_2 = \frac{I_C}{10} = \frac{1.4mA}{10} = 140\mu 4$

$\therefore R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{15 - (V_{BE} + V_E)}{140\mu 4} = \frac{15 - (0.7 + 5)}{140\mu 4} = 66.43K\Omega$ (use standard 68kΩ)

Selection of C_1 and C_2

The coupling capacitors C_1 and C_2 should have negligible effect on the frequency response of the circuit. So, the reactance of each coupling capacitor is selected to be approximately equal to $1/10^{th}$ of the impedance in series with it at the lowest operating frequency for the circuit.

$$X_{C1} \approx \frac{Z_i}{10} = \frac{R_1 \| R_2 \| h_{ie}}{10} = \frac{68K \| 22K \| 3K}{10} = 254\Omega \qquad \therefore$$

$$C_1 = \frac{1}{2\pi\pi_L X_{C1}} = \frac{1}{2 \times \pi \times 100 \times 254} = 6\mu F$$ (Standard value 10μF)

$$X_{C2} \approx \frac{R_L}{10} = \frac{47K}{10} = 4.7K\Omega \therefore \qquad C_2 = \frac{1}{2\pi\pi_L X_{C2}} = \frac{1}{2 \times \pi \times 100 \times 4.7K} = 0.34\mu F$$

(use a standard 0.47μf)

$C_1 = C_C$in Input Side

$C_2 = C_C$ in Output Side

Selection of C_E

$$X_{CE} = \frac{h_{ie}}{1 + h_{fe}} = \frac{3K\Omega}{1 + 190} = 15.71$$

$$\therefore \qquad C_E = \frac{1}{2\pi\pi_L X_{CE}} = \frac{1}{2 \times \pi \times 100 \times 15.71} = 101.36\mu 0$$ (use a standard 100μf)

Neglect source resistance R_S and feedback resistor R_f

.

7.6 PROCEDURE

Frequency Response of Current- Series Feedback Amplifier

1. Connect the circuit as shown in the figure.
2. Connect a sine- wave generator set at 1000Hz frequency and 50mV peak-to-peak signal voltage at the input of the amplifier circuit.
3. Connect an oscilloscope across the output nodes. Observe the sine wave output on the oscilloscope. Adjust the output of the sine-wave generator until undistorted. Maximum signal output is obtained.
4. Observe and measure the peak-to-peak amplitude of input and output signal and record the values in the tabulation provided.
5. Now, sweep the input signal frequency in the range 30Hz to 1 MHz by adjusting the sine wave generator output.
6. For each setting of input frequency, measure the output signal voltage.
7. Draw the frequency response curve on a semi-log graph sheet. From this plot, obtain the values of mid-band voltage gain, upper and lower cut-off frequency and BW (fh-fl).

Frequency Response of Amplifier without Negative Feedback

1. Remove Rf from the circuit and connect RE and CE directly to the emitter terminal.
2. Measure and record in the table, the frequency response of this circuit without Rf by repeating steps 5 through 6.

7.7TABULATION

Measurement of frequency response of current series feedback amplifier

V_{in}=

Frequency (in Hz)	**V_0 (Volts)**	**Gain= V_0/V_{in}**	**Gain (dB) = $20 \log(V_o/V_{in})$**

Measurement of frequency response of amplifier without feedback

V_{in}=

Frequency (in Hz)	V_0 (Volts)	Gain= V_0/V_{in}	Gain (dB) = 20 log(V_o/V_{in})

7.8 PRELAB QUESTIONS:

1. What do you understand by feedback in amplifiers?
2. Explain the terms feedback factor and open loop gain?
3. Compare the negative feedback and positive feedback?
4. Explain the stability of feedback amplifier?
5. Define Nyquist criterion?

7.9 POST LAB QUESTIONS:

1. What is the other name for current series feedback amplifiers?
2. What is the effect of current series feedback amplifier on the input impedance of the amplifier?
3. What is the formula for input resistance of a current series feedback amplifiers?
4. What is the effect of negative feedback on the bandwidth of an amplifiers?
5. What are the fundamentals assumptions that are made in feedback amplifiers?

7.10 RESULT:

4. The current series feedback amplifier was designed, constructed and its frequency response was plotted.
5. The following parameters were observed.

Frequency response data	**Current series feedback Amplifier**	**Current series Amplifier without feedback**
Mid_band Voltage Gain		
Bandwidth		

8.DESIGN AND ANALYSIS OF LC OSCILLATOR

8.1 OBJECTIVE

To design and analyze aColpitts Oscillator to generate a sine wave of frequency 100 KHz.

8.2 HARDWARE REQUIRED

a.	Power supply	:	Dual variable regulated low voltage DC source (0-30V, 0-2A)
b.	Equipments	:	CRO (0-30MHz)
c.	Resistors	:	R1=47kΩ, R2=10kΩ, Rc=2.2kΩ, Re=470Ω
d.	Capacitor	:	$C_e = C_{out} = 0.1\mu F$, $C_1 = C_2 = 50.7nF$
e.	Inductor	:	0.1mH
f.	Semiconductor	:	BC107 or BC109
g.	Miscellaneous	:	Bread board and wires

8.3 THEORY

The colpitts oscillator use tapped capacitance instead of tapped inductance used in Hartley oscillator. The tank circuit is made up of two capacitors C1 and C2 connected is series with each other across a fixed inductance (L). The feedback between the O/P & I/P circuit is accomplished by the voltage developed across the capacitor C2.

The feedback fraction,

$$\beta = C_1 / C_2$$

For oscillation to start, the voltage gain (AV) must be greater I/β or (C_2/C_1) , i.e $Av > C_2/C_1$

The frequency of oscillation is given by the relation,

$$\mathbf{f = 1/2\pi\sqrt{L.C_T}}$$

Where $C_T = C_2.C_1 / C_2+C_1$.

The capacitors C_1 and C_2 act as a simple alternating voltage divider. A total phase shift of 360^o between the emitter base and collector base circuits.

When the circuit is emerged by switching on the supply the capacitors C_1 and $C_2$are charged. The capacitors discharge through the coil (L) which sets up the oscillations of the frequency $f = 1/2\pi\sqrt{L.C}$. These oscillations across the capacitor C_2 are feedback to the base emitter junction and appear in an amplified form at the collector. Because of the positive feedback, the oscillations of constant amplitude are produced.

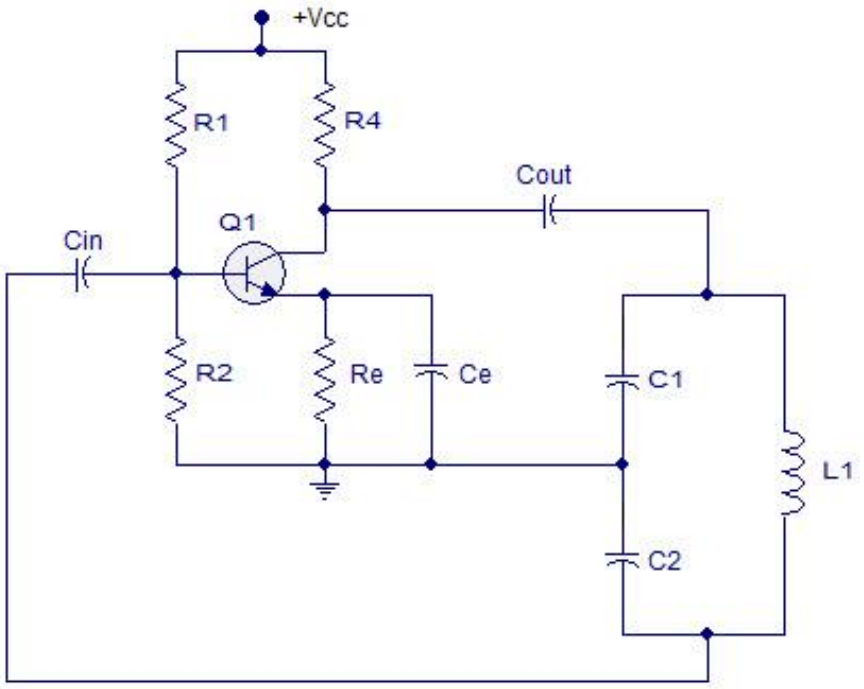


Fig 8.1 Circuit diagram of Colpitts Oscillator

8.4 OPERATION

In the circuit diagram resistors R_1 and R_2 gives a voltage divider biasing to the transistor. Resistor Rc limits the collector current of the transistor. C_{in} is the input DC decoupling capacitor while C_{out} is the output decoupling capacitor. Re is the emitter resistor and it's meant for thermal stability. Ce is the emitter by-pass capacitor. Job of the emitter by-pass capacitor is to by-pass the amplified AC signals from dropping across Re. The emitter by-pass capacitor is not there, the amplified AC signal will drop across Re and it will alter the DC biasing conditions of the transistor and the result will be reduced gain. Capacitors C_1, C_2 and inductor L_1 forms the tank circuit. Feedback to the base of transistor is taken from the junction of Capacitor C_4 and inductor L_1 in the tank circuit.

When power supply is switched ON, capacitors C_1 and C_2starts charging. When they are fully charged they starts discharging through the inductor L_1. When the capacitors are fully discharged, the electrostatic energy stored in the capacitors gets transferred to the inductor as magnetic flux. The inductor starts discharging and capacitors gets charged again. This transfer of energy back and forth between capacitors and inductor is the basis of oscillation. Voltage across C_2 is phase opposite to that of the voltage across the C_1 and it is the voltage across C_2 that is fed back to the transistor. The feedback signal at the base of transistor appears in the amplified form across the collector and emitter of the transistor.

The energy lost in the tank circuit is compensated by the transistor and the oscillations are sustained. The tank circuit produces 180° phase shift and the transistor itself produces another 180° phase shift. That means the input and output are in phase and it is a necessary condition of positive feedback for maintaining sustained oscillations. The frequency of oscillations of the Colpitts oscillator can be determined using the equation below.

8.5 MODEL GRAPH

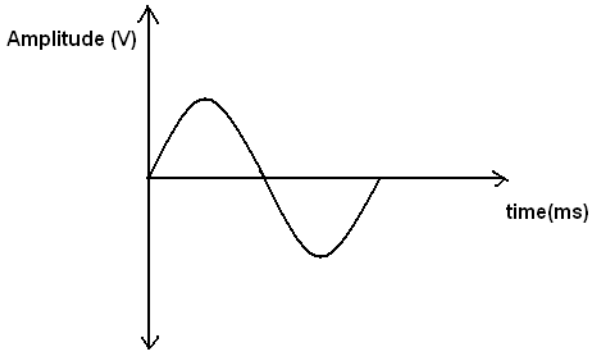


Fig 8.2 Model Graph

8.6 DESIGN PROBLEM

Feedback Network Design

Given f = 100 KHz

Assume L = 0.1mH

Oscillation frequency $f = 1/(2\pi\sqrt{LC_T})$

$100KHz = 1/(2\pi\sqrt{(0.1*10\text{^}-3)*C_T})$

$C_T = 25.3nF$

$C_T = C1C2/ (C1+C2)$

Let C1 = C2 = C

So C = 50.7nF.

Amplifier Design

Given: V_{CC} =10V; I_C = 2 mA, β = 200

Select $C_{in}= C_{out}= C_e$= 0.1uF

$V_{CE} = V_{CC}/2 = 5V$

$V_{RE} = V_{CC}/10 = 1V$

$R_E = V_{RE}/I_C = 500\ \Omega$

R_E= 470Ω (Std. Value)

$V_{CC} = V_{RE} + V_{CE} + I_CR_C$

$R_C = (V_{CC} – V_{CE} – V_{RE})/I_C$

R_C = 2 KΩ

R_C = 2.2 KΩ (Std. Value)

$V_{R2} = V_{BE} + V_{RE} = 0.7 +1 = 1.7$ V

$R_2 = \beta R_E/10 = 10\ K\Omega$

R2 = 10 KΩ

$V_{R1} + V_{R2} = V_{CC}$

$V_{R1} = V_{CC} – V_{R2} = 8.3\ V$

We have, $V_{R1}/V_{R2} = R_1 /R_2$

$R_1 = (V_{R1}/V_{R2}) \times R_2$

$R_1 = 48\ K\Omega$

R_1 = 47 KΩ (Std. Value)

Design Constraints

1. An initial voltage of 1 V has been assigned to any of the capacitor in the tank circuit to start the oscillations.
2. Assign 0 for remaining all capacitors and inductors.

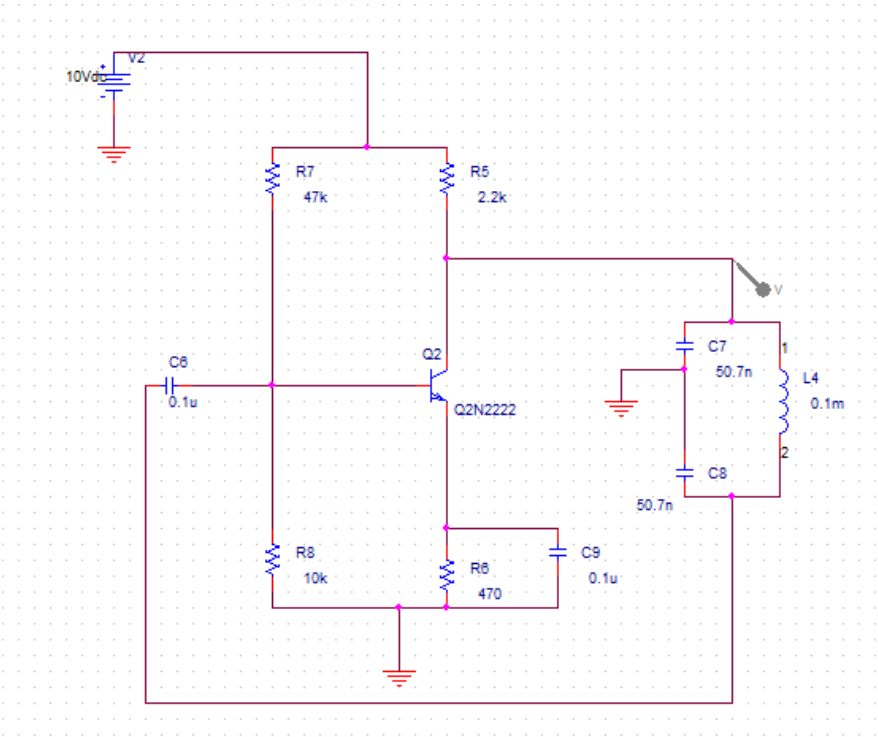


Fig 8.3 Designed Circuit in PSPICE

8.7 PROCEDURE

1. Connections are made as shown in the circuit diagram.
2. The DC power supply is switched ON.
3. The output waveform is displayed on the CRO.
4. The peak to peak Amplitude and time period of the sine wave is noted.
5. The graph of output waveform is drawn.

8.8 TABULATION

	Amplitude (Volts)	**Time period(sec)**	**Frequency (Hz)**
Practical value			
Theoretical value			

8.9 PRELAB QUESTIONS

1. Give the condition which determines the frequency of oscillation
2. How clap oscillator can be constructed from colpitts oscillator?
3. Explain the phase-shift principle in LC oscillators?
4. Compare and contrast RC & LC oscillators.
5. Where do you use IC oscillators?

8.10 POSTLAB QUESTIONS

1. What are the merits and Demerits of Colpitts oscillator?
2. What will be the value of inductance if the frequency is 1.5 KHz and C_T is 100nF?
3. Explain the main difference between an amplifier and an oscillator.
4. Write down the expression for frequency of oscillation in Colpitts oscillator.
5. Why the frequency of oscillation is not stable during a long time operation in transistor oscillators.
6. What is the minimum feedback ratio needed to generate oscillations?

8.11 RESULT

Thus theColpitts oscillator is designed and analyzed using PSPICE and the frequency of oscillation is measured.

Frequency of oscillation, Theoretical f_T= ,

Practical f_P=

9. PSPICE SIMULATION OF TWO TRANSISTOR CURRENT SOURCE USING BJT

9.1 OBJECTIVE

To design and construct two BJT transistor current source

9.2 SOFTWARE REQUIRED

PSPICE – OrCAD 9.2 lite

9.3 BACKGROUND

SPICE is software that simulates electronic circuits. SPICE can perform various analyses such as DC analysis, Transient analysis, AC analysis and operating point measurements. SPICE contains model for common circuit elements active as well as passive and it is possible of simulating most electronic circuits. The abbreviation of SPICE is **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

9.4 THEORY

Two transistor current sources also called current mirror is the basic building block in design of IC current sources. It consists of two matched or identical transistors Q1 and Q2 operating at same temperature with base and emitter terminals connected together. I.e B-E voltage is therefore the same in two transistors . When the supply voltages are applied the B-E junction of Q1 is forward biased and reference current Iref is established. Bias current Io is established by Q1, Q2 and Iref this in turn establishes quiescent current in Q3 and Q4. In constant current source circuits Beta is a dc term which is the ratio of the dc collector current to the dc base current.

9.5 CIRCUIT DIAGRAM

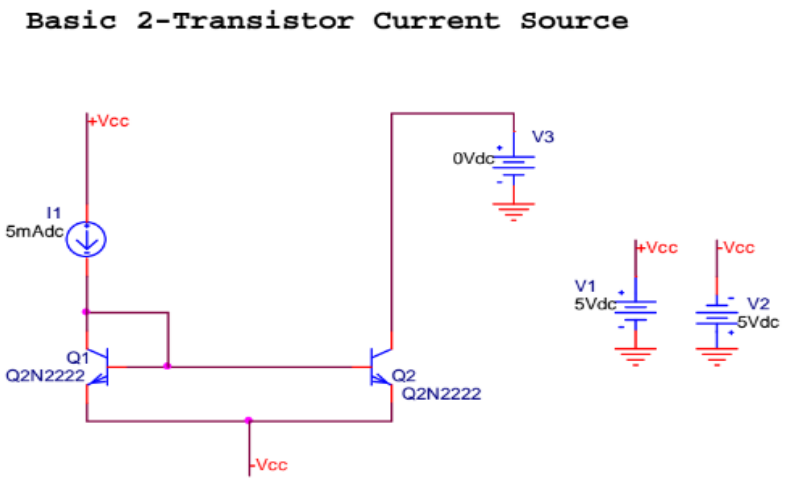
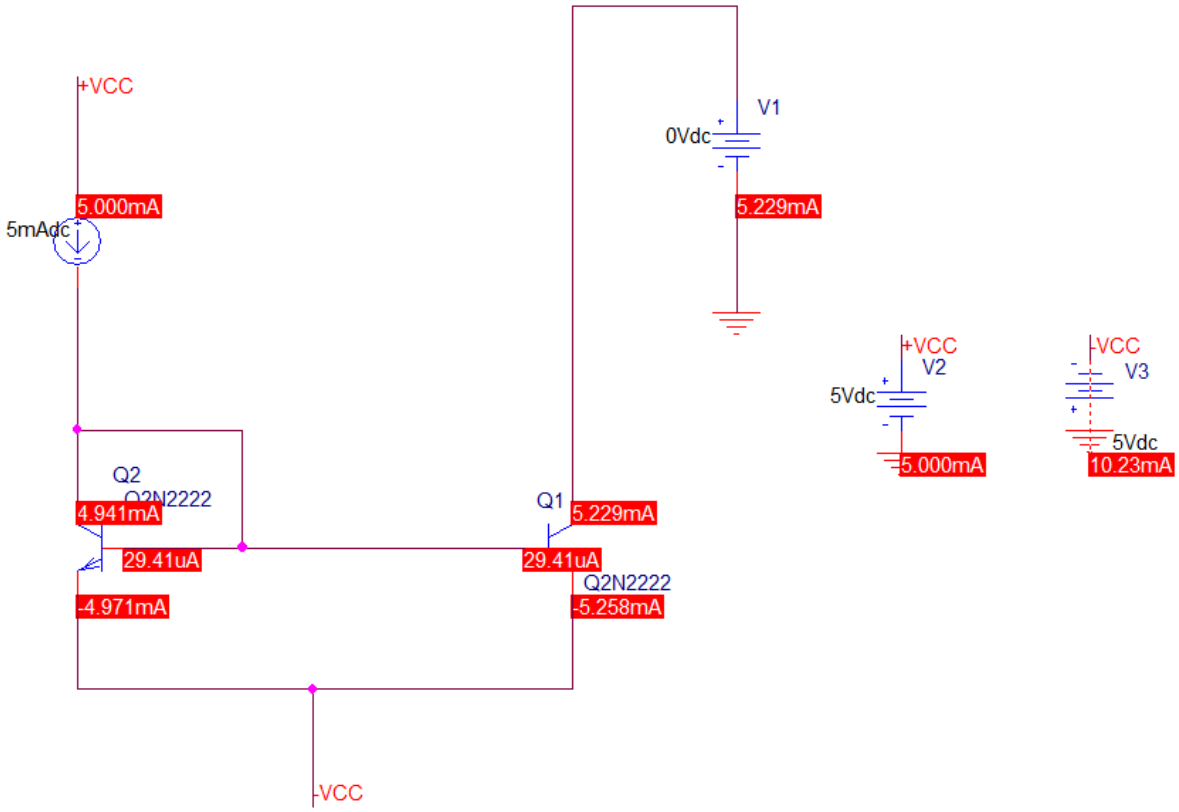


Fig 9.1 Schematic Diagram using PSPICE

9.6 PROCEDURE

1. Open Capture Lite Edition.
2. Go to the File menu and select New Project. Select Analog or Mixed A/D
3. Create a blank project and then click OK.
4. Select ‘Place’ option from tool bar. Pick and place all the required circuit components by just clicking on the elements.
5. Connect the components as per circuit diagram using ‘place wire’ button that is available in tool bar.
6. Click on each components to give the parameter values as per design. Save the schematic.
7. Create a new simulation profile. Mention the type of analysis and simulate the circuit.
8. Measure the voltages and currents at different points and tabulate the readings.

9.7 PSPICE OUTPUT



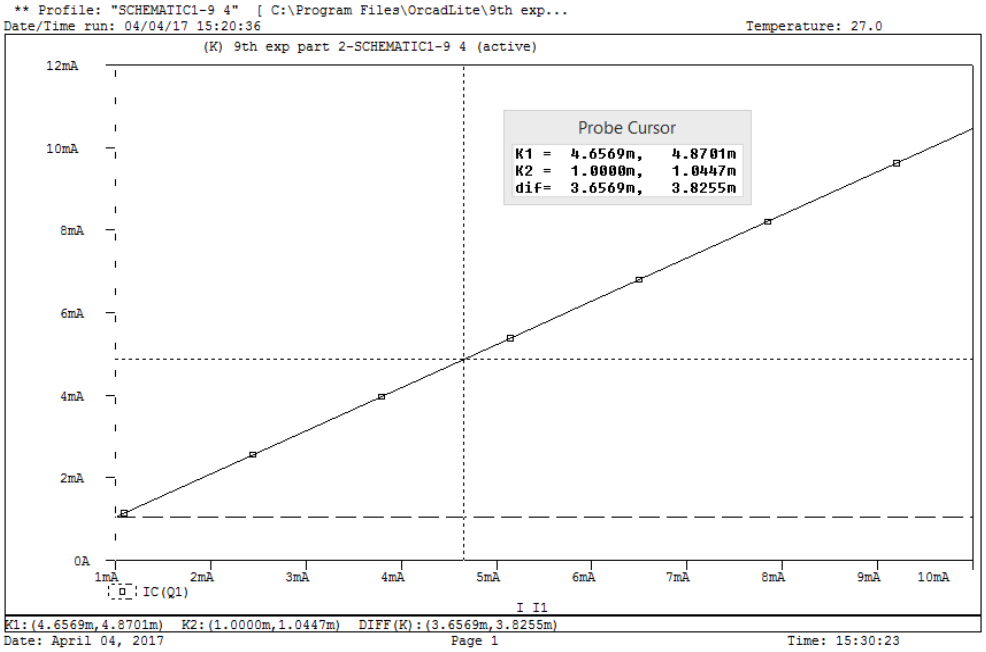


Fig 9.2 Simulation output of 2 transistor BJT current source

9.8 Prelab

1. Define current source

2. Types of Current source

3. What is meant by current mirror?

3. Current relationship between reference current and source

9.9 Post Lab

1. Discuss the differences between current sink and current source

2. Why are common emitter amplifiers more popular?

9.10 RESULT:

Thus two transistor current source using BJT was designed and constructed using PSPICE.

10. PSPICE SIMULATION OF TWO TRANSISTOR CURRENT SOURCE USING FET

10.1 OBJECTIVE

To design and construct two transistor current source using NMOS FET.

10.2 SOFTWARE REQUIRED

PSPICE – OrCAD 9.2 lite

10.3 BACKGROUND

SPICE is software that simulates electronic circuits. SPICE can perform various analyses such as DC analysis, Transient analysis, AC analysis and operating point measurements. SPICE contains model for common circuit elements active as well as passive and it is possible of simulating most electronic circuits. The abbreviation of SPICE is **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

10.4 THEORY

The basic current mirror or current source can also be implemented using MOSFET transistors. The transistor M1 is operating in the saturation or active mode, and so is M2. In this setup, the output current IOUT is directly related to IREF.

The drain current of a MOSFET ID is a function of both the gate-source voltage and the drain-to-gate voltage of the MOSFET given by ID = f (VGS, VDG), a relationship derived from the functionality of the MOSFET device. In the case of transistor M1 of the mirror, ID = IREF. Reference current IREF is a known current, and can be provided by a resistor as shown, or by a "threshold-referenced" or "self-biased" current source to ensure that it is constant, independent of voltage supply variations. Using $V_{DG} = 0$ for transistor M_1, the drain current in M_1 is $I_D = f(V_{GS}, V_{DG}=0)$, so we find: $f(V_{GS}, 0) = I_{REF}$, implicitly determining the value of V_{GS}. Thus I_{REF} sets the value of V_{GS}.

The circuit in the diagram forces the same V_{GS} to apply to transistor M_2. If M_2 is also biased with zero V_{DG} and provided transistors M_1 and M_2 have good matching of their properties, such as channel length, width, threshold voltage, etc., the relationship $I_{OUT} = f(V_{GS}, V_{DG} = 0)$ applies, thus setting $I_{OUT} = I_{REF}$; that is, the output current is

the same as the reference current when V_{DG}= 0 for the output transistor, and both transistors are matched.

10.5 CIRCUIT DIAGRAM

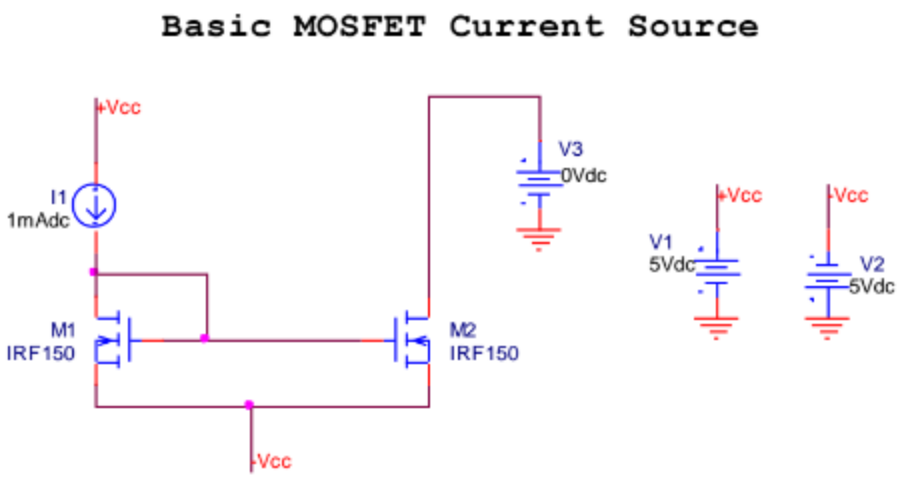


Fig 10.1 Schematic Diagram using PSPICE

10.6 PROCEDURE

1. Open Capture Lite Edition.
2. Go to the File menu and select New Project. Select Analog or Mixed A/D
3. Create a blank project and then click OK.
4. Select ‘Place’ option from tool bar. Pick and place all the required circuit components by just clicking on the elements.
5. Connect the components as per circuit diagram using ‘place wire’ button that is available in tool bar.
6. Click on each components to give the parameter values as per design. Save the schematic.
7. Create a new simulation profile. Mention the type of analysis and simulate the circuit.
8. Measure the voltages and currents at different points and tabulate the readings.

10.7 PRELAB QUESTIONS

1. Why do you call FET as field effect transistor?

2. Why FET is called a unipolar device?

3. Write down the relationship between various FET parameters?

4. How FET devices are classified?

5. Give the drain current equation of JFET.

10.8 POSTLAB QUESTIONS

1. Why the input impedance of FET is more than that of a BJT?

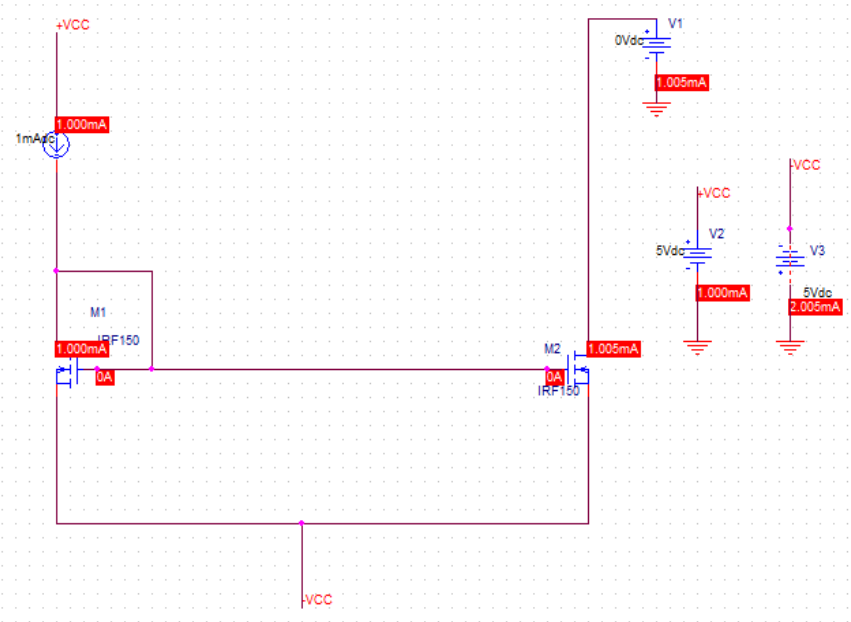
2. Why N channel FET's are preferred over P channel FET's?

3. Mention the applications of FET.

4. List the advantages of FET.

5. Compare N channel FET and P channel FET.

10.9 PSPICE OUTPUT



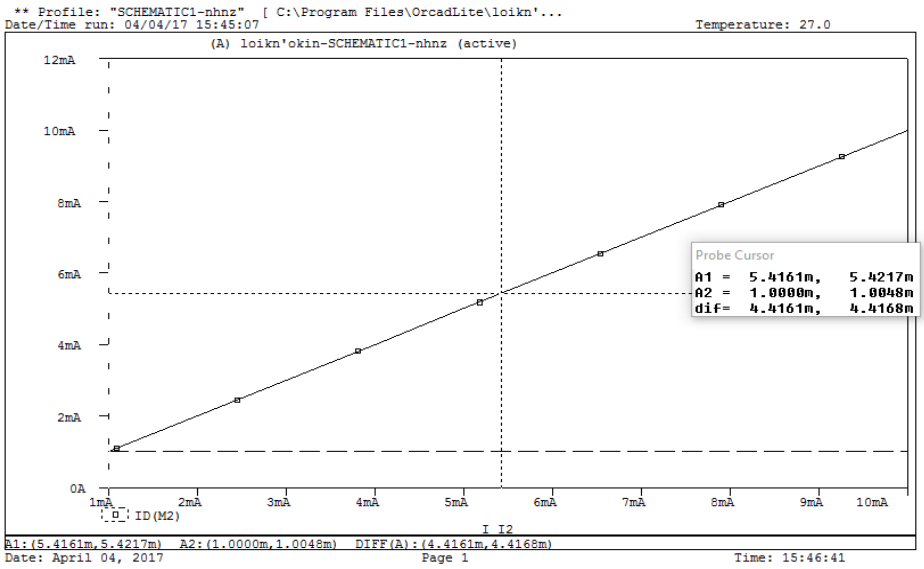


Fig 10.2 Simulation output of 2 transistor FET current source

10.10 RESULT:

Thus the two transistor current source using NMOS FET was designed and studied using PSPICE.

11. PSPICE SIMULATION OF COMMON EMITTER AMPLIFIER WITH ACTIVE LOAD

11.1 OBJECTIVE

To design and construct two BJT transistor current source

11.2 SOFTWARE REQUIRED

PSPICE – OrCAD 9.2 lite

11.3 BACKGROUND

SPICE is software that simulates electronic circuits. SPICE can perform various analyses such as DC analysis, Transient analysis, AC analysis and operating point measurements. SPICE contains model for common circuit elements active as well as passive and it is possible of simulating most electronic circuits. The abbreviation of SPICE is **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

11.4 THEORY

The current source consists of *pnp* transistors to generate a sourcing current source, and its output resistance acts as the load of transistor Q1. Since the collector load element is a *pnp* transistor instead of a resistor, it is said to be *active.* Since a DC supply offers zero impedance to anAC signal, *V*CC behaves as short-circuited; that is, one side of Q2, Q3, and *R*B is connected to the ground.

11.5 CIRCUIT DIAGRAM

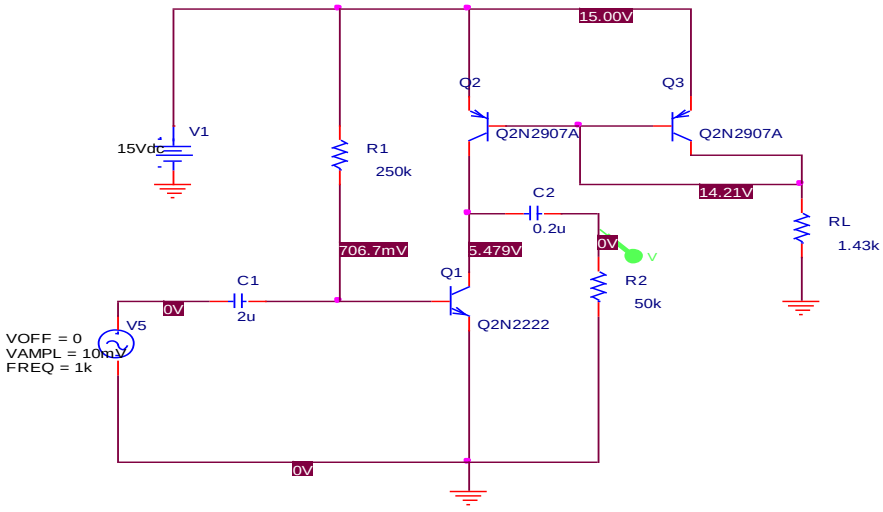
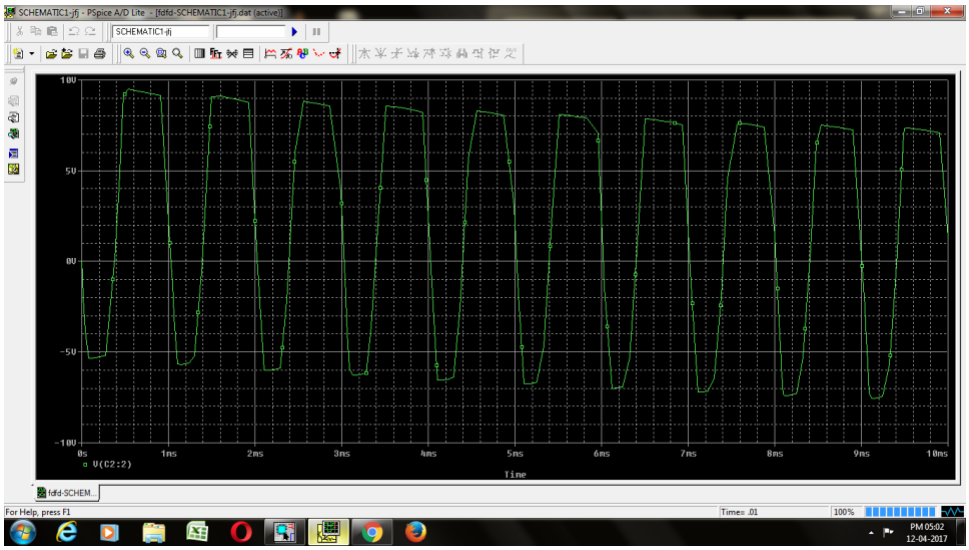
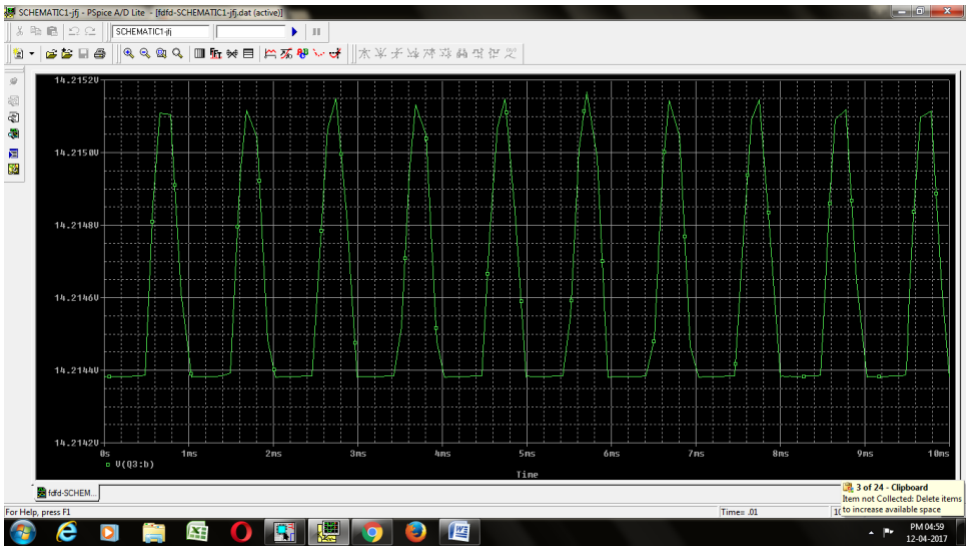


Fig 11.1 Schematic Diagram using PSPICE

11.6 PSPICE OUTPUT





11.7 PROCEDURE

1. Open Capture Lite Edition.
2. Go to the File menu and select New Project. Select Analog or Mixed A/D
3. Create a blank project and then click OK.
4. Select ‘Place’ option from tool bar. Pick and place all the required circuit components by just clicking on the elements.
5. Connect the components as per circuit diagram using ‘place wire’ button that is available in tool bar.
6. Click on each components to give the parameter values as per design.Save the schematic.
7. Create a new simulation profile. Mention the type of analysis and simulate the circuit.

11.8 RESULT:

Thus common emitter amplifier with active load was designed and constructed using PSPICE.

12. PSPICE SIMULATION OF MOSFET COMMON SOURCE AMPLIFIER WITH ACTIVE LOAD

12.1 OBJECTIVE

To design and construct two MOSFET transistor current source using Active load.

12.2 SOFTWARE REQUIRED

PSPICE – OrCAD 9.2 lite

12.3 BACKGROUND

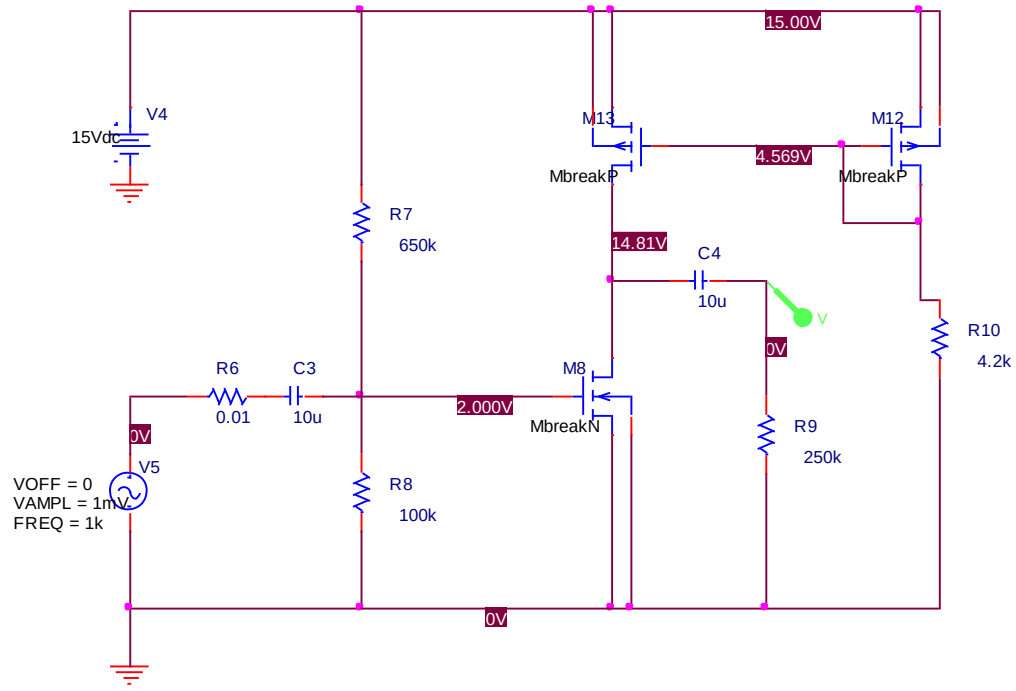
SPICE is software that simulates electronic circuits. SPICE can perform various analyses such as DC analysis, Transient analysis, AC analysis and operating point measurements. SPICE contains model for common circuit elements active as well as passive and it is possible of simulating most electronic circuits. The abbreviation of SPICE is **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

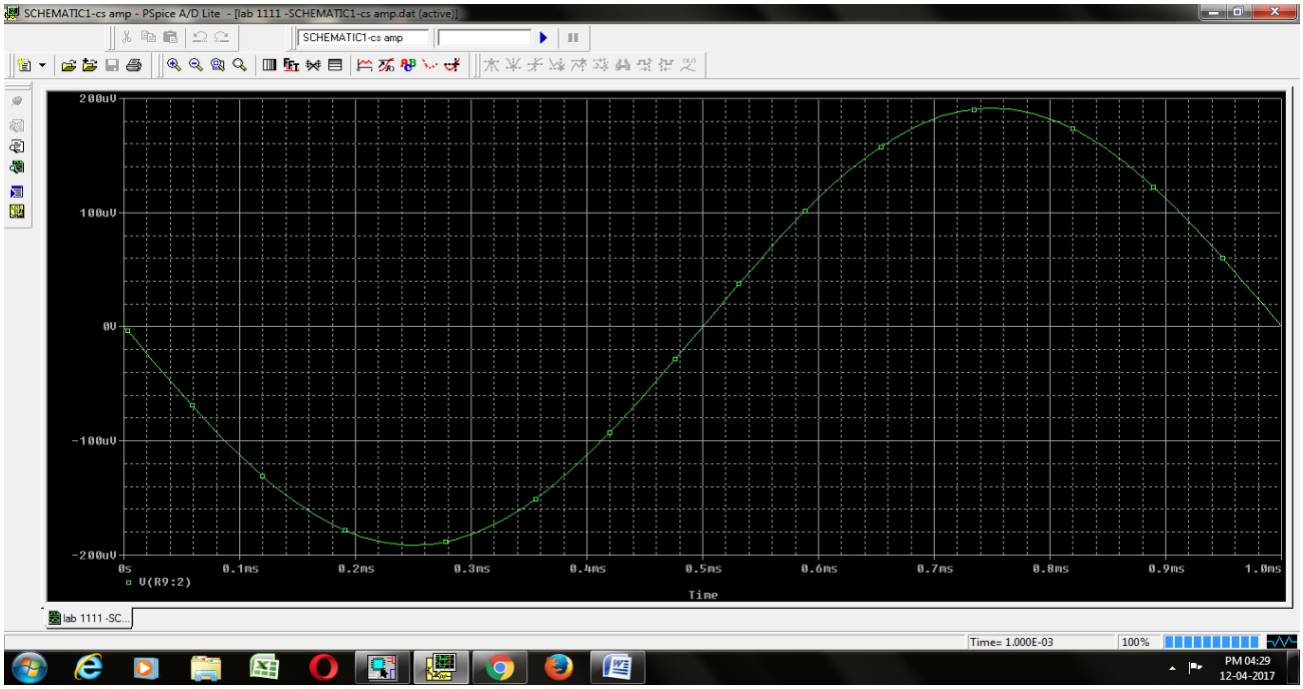
12.4 THEORY:

A basic MOSFET current source, which can be represented with a sinking current source IO with an output resistance. Thetwo transistors M2 and M3 are identical, their gate-to-source voltages are equal, and their drain currents will be same. That is, ID2 = ID3. Thus the output current IO (=ID2) will be the mirror of ID3. Since VDS3= VGS3, which is greater than or equal to (VGS3- Vt3), M3 will be in saturation.Vt2 and Vt3 be the threshold voltages of M2 and M3, respectively. For M2 to be in saturation, VDS2 must be greater than (VGS2- Vt2). This condition reduces the voltage compliance range of the MOSFET current sourceand prevents it from operating from a low power supply.

*Vtis the threshold voltage of a MOSFET, whereas VT is the thermal voltage.

12.5 CIRCUIT DIAGRAM:





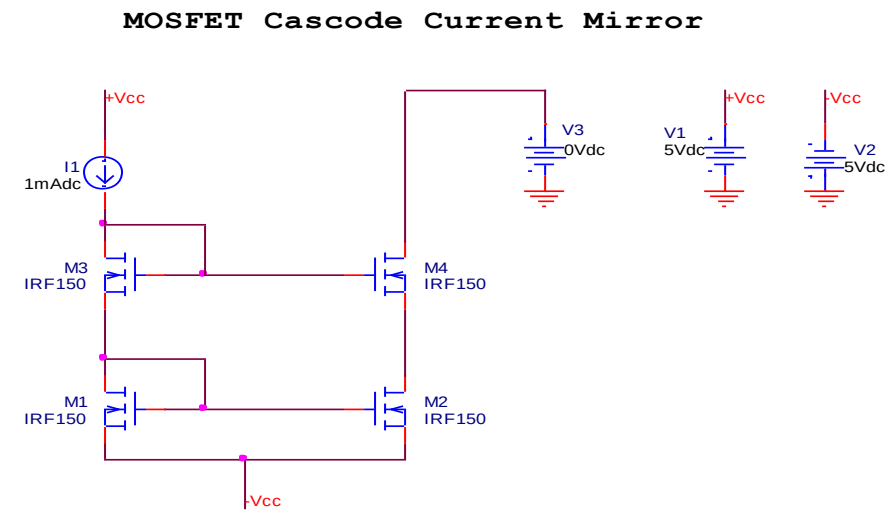


Fig 12.1 Schematic Diagram using PSPICE

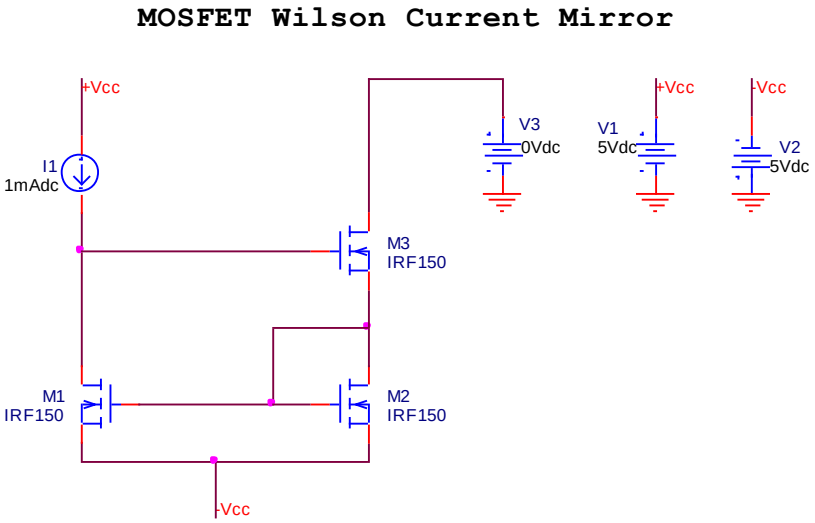


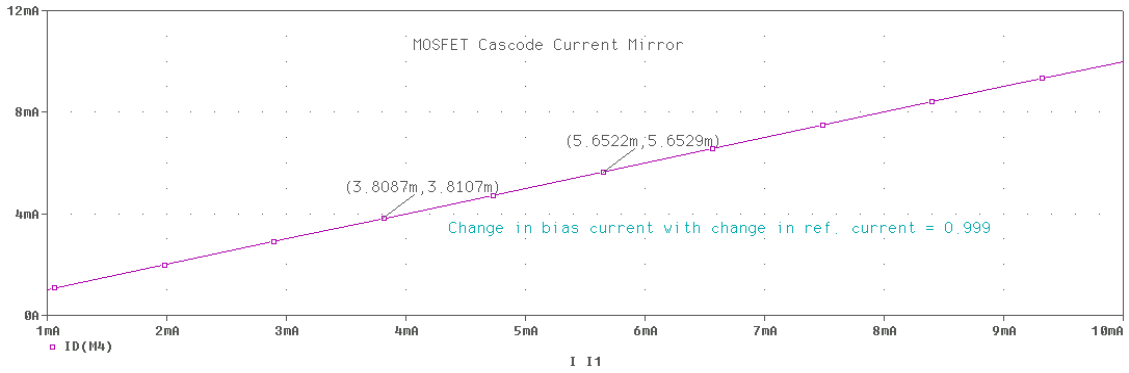
Fig 12.2 Schematic Diagram using PSPICE

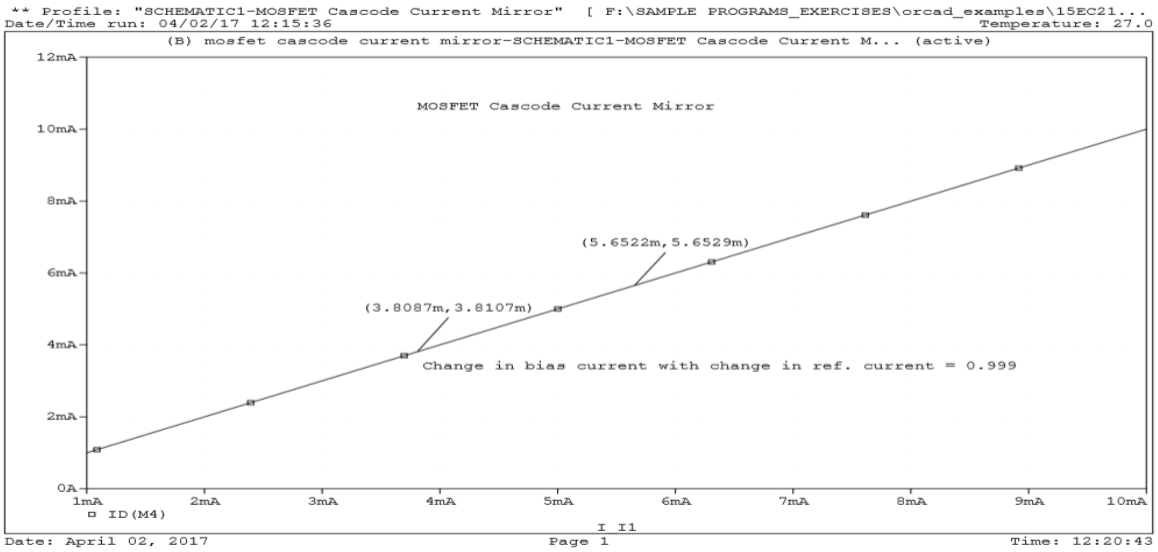
12.6 PROCEDURE

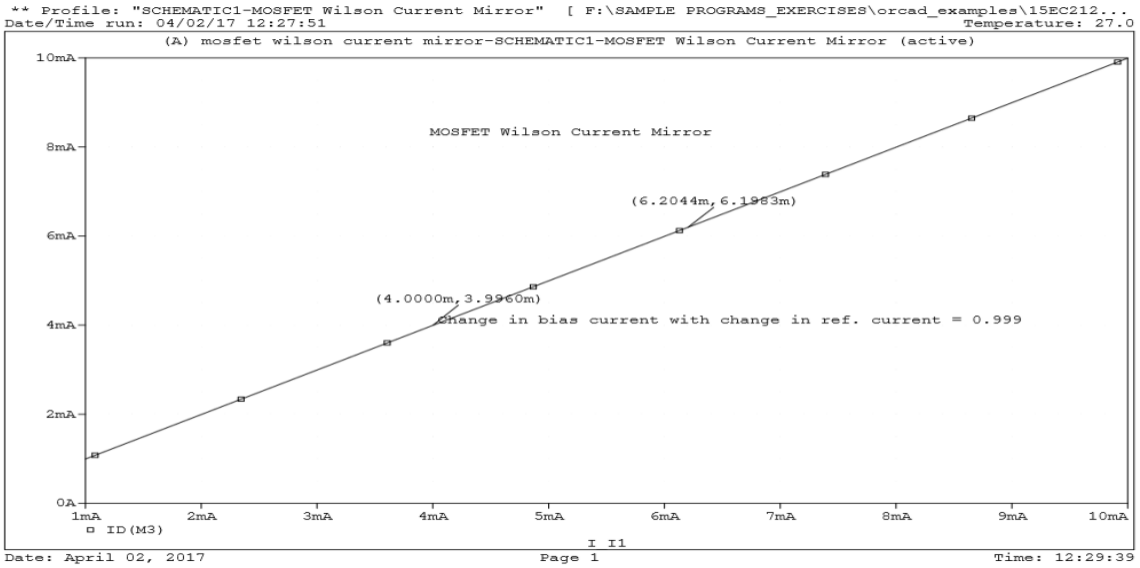
1. Open Capture Lite Edition.
2. Go to the File menu and select New Project. Select Analog or Mixed A/D
3. Create a blank project and then click OK.
4. Select ‘Place’ option from tool bar. Pick and place all the required circuit components by just clicking on the elements.
5. Connect the components as per circuit diagram using ‘place wire’ button that is available in tool bar.
6. Click on each components to give the parameter values as per design.Save the schematic.

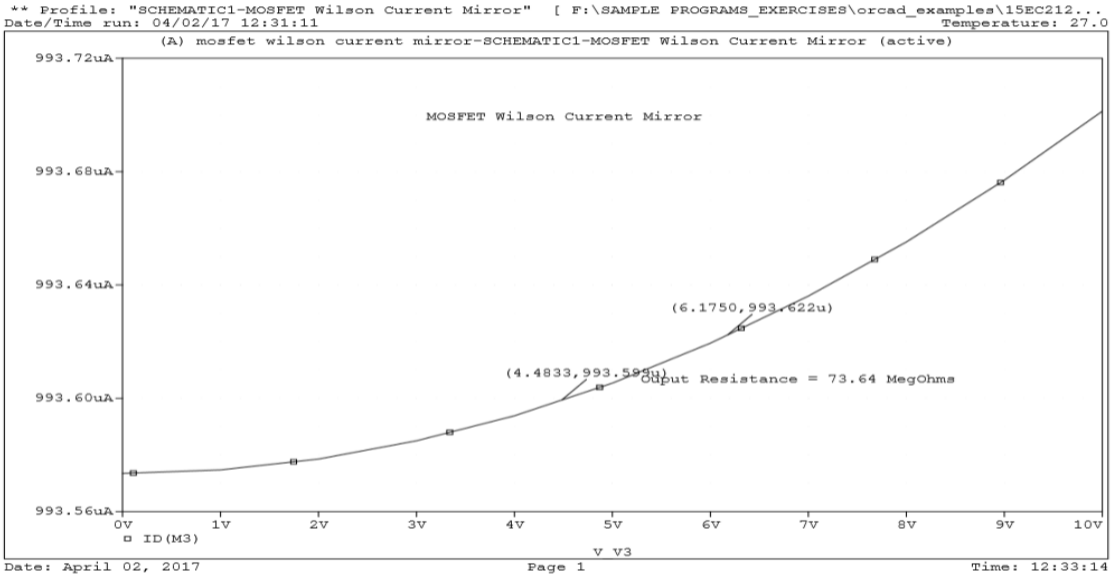
7. Create a new simulation profile. Mention the type of analysis and simulate the circuit.

12.7 PSPICE OUTPUT









12.8 .RESULTS:

Thus MOSFET common source amplifier with active load was designed and constructed using PSPICE.

13. SIMULATION EXPERIMENTS USING PSPICE- DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

13.1 OBJECTIVE

To simulate differential amplifer with active load using PSPICE and plot frequency response

13.2 SOFTWARE REQUIRED

PSPICE – OrCAD 9.2 lite

13.3 THEORY

The typical BJT differential pair amplifier consists of a pair of transistors coupled at the emitters to a current source, having equal resistances in each collector and equal, but opposite, signal sources in each base. The amplifier has several variations on this basic configuration. The basic configuration shown in Figure 1 will be studied in this experiment. The important characteristics for the differential pair amplifier to be studied in this experiment are: differential voltage gain A_{Vd}, common mode gain A_{Vcm}, common-mode rejection ration CMRR, and single-ended voltage gain A_{Vse}.

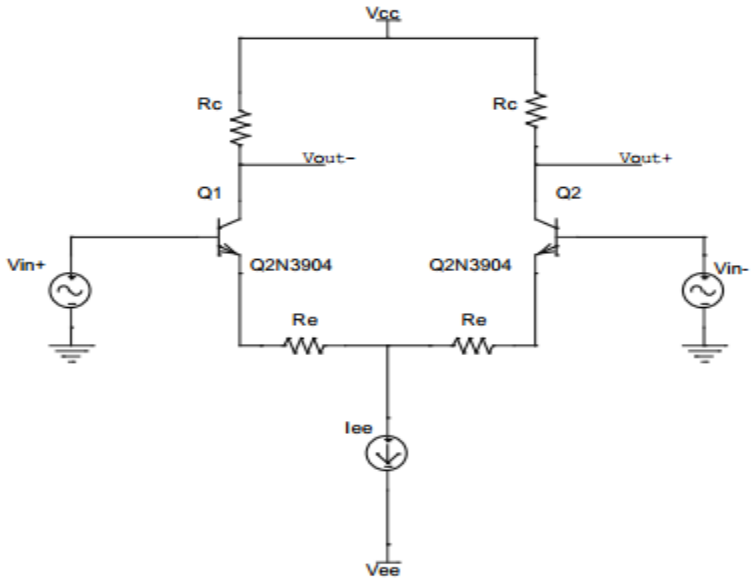


Fig 13.1 Basic BJT Differential Pair Amplifier

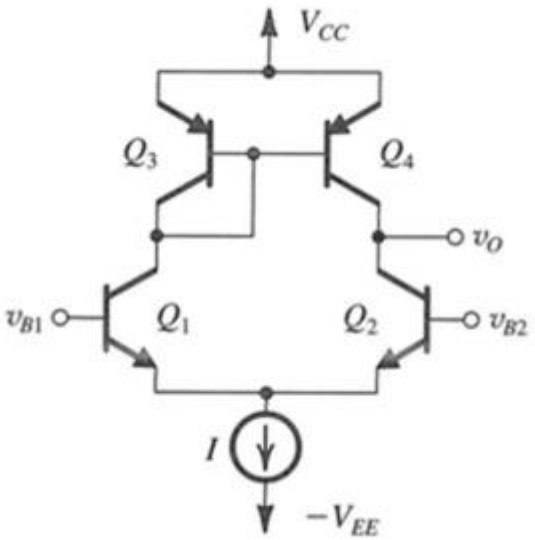


Fig 13.2BJT Differential Pair Amplifier with Active load

Assuming that $r_{o1,2} >> R_C$ and $r_{e1} = r_{e2}$, the following information can be found for thedifferential pair BJT amplifier:

$$V_{in} = V_{in}(+) + V_{in}(-)$$

$$V_{out}(-) = -i_{c1}R_c = -\alpha i_{e1}R_c \text{ and } V_{out}(+) = -i_{c2}R_c = -\alpha i_{c2}R_c$$

$$i_{e1} = \frac{V_{in}}{2r_{e1}+2R_e} \qquad \text{and} \qquad i_{e2} = \frac{V_{in}}{2r_{e2}+2R_e}$$

$$A_{Vd} = \frac{V_{out}(+) - V_{out}(-)}{V_{in}(+) - V_{in}(-)} = \frac{\alpha\left(\left(\frac{V_{in}}{2}\right)\frac{R_c}{r_e + R_e} - \left(-\left(\frac{V_{in}}{2}\right)\frac{R_c}{r_e + R_e}\right)\right)}{V_{in}} = \frac{\alpha R_c}{r_e + R_e}$$

Note: $V_{in}(+)$ and $V_{in}(-)$ are equal and opposite – and add together to make V_{in}.

The single-ended gain (output taken at either $V_{out(+)}$ or $V_{out(-)}$, is then:

$$A_{Vse} = \frac{V_{out}(+)}{V_{in}(-)} = \frac{V_{out}(-)}{V_{in}(+)} = \frac{1}{2} A_{Vd} = \frac{\alpha R_c}{2r_e + 2R_e}$$

Thse results are derived by looking at the output current i_c flowing through the resistorsR_c, its relati on to i_e, and finding the resultant voltage at the output terminals (in smallsignal terms). The common mode gain is found by applying the input signal to both the (+) and (-) inputs to the differential pair. The differential output voltage with a common mode input is zero since:

$$V_{out}(+) = V_{out}(-) = -V_{cm}\left(\frac{\alpha R_c}{r_e + R_e + 2r_{ee}}\right)$$

and

$$A_{Vcmd} = V_{out}(+) - V_{out}(-) = 0$$

However, the single-ended common-mode voltage gain is not zero and is given by:

$$A_{Vcmse} = \frac{V_{out}(+)}{V_{cm}} = \frac{V_{out}(-)}{V_{cm}} = \frac{-\alpha R_c}{r_e + R_e + 2r_{ee}}$$

*Note: The term $2r_{ee}$ is derived from the resistance of the current source i_{ee} which is ideally infinity, but in practical circuits is not infinitely high.

The common-mode rejection ratio is defined by the division of the single-ended differential circuit gain by the single-ended common-mode gain as follow

$$CMRR = \frac{A_{Vdse}}{A_{Vcmse}} = \frac{\frac{\alpha R_c}{2r_e + 2R_e}}{\frac{\alpha R_c}{r_e + R_e + 2r_{ee}}} = \frac{r_e + R_e + 2r_{ee}}{2r_e + 2R_e} \approx \frac{r_{ee}}{r_e + R_e} \text{ since } r_{ee} >> r_e + R_e$$

From the above equations it can be seen that the differential amplifier enhances the difference between the inputs and suppresses the common mode component. This desirable characteristic is used to attenuate unwanted presences in the input signal such as noise from a coaxial cable or from an audio cable. Differential amplifiers often make use of active loads: a current mirror circuit to establish collector currents between the two transistors, rather than load resistors.What does the current mirror “look like” to the common-emitter side of the differential amplifier circuit, when we apply the Superposition theorem? What aspect of the differential amplifier’s performance is primarily enhanced with the addition of the current mirror to the primarily enhanced with the addition of the current mirror to the circuit?

Adding a current mirror greatly increases the effective resistance on the collector terminal of the common-emitter side, and so greatly increases the amplifier's differential voltage gain.
Notes: Ask your students to explain why the differential voltage gain increases. One hint is the internal (Norton) resistance of an ideal current source: infinite ohms! Ask your students how this equivalent resistance compares to the (finite) values of the resistors replaced by the current mirror, and what impact that change has on voltage gain.

6.4 PROCEDURE

1. Open Capture Lite Edition.
2. Go to the File menu and select New Project. Select Analog or Mixed A/D
3. Create a blank project and then click OK.
4. Select 'Place' option from tool bar. Pick and place all the required circuit components by just clicking on the elements.
5. Connect the components as per circuit diagram using 'place wire' button that is available in tool bar.
6. Click on each components to give the parameter values as per design. Save the schematic.
7. Create a new simulation profile. Mention the type of analysis and simulate the circuit.
8. Measure the voltages and currents at different points and tabulate the readings.

13.5 PSPICE OUTPUT

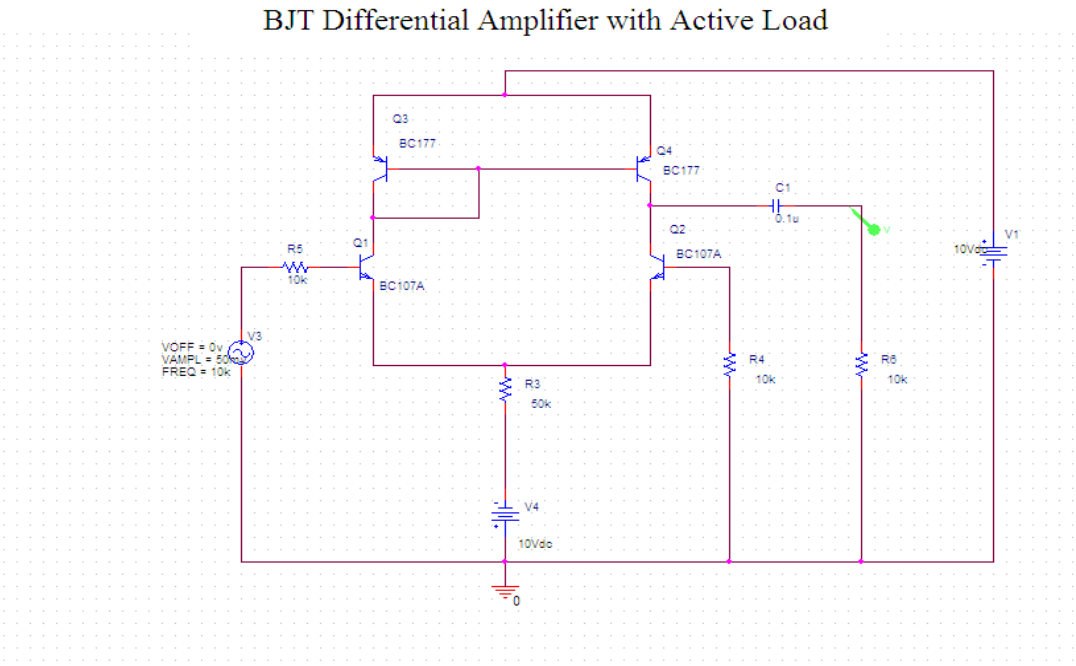


Fig 13.3 Schematic Diagram using PSPICE

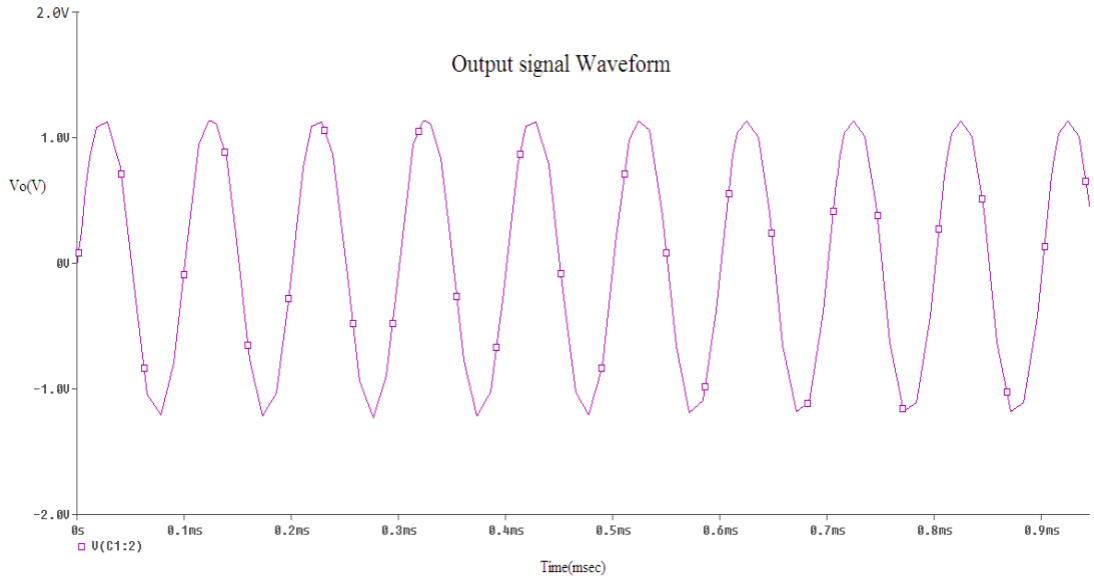


Fig 13.4 Output Waveform

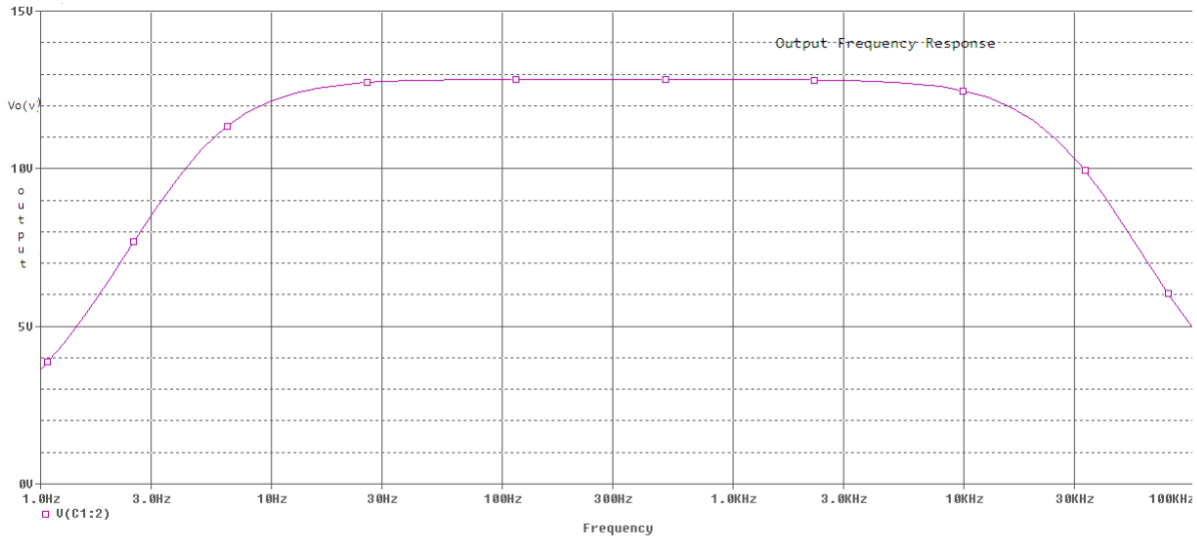


Fig 13.5 Output frequency response plot

13.6 TABULATION

V_i = _____ mV

S.No	V_o(volts)	Gain=V_o/V_i	Gain in dB

13.7 PRELAB QUESTIONS

1. What is differential amplifier?
2. Define differential mode gain?
3. Define common mode gain?
4. Define CMRR?
5. What are the applications of differential amplifier?
6. What are the classifications of differential amplifier?

13.8 POSTLAB QUESTIONS

1. What active load?
2. What is the advantage of active load in differential amplifier?
3. Summarize the formula for differential input resistance,transcoductance,differential gain for frequency single ended balanced output differential amplifier?
4. Is it possible to change time period of the waveform without changing R & C?

13.9 RESULT:

Thus differential amplifier with active load was designed and constructed using PSPICE.

APPENDIX