

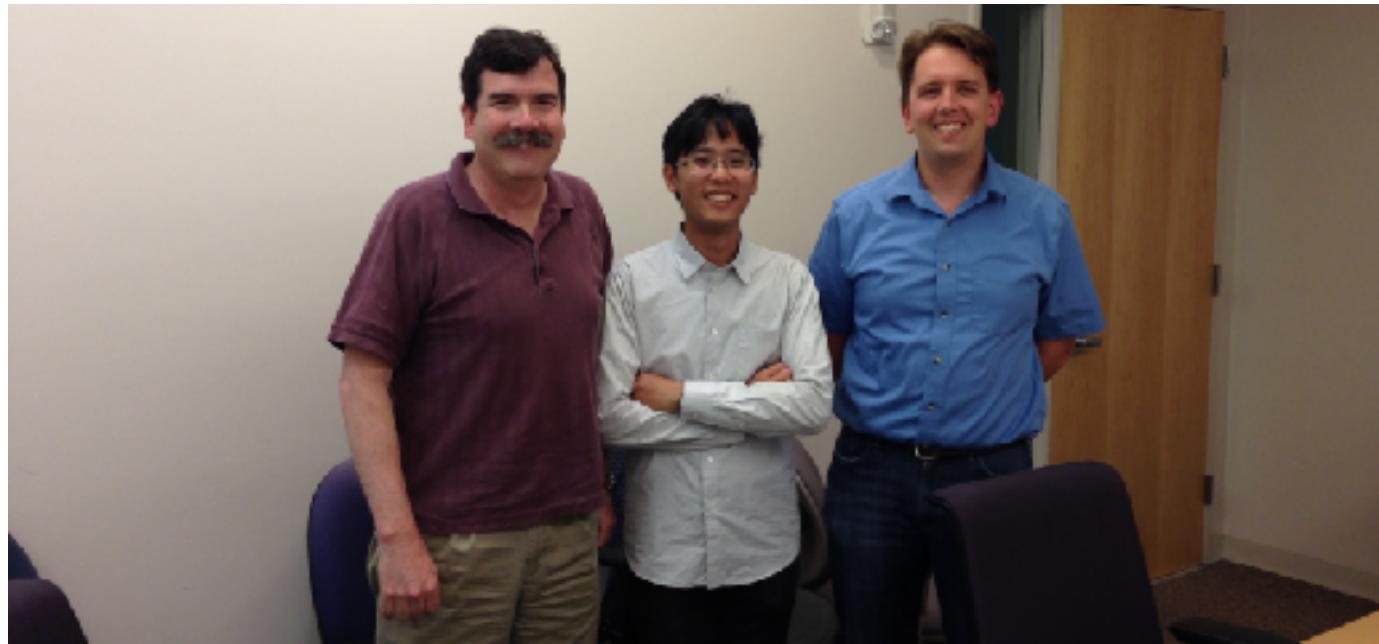
Multithreaded Architectures and Programming on Multithreaded Architectures

Hung-Wei Tseng

Outline

- Multithreaded processors
- Programming multithreaded processors & necessary architectural support

Simultaneous multithreading



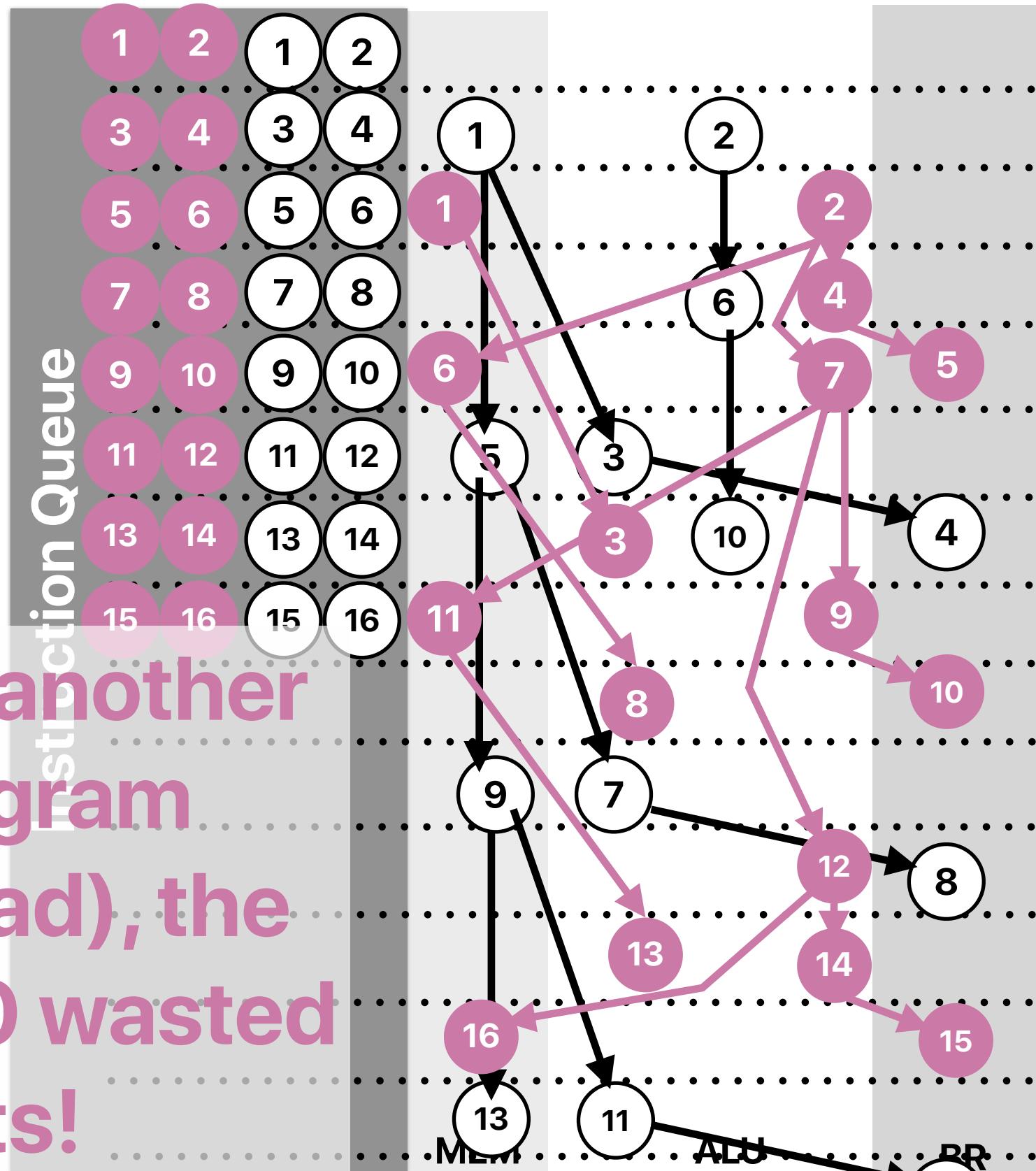
Simultaneous multithreading

- Invented by Dean Tullsen (Now a professor at **UCSD CSE**)
- The processor can schedule instructions from different threads/processes/programs
- Fetch instructions from different threads/processes to fill the not utilized part of pipeline
 - Exploit “thread level parallelism” (TLP) to solve the problem of insufficient ILP in a single thread
 - You need to create an illusion of multiple processors for OSs

Concept: Simultaneous Multithreading (SMT)

① movq 8(%rdi), %rdi
② addl \$1, %eax
③ testq %rdi, %rdi
④ jne .L3
⑤ movq 8(%rdi), %rdi
⑥ addl \$1, %eax
⑦ testq %rdi, %rdi
⑧ jne .L3
⑨ movq 8(%rdi), %rdi
⑩ addl \$1, %eax
⑪ testq %rdi, %rdi
⑫ jne .L3

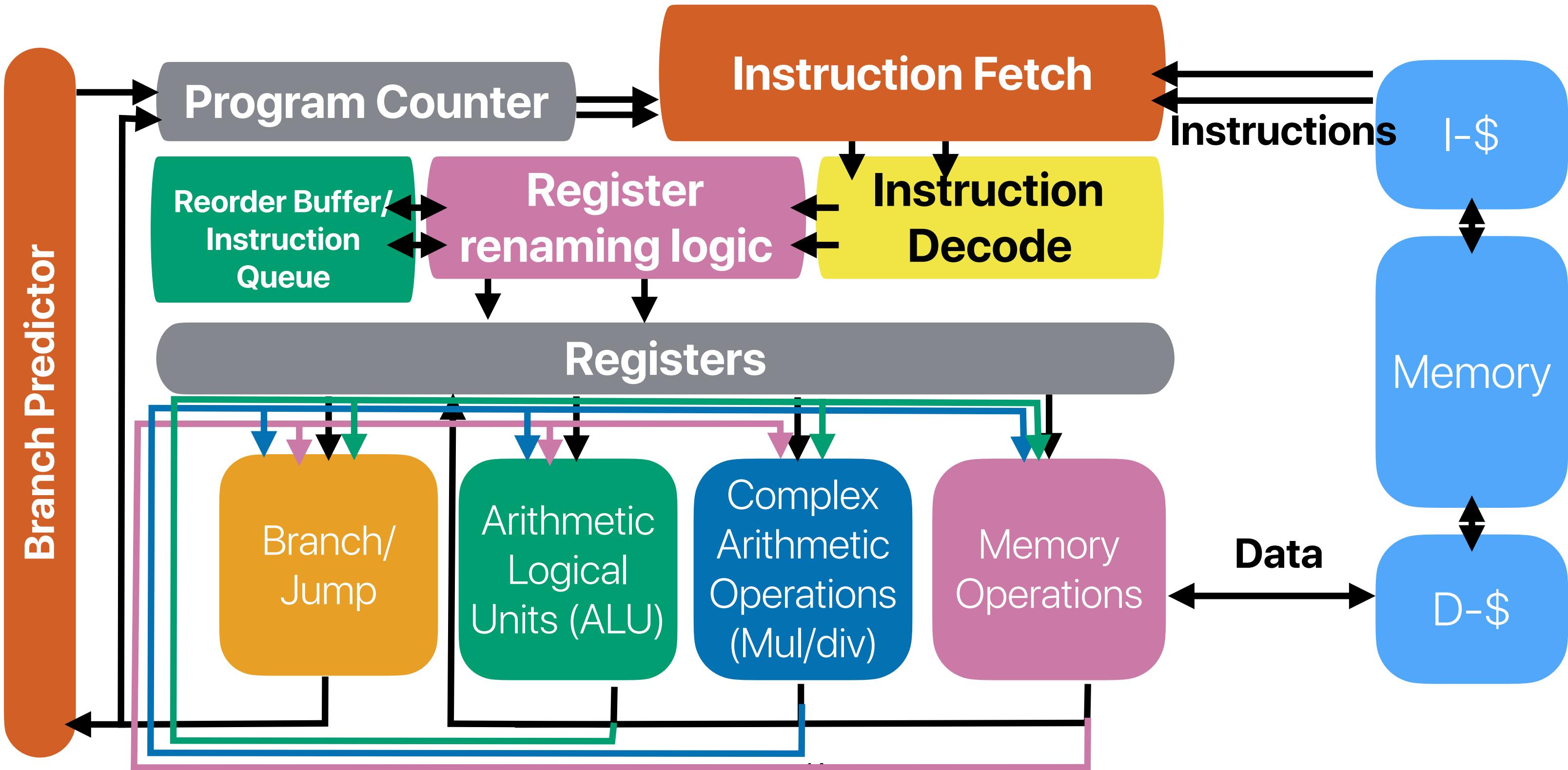
By scheduling another running program instance (thread), the processor has 0 wasted issue slots!



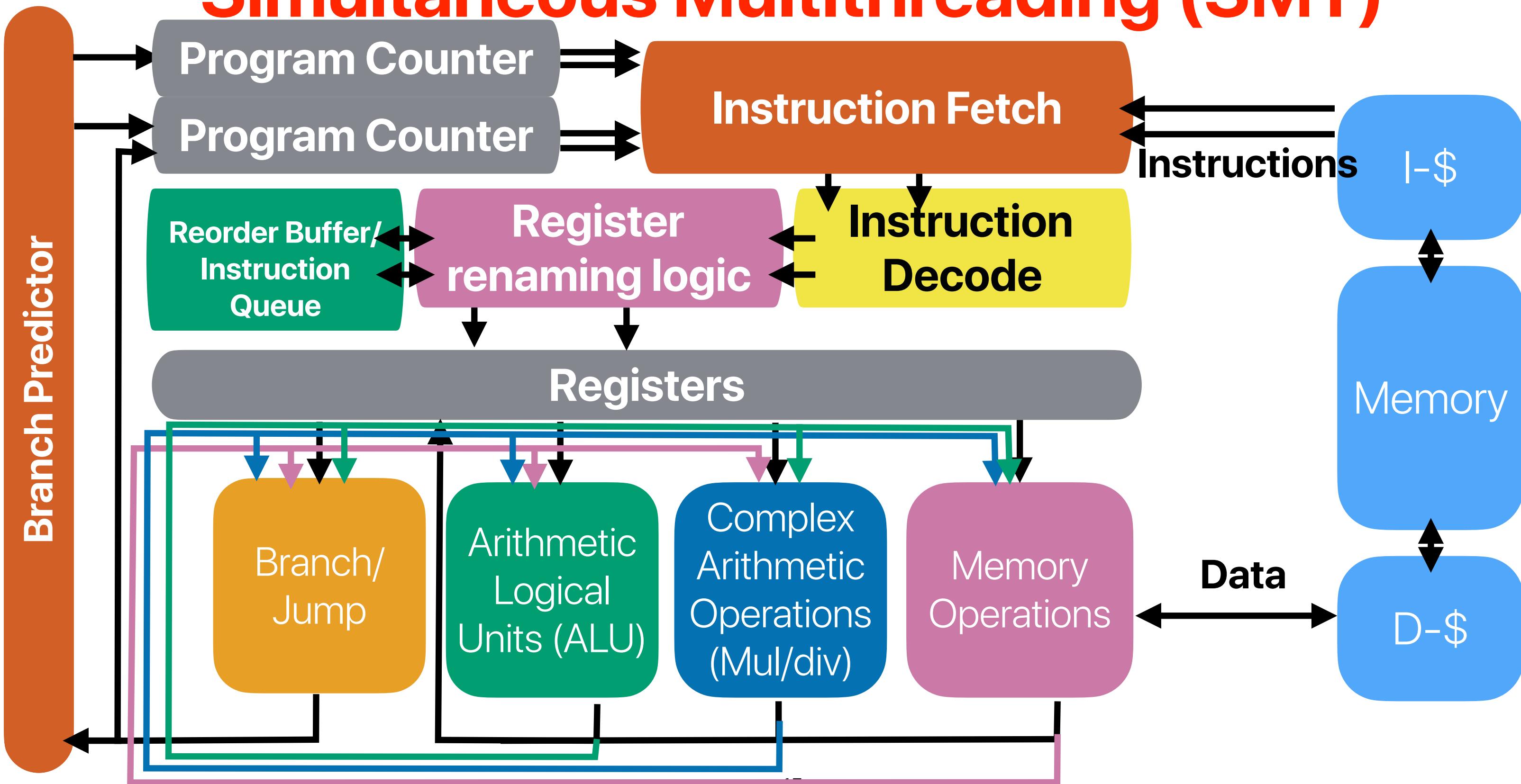
How do we support two running programs in one pipeline?

- We need two program counters
- We need two sets of architectural to physical register mappings
- We do not need
 - Duplicated cache — virtually indexed, physically tagged cache already addressed that
 - Duplicated pipeline functional units — isn't sharing the whole purpose?
 - Duplicated reorder buffer — you simply need to tag which process the instruction belongs to

Recap: Register renaming



Simultaneous Multithreading (SMT)



SMT from the user/OS' perspective





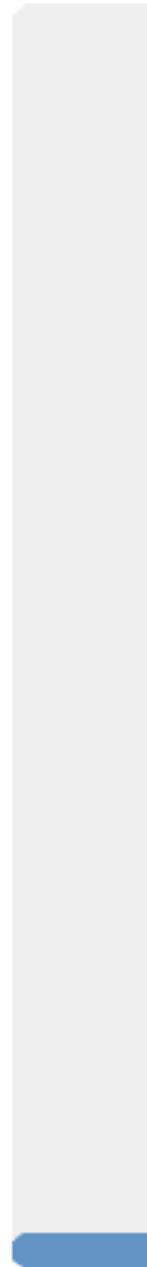
Pros/Cons of SMT

- How many of the following statements about SMT is/are correct?
 - ① SMT makes processors with deep pipelines more tolerable to mis-predicted branches
 - ② SMT can improve the throughput of a single-threaded application
 - ③ SMT processors can better utilize hardware during cache misses comparing with superscalar processors with the same issue width
 - ④ SMT processors can have higher cache miss rates comparing with superscalar processors with the same cache sizes when executing the same set of applications.

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B. 1
C. 2
D. 3
E. 4

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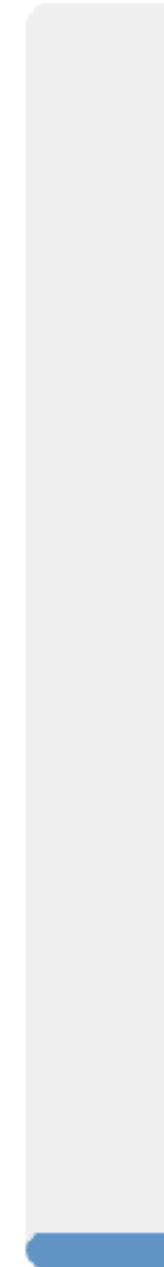
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A

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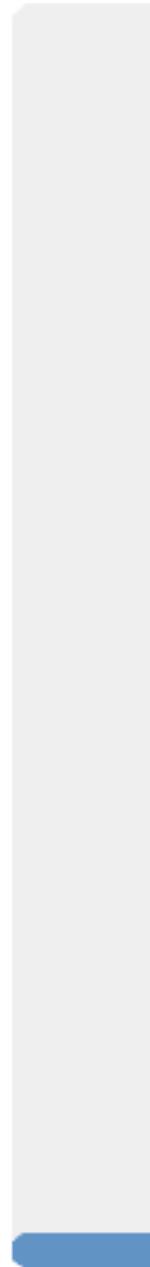
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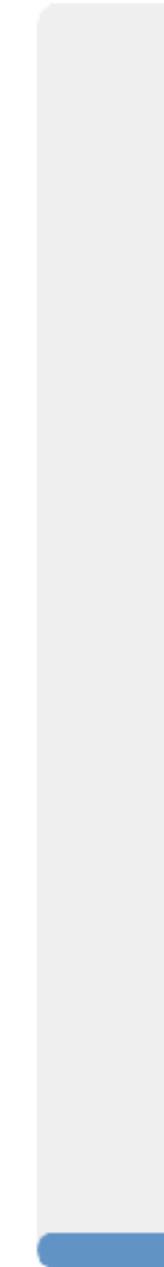
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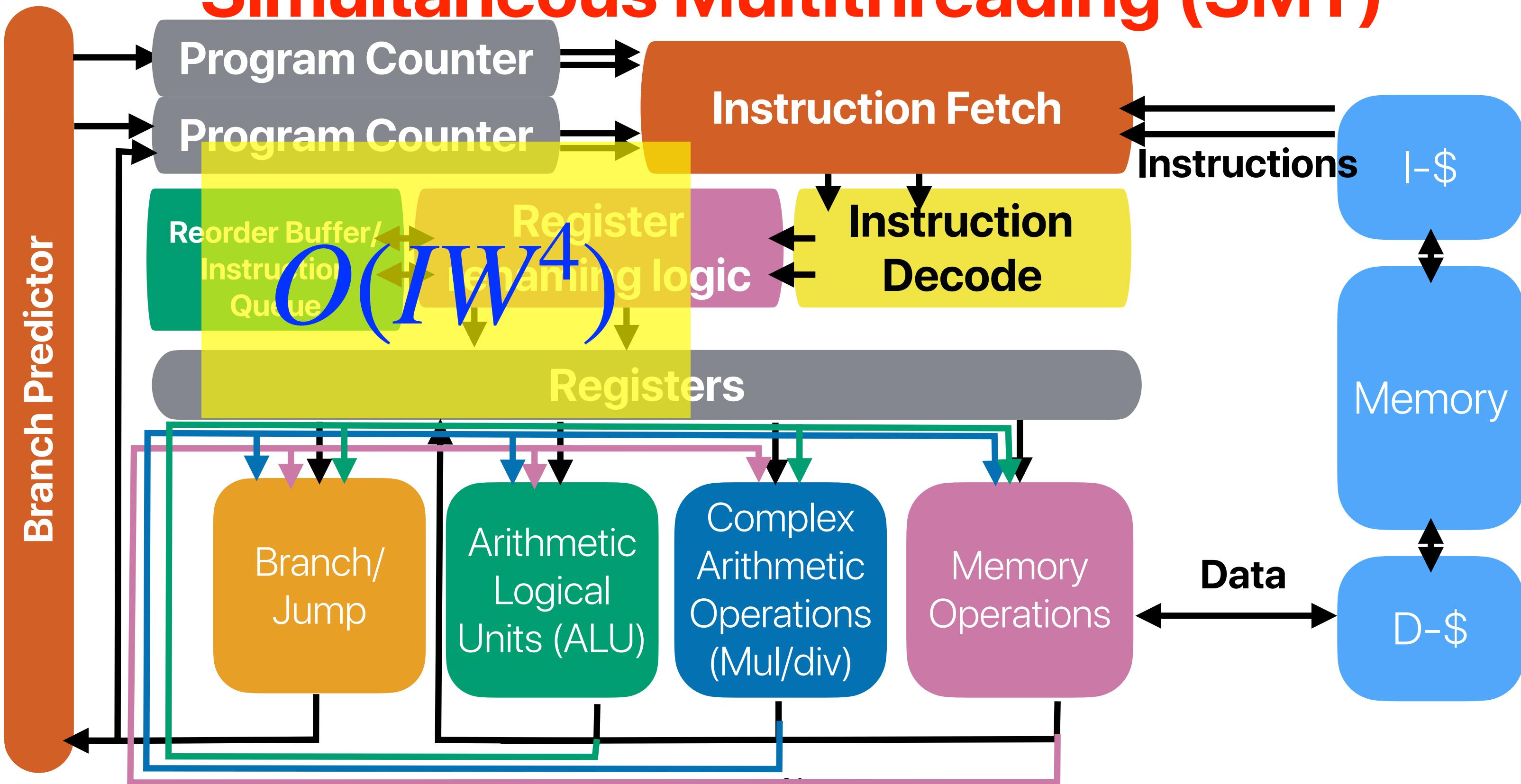
E

SMT

- Improve the throughput of execution
 - May increase the latency of a single thread
- Less branch penalty per thread
- Increase hardware utilization
- Simple hardware design: Only need to duplicate PC/Register Files
- Real Case:
 - Intel HyperThreading (supports up to two threads per core)
 - Intel Pentium 4, Intel Atom, Intel Core i7
 - AMD RyZen (Zen microarchitecture)
 - If you see a processor with “threads” more than “cores”, that must be because of SMT!

Architecture:	x86_64
CPU op-mode(s):	32-bit, 64-bit
Byte Order:	Little Endian
Address sizes:	39 bits physical, 48 bits virtual
CPU(s):	8
On-line CPU(s) list:	0-7
Thread(s) per core:	2
Core(s) per socket:	4
Socket(s):	1
NUMA node(s):	1
Vendor ID:	GenuineIntel
CPU family:	6
Model:	151
Model name:	12th Gen Intel(R) Core(TM) i3-12100F
Stepping:	5
CPU MHz:	3300.000
CPU max MHz:	5500.0000
CPU min MHz:	800.0000
BogoMIPS:	6604.80
Virtualization:	VT-x
L1d cache:	192 KiB
L1i cache:	128 KiB

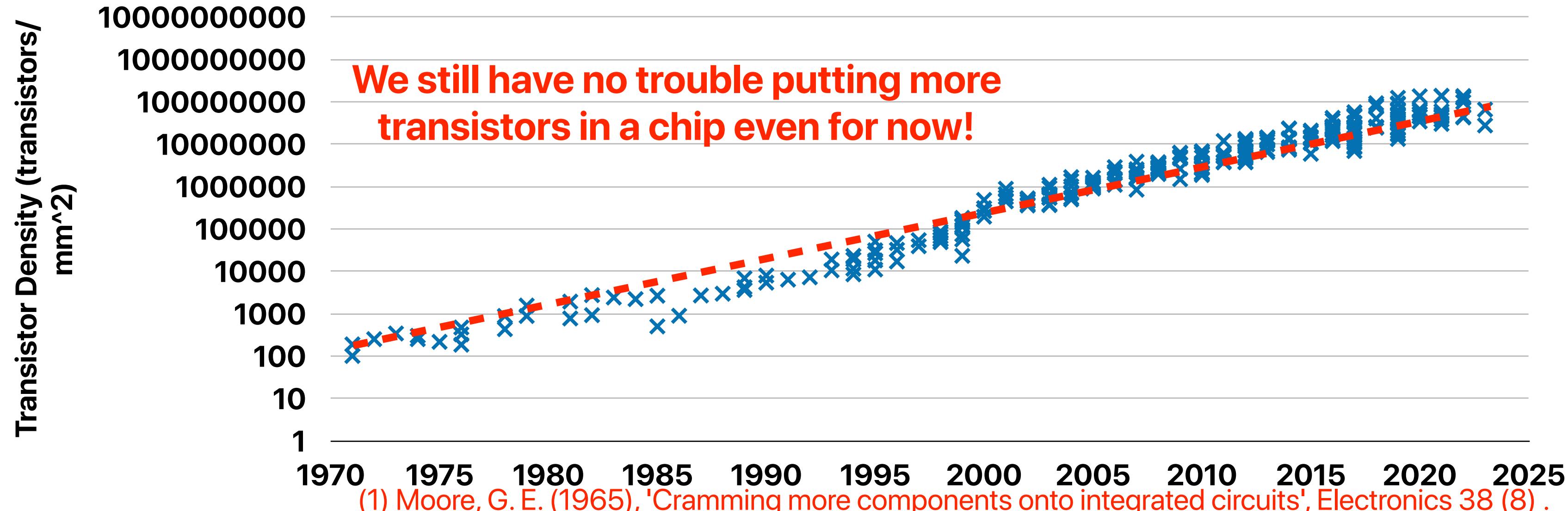
Simultaneous Multithreading (SMT)



Chip-Multiprocessors (CMP) or Multi-core processors

Recap: Moore's Law⁽¹⁾

- The number of transistors we can build in a fixed area of silicon doubles every 12 ~ 24 months.
- Moore's Law "was" the most important driver for historic CPU performance gains



Transistor counts

Microarchitecture	Transistor Count	Issue-width	Year
Alder Lake	325 M	5x ALU, 7x Memory	2021
Coffee Lake	217 M	4x ALU, 4x Memory	2017
Sandy Bridge	290 M	3x ALU, 3x Memory	2011
Nehalem	182.75 M	3x ALU, 3x Memory	2008



How many transistors per core on Coffee Lake?



The Coffee Lake processor has 217 million transistors per core. It is manufactured using Intel's second 14 nm process. The Coffee Lake processors introduced i5 and i7 CPUs featuring six cores (along with hyper-threading in the case of the later models) and no hyperthreading.



The transistor count per core on Coffee Lake is lower than that of some other modern processors, such as the Ryzen 5 5600X which has 390 million transistors per core. However, Coffee Lake still offers good performance, thanks to its high clock speeds and efficient power delivery.

Here is a table of the transistor counts per core for some other modern processors:

Processor	Transistors per core
Coffee Lake	217 million
Ryzen 5 5600X	390 million
Core i7 12700K	425.8 million

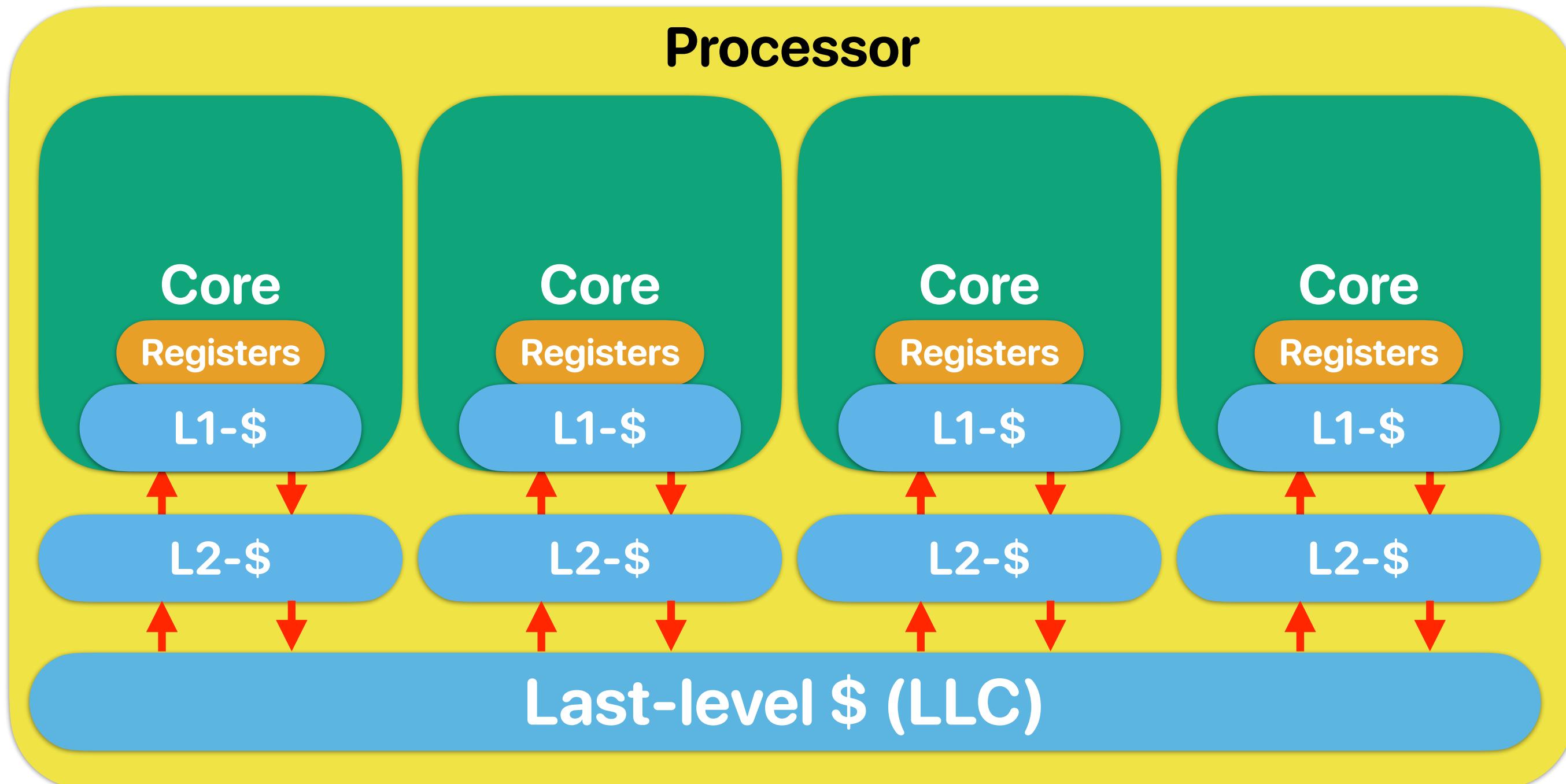
2x 3-issue ALUs Nehalem

Nehalem Alder Lake Nehalem
6-issue 12-issue 6-issue

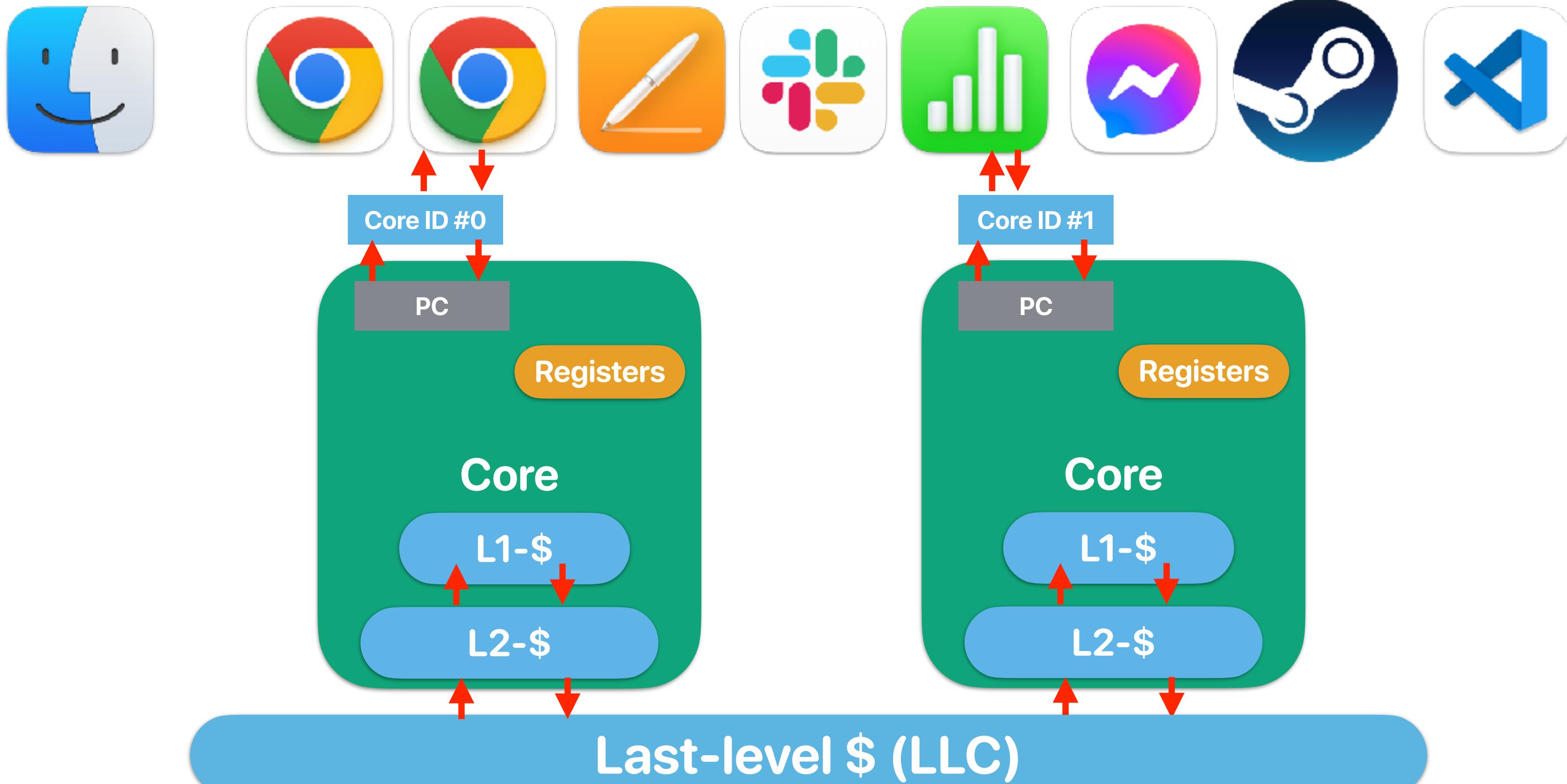
1x 5-issue ALUs Alder Lake

Based on https://en.wikipedia.org/wiki/Transistor_count

Concept of CMP



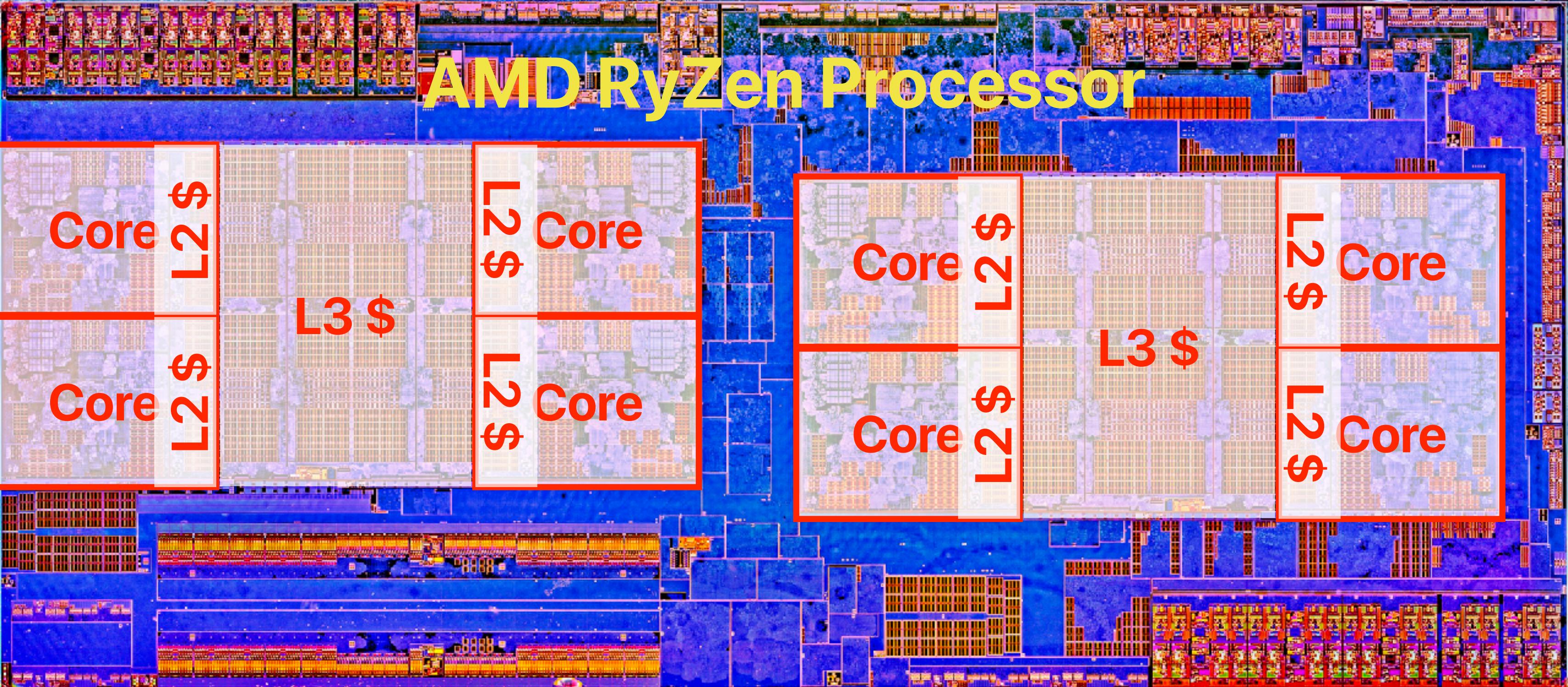
CMP from the user/OS' perspective



Modern processors have both CMP/SMT



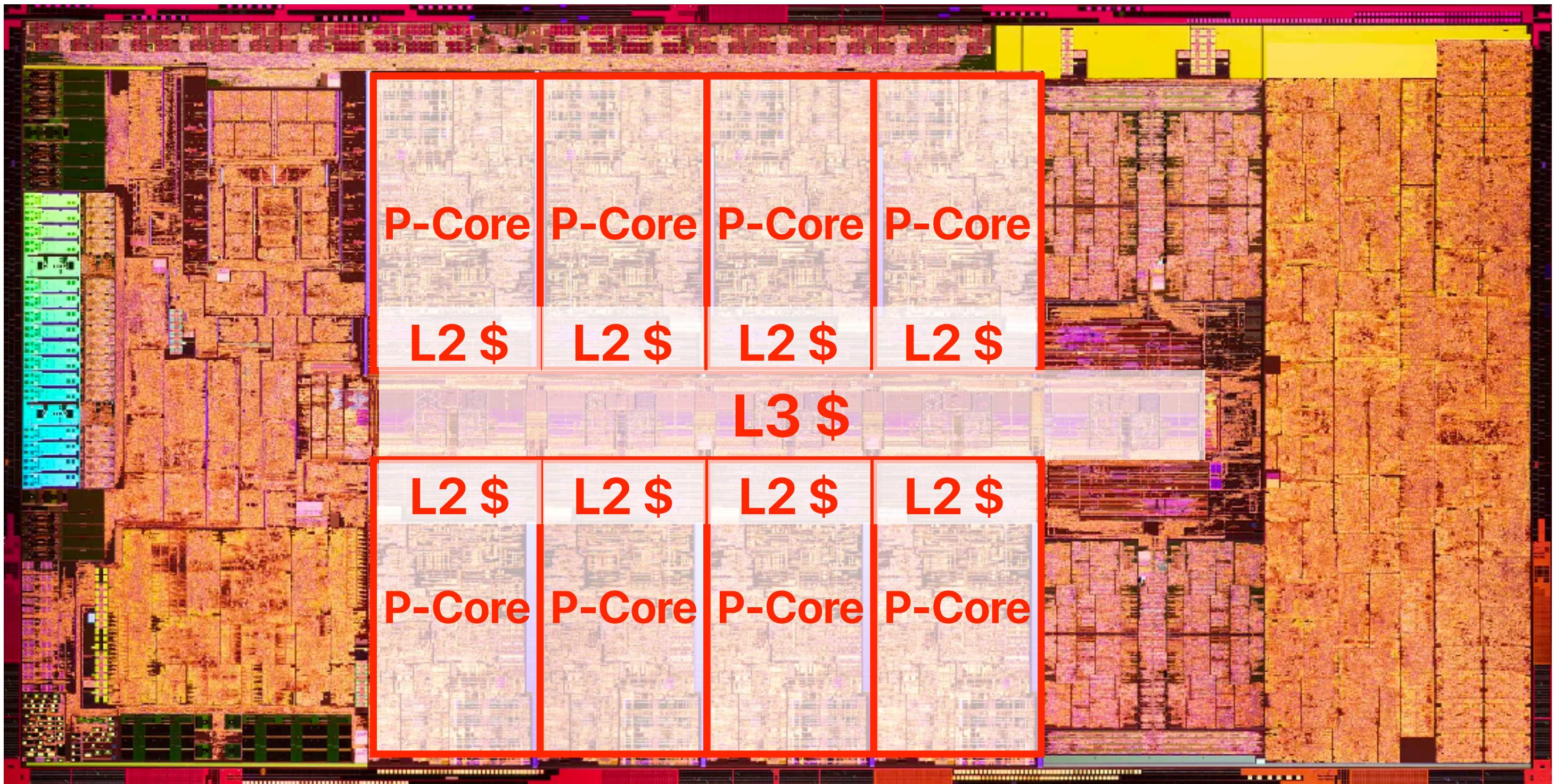
AMD Ryzen Processor



AMD

RYZEN

Intel Alder Lake



SMT v.s. CMP

- An SMT processor is basically a SuperScalar processor with multiple instruction front-end. Assume within the same chip area, we can build an SMT processor supporting 4 threads, with 6-issue pipeline, 64KB cache or — a CMP with 4x 2-issue pipeline & 16KB cache in each core. Please identify how many of the following statements are/is correct when running programs on these processors.
 - ① If we are just running one program in the system, the program will perform better on an SMT processor — **you have more resources for the program**
 - ② If we are running 4 applications simultaneously, the cache miss rates will be higher in the SMT processor
 - ③ If we are running 4 applications simultaneously, the branch mis-prediction will be higher in the SMT processor — **it depends!**
 - ④ If we are running one program with 4 parallel threads, the cache miss rates will be higher in the SMT processor — **it depends!**
 - ⑤ If we are running one program with 4 parallel threads simultaneously, the branch mis-prediction will be longer in the SMT processor — **it depends!**

A. 1 **There is no clear win on each — why not having both?**

B. 2

C. 3

D. 4 **The only thing we know for sure — if we don't parallel the program, it won't get any faster on CMP**

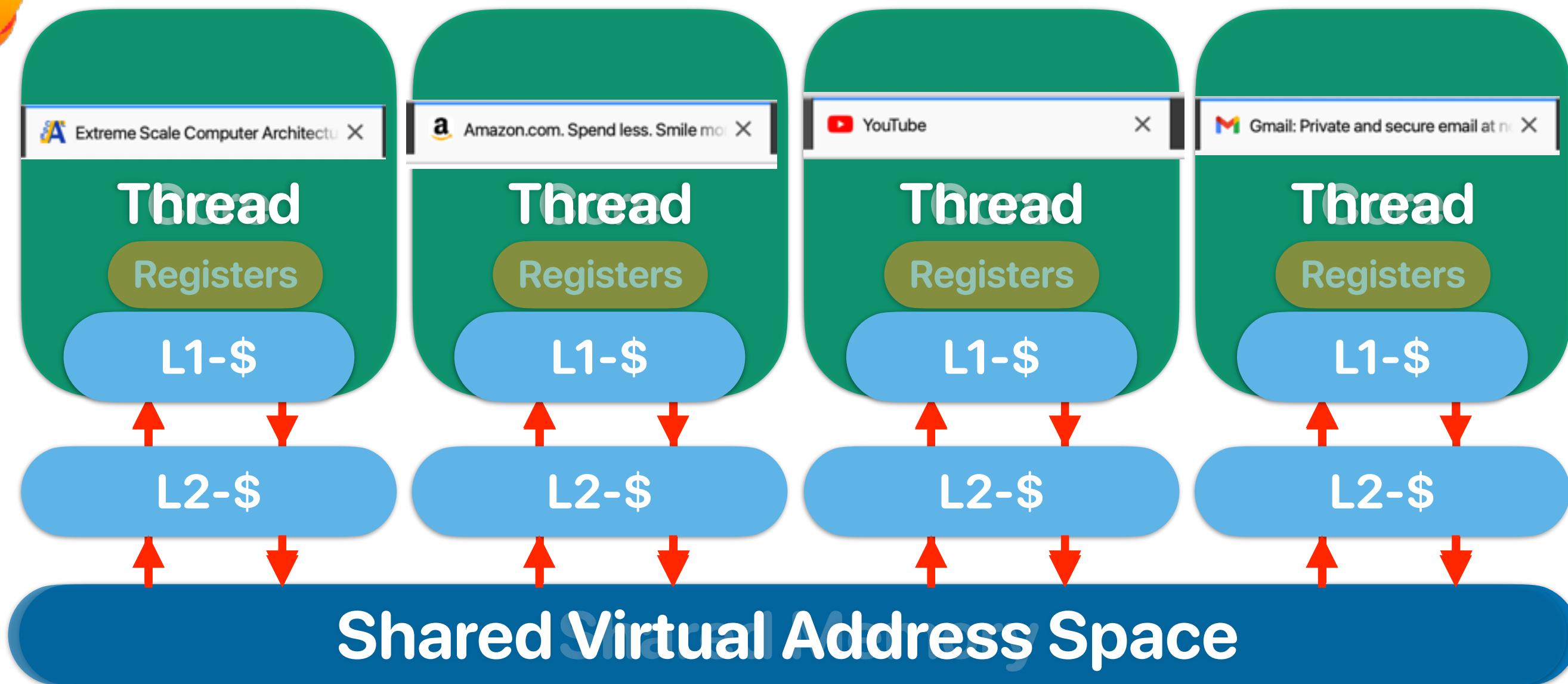
E. 5

Parallel Programming & Architectural Supports for Parallel Programming

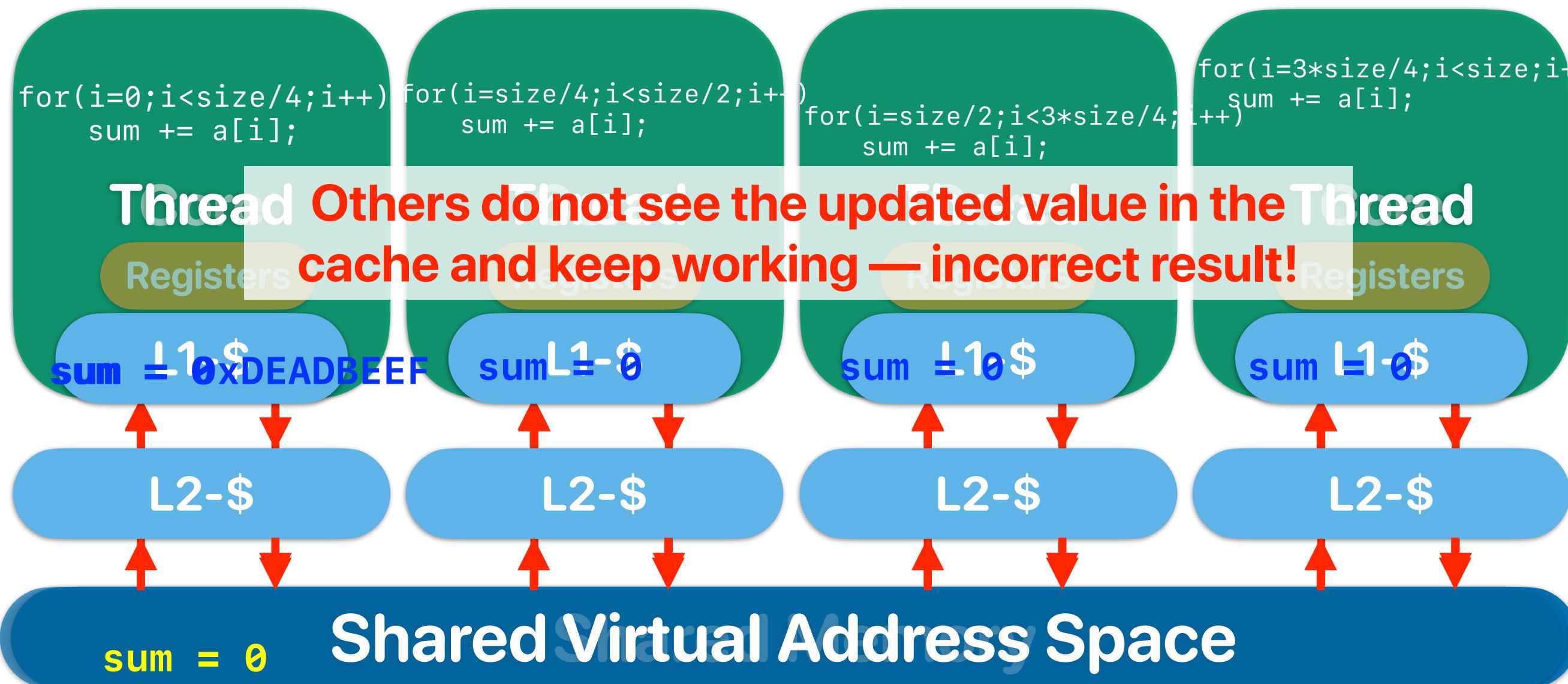
Parallel programming

- To exploit parallelism you need to break your computation into multiple “processes” or multiple “threads”
- Processes (in OS/software systems)
 - Separate programs actually running (not sitting idle) on your computer at the same time.
 - Each process will have its own virtual memory space and you need explicitly exchange data using inter-process communication APIs
- Threads (in OS/software systems)
 - Independent portions of your program that can run in parallel
 - All threads share the same virtual memory space
- We will refer to these collectively as “threads”
 - A typical user system might have 1-8 actively running threads.
 - Servers can have more if needed (the sysadmins will hopefully configure it that way)

What software thinks about “multiprogramming” hardware



What software thinks about “multiprogramming” hardware



Coherency & Consistency

- Coherency — Guarantees all processors see the same value for a variable/memory address in the system when the processors need the value at the same time
 - What value should be seen
- Consistency — All threads see the change of data in the same order
 - When the memory operation should be done

Simple cache coherency protocol

- Snooping protocol
 - Each processor broadcasts / listens to cache misses
- State associate with each block (cacheline)
 - Invalid
 - The data in the current block is invalid
 - Shared
 - The processor can read the data
 - The data may also exist on other processors
 - Exclusive
 - The processor has full permission on the data
 - The processor is the only one that has up-to-date data

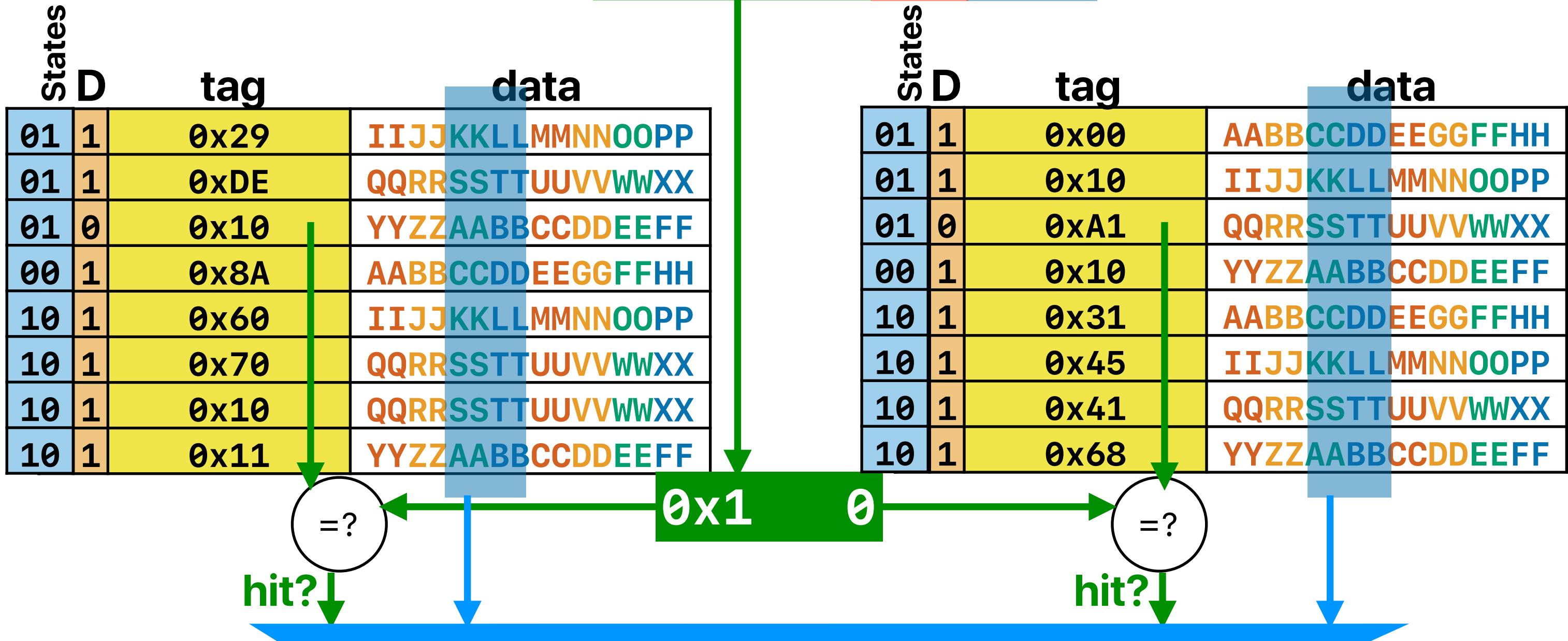
Coherent way-associative cache

memory address:

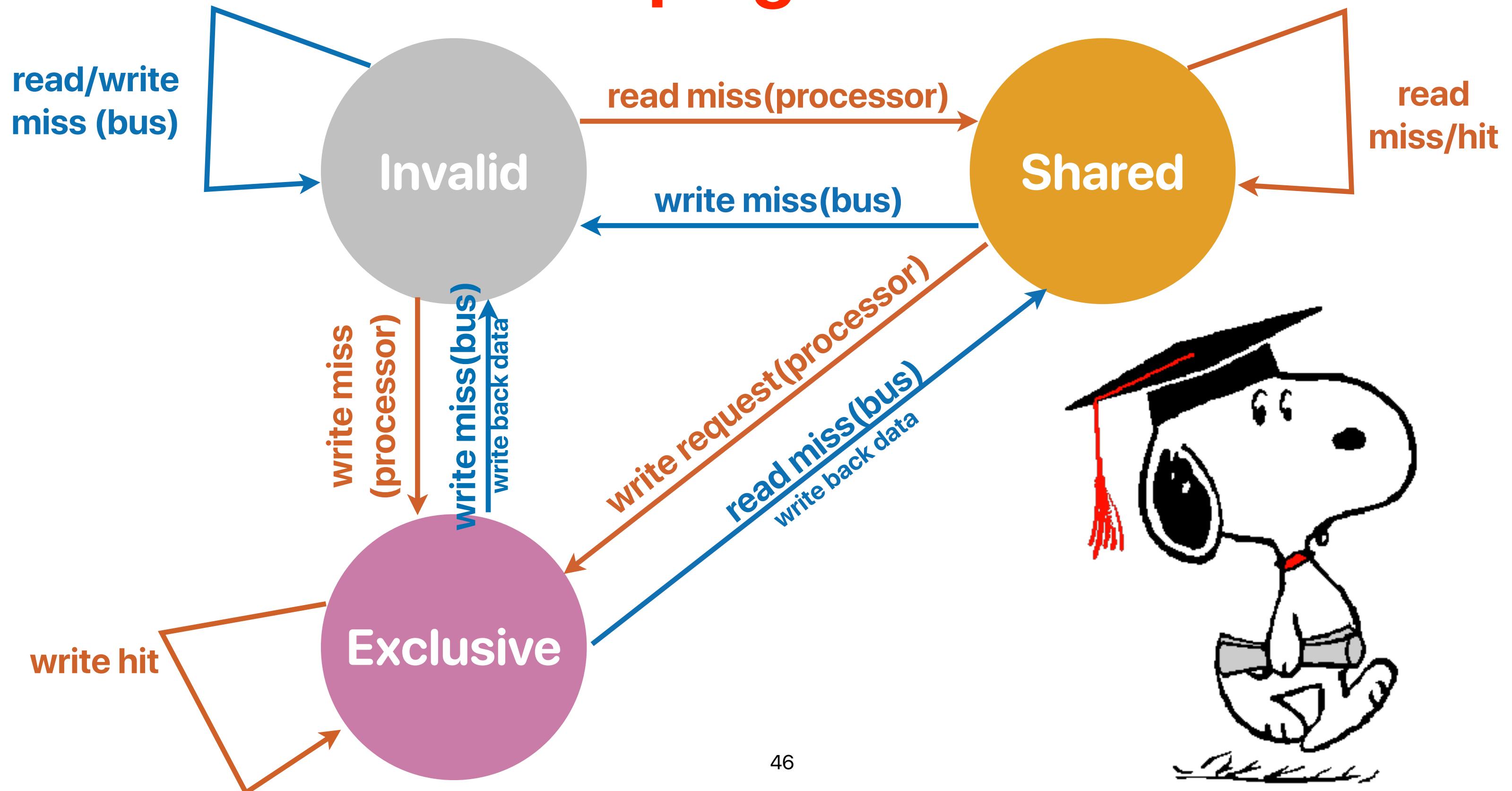
$0x0$ 8 tag 2 set 4 block
index offset

memory address:

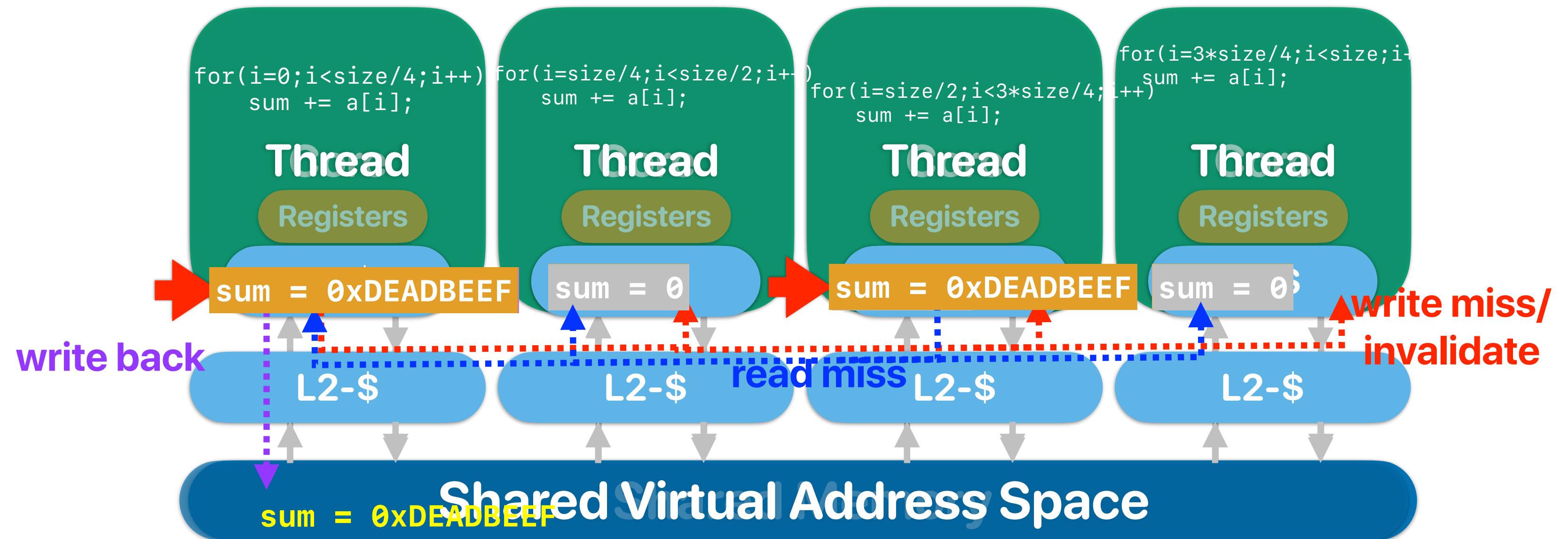
0b0000100000100100



Snooping Protocol



What happens when we write in coherent caches?



Observer

thread 1	thread 2
<pre>int loop; int main() { pthread_t thread; loop = 1; pthread_create(&thread, NULL, modifyloop, NULL); while(loop == 1) { continue; } pthread_join(thread, NULL); fprintf(stderr,"User input: %d\n", loop); return 0; }</pre>	<pre>void* modifyloop(void *x) { sleep(1); printf("Please input a number:\n"); scanf("%d",&loop); return NULL; }</pre>

Observer

prevents the compiler from putting the variable "loop" in the "register"

thread 1

```
volatile int loop;

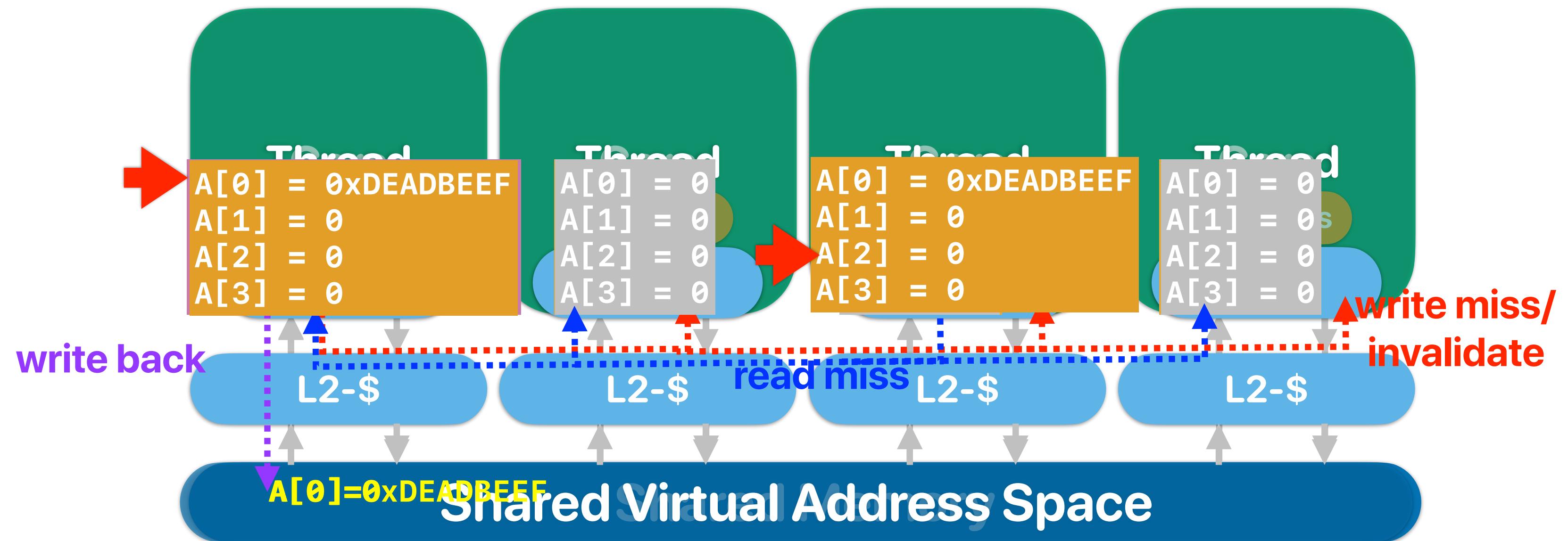
int main()
{
    pthread_t thread;
    loop = 1;

    pthread_create(&thread, NULL, modifyloop,
NULL);
    while(loop == 1)
    {
        continue;
    }
    pthread_join(thread, NULL);
    fprintf(stderr,"User input: %d\n", loop);
    return 0;
}
```

thread 2

```
void* modifyloop(void *x)
{
    sleep(1);
    printf("Please input a number:\n");
    scanf("%d",&loop);
    return NULL;
}
```

Cache coherency



L v.s. R

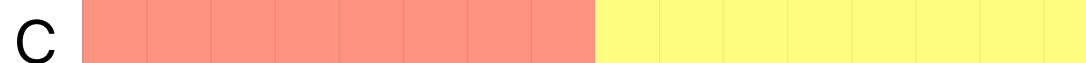
Version L

```
void *threaded_vadd(void *thread_id)
{
    int tid = *(int *)thread_id;
    int i;
    for(i=tid;i<ARRAY_SIZE;i+=NUM_OF_THREADS)
    {
        c[i] = a[i] + b[i];
    }
    return NULL;
}
```



Version R

```
void *threaded_vadd(void *thread_id)
{
    int tid = *(int *)thread_id;
    int i;
    for(i=tid*(ARRAY_SIZE/NUM_OF_THREADS);i<(tid+1)*(ARRAY_SIZE/NUM_OF_THREADS);i++)
    {
        c[i] = a[i] + b[i];
    }
    return NULL;
}
```



4Cs of cache misses

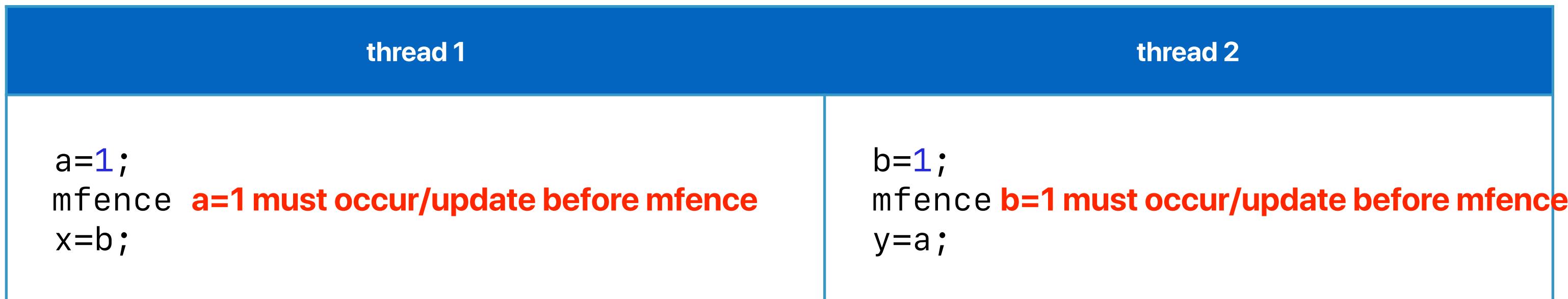
- 3Cs:
 - Compulsory, Conflict, Capacity
- Coherency miss:
 - A “block” invalidated because of the sharing among processors.

False sharing

- True sharing
 - Processor A modifies X, processor B also want to access X.
- False sharing
 - Processor A modifies X, processor B also want to access Y. However, Y is invalidated because X and Y are in the same block!

fence instructions

- x86 provides an “mfence” instruction to prevent reordering across the fence instruction
 - All updates prior to mfence must finish before the instruction can proceed
- x86 only supports this kind of “relaxed consistency” model. You still have to be careful enough to make sure that your code behaves as you expected



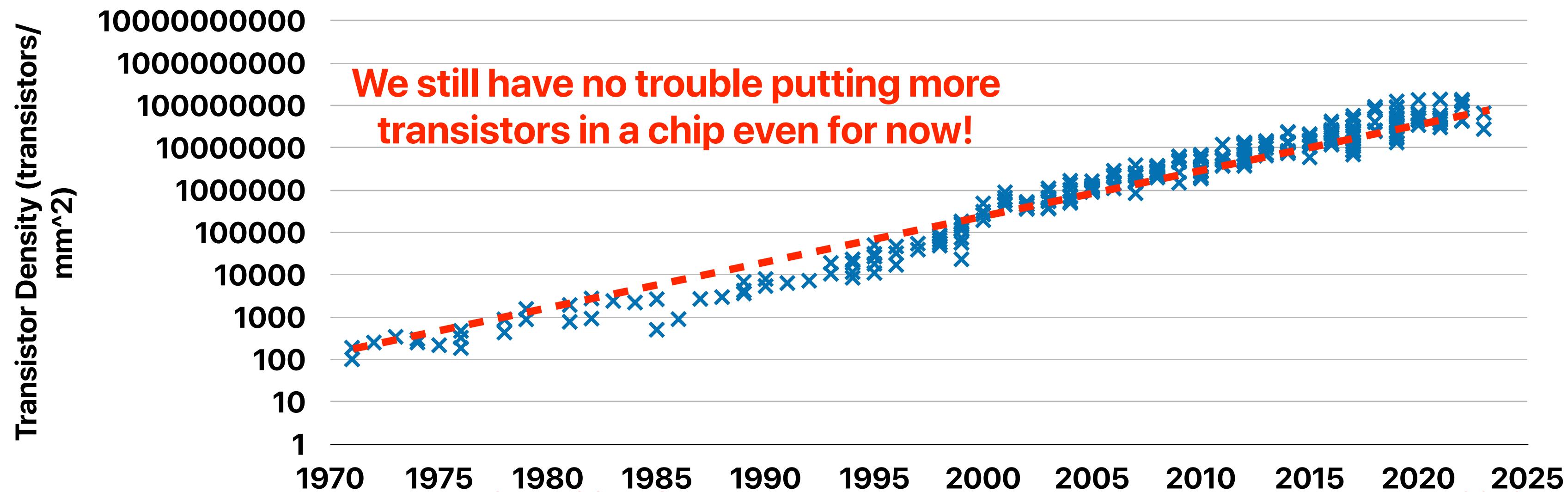
Take-aways of parallel programming

- Processor behaviors are non-deterministic
 - You cannot predict which processor is going faster
 - You cannot predict when OS is going to schedule your thread
- Cache coherency only guarantees that everyone would eventually have a coherent view of data, but not when
- Cache consistency is hard to support

The limiting factor of modern processor performance

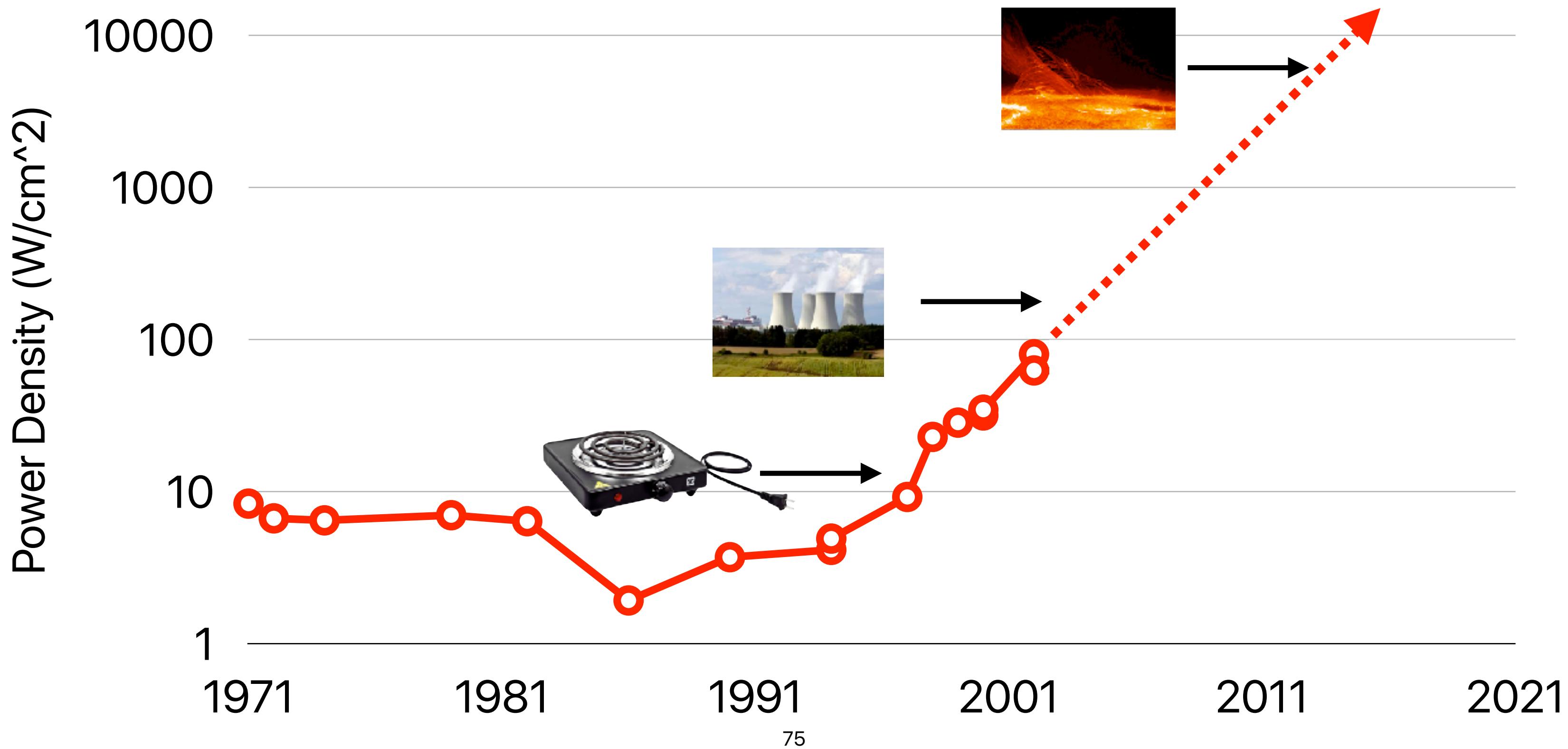
Moore's Law⁽¹⁾

- The number of transistors we can build in a fixed area of silicon doubles every 12 ~ 24 months.
- Moore's Law "was" the most important driver for historic CPU performance gains



(1) Moore, G. E. (1965), 'Cramming more components onto integrated circuits', Electronics 38 (8).

Power Density of Processors





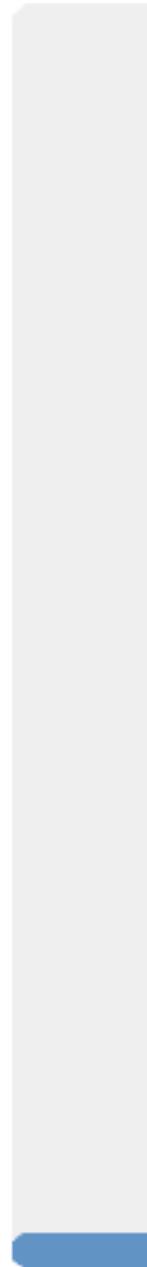
Power & Energy

- Regarding power and energy, how many of the following statements are correct?
 - ① Lowering the power consumption helps extending the battery life
 - ② Lowering the power consumption helps reducing the heat generation
 - ③ Lowering the energy consumption helps reducing the electricity bill
 - ④ A CPU with 10% utilization can still consume 33% of the peak power

A. 0
B. 1
C. 2
D. 3
E. 4

0

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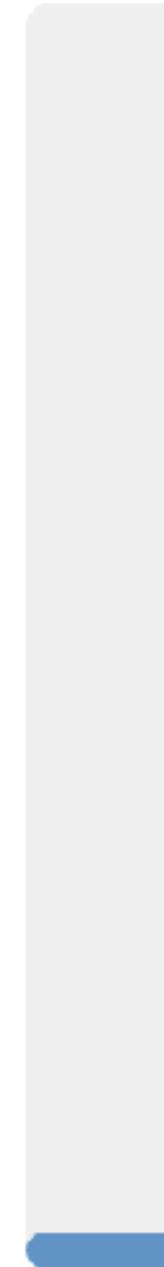
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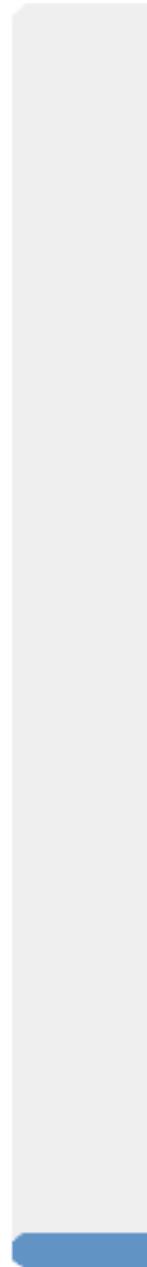
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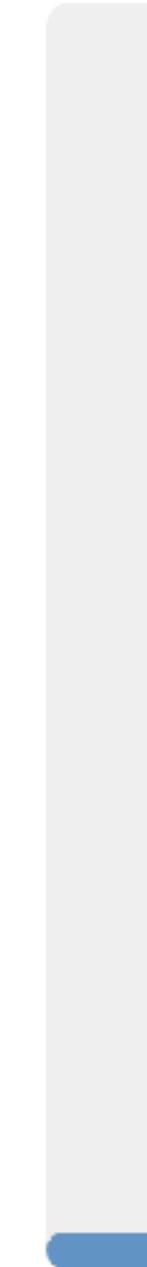
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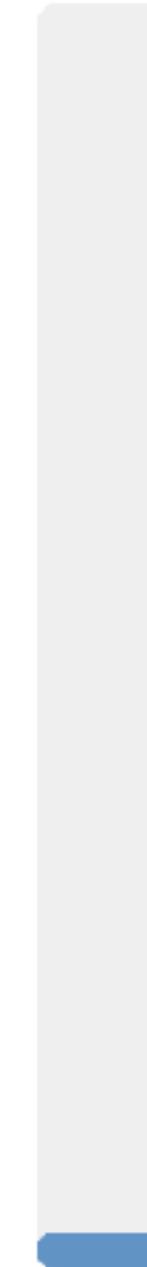
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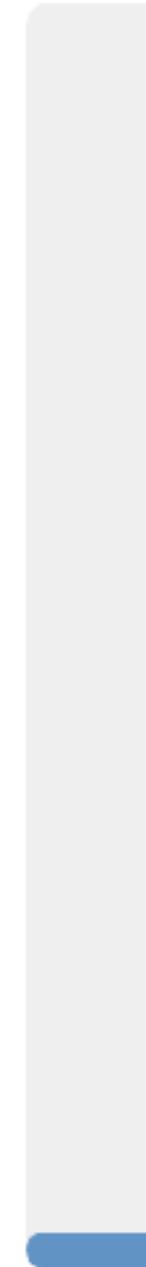
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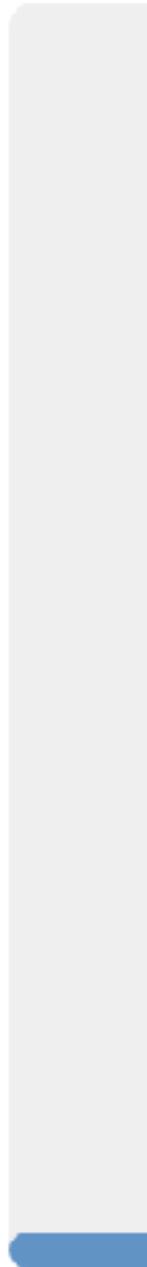
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- B. 1
- C. 2
- D. 3
- E. 4

Power consumption

Power v.s. Energy

- Power is the direct contributor of “heat”
 - Packaging of the chip
 - Heat dissipation cost
- $\text{Energy} = P * ET$
 - The electricity bill and battery life is related to energy!
 - Lower power does not necessarily means better battery life if the processor slow down the application too much

Dynamic/Active Power

- The power consumption due to the switching of transistor states
- Dynamic power per transistor

$$P_{dynamic} \sim \alpha \times C \times V^2 \times f \times N$$

- α : average switches per cycle
- C : capacitance
- V : voltage
- f : frequency, usually linear with V
- N : the number of transistors

Static/Leakage Power

- The power consumption due to leakage — transistors do not turn all the way off during no operation
- Becomes the **dominant** factor in the most advanced process technologies.

$$P_{leakage} \sim N \times V \times e^{-V_t}$$

- N : number of transistors
- V : voltage
- V_t : threshold voltage where transistor conducts (begins to switch)

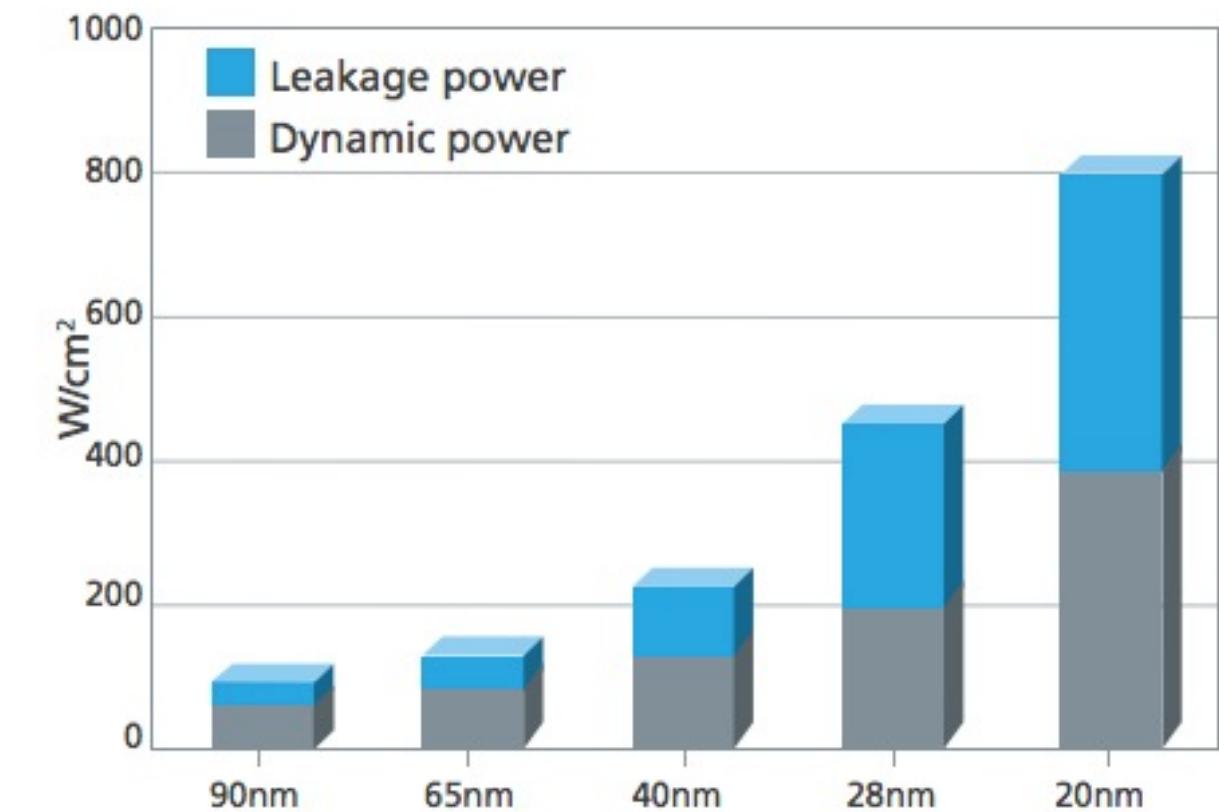


Figure 1: Leakage power becomes a growing problem as demands for more performance and functionality drive chipmakers to nanometer-scale process nodes (Source: IBS).

Dynamic/Active Power

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- Dynamic power per transistor

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- α : average switches per cycle
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- f : frequency, usually linear with V
- N : the number of transistors

Demo — changing the max frequency and performance

- Change the maximum frequency of the intel processor — you learned how to do this when we discuss programmer's impact on performance
- LIKWID a profiling tool providing power/energy information
 - likwid-perfctr -g ENERGY [command_line]
 - Let's try blockmm and popcorn and see what's happening!

matmul

CPU name: Intel(R) Core(TM) i5-9600K CPU @ 3.70GHz
 CPU type: Intel Coffeelake processor
 CPU clock: 3.70 GHz

Metric	Sum	Min	Max	Avg
Runtime (RDTSC) [s] STAT	56.7402	9.4567	9.4567	9.4567
Runtime unhalted [s] STAT	38089.9565	2.764721e-05	38089.9547	6348.3261
Clock [MHz] STAT	1.504735e+07	2530.3125	15027380	2.507892e+06
CPI STAT	29.6923	0.7684	11.1499	4.9487
Temperature [C] STAT	275	42	57	45.8333
Energy [J] STAT	247.1262	0	247.1262	41.1877
Power [W] STAT	26.1325	0	26.1325	4.3554
Energy PP0 [J] STAT	240.7318	0	240.7318	40.1220
Power PP0 [W] STAT	25.4563	0	25.4563	4.2427
Energy PP1 [J] STAT	0	0	0	0
Power PP1 [W] STAT	0	0	0	0
Energy DRAM [J] STAT	17.2582	0	17.2582	2.8764
Power DRAM [W] STAT	1.8250	0	1.8250	0.3042

Metric	Sum	Min	Max	Avg
Runtime (RDTSC) [s] STAT	202.3806	33.7301	33.7301	33.7301
Runtime unhalted [s] STAT	38089.3146	4.738974e-05	38089.3131	6348.2191
Clock [MHz] STAT	4.202013e+06	1135.3997	4196110	700335.5505
CPI STAT	14.9386	0.9997	6.2225	2.4898
Temperature [C] STAT	223	37	38	37.1667
Energy [J] STAT	88.4080	0	88.4080	14.7347
Power [W] STAT	2.6210	0	2.6210	0.4368
Energy PP0 [J] STAT	67.5248	0	67.5248	11.2541
Power PP0 [W] STAT	2.0019	0	2.0019	0.3337
Energy PP1 [J] STAT	0	0	0	0
Power PP1 [W] STAT	0	0	0	0
Energy DRAM [J] STAT	44.9120	0	44.9120	7.4853
Power DRAM [W] STAT	1.3315	0	1.3315	0.2219

pop count

Metric	Sum	Min	Max	Avg
Runtime (RDTSC) [s] STAT	11.8086	1.9681	1.9681	1.9681
Runtime unhalted [s] STAT	2.3622	0	2.3620	0.3937
Clock [MHz] STAT	17807.5257	2106.5416	4465.2964	2967.9209
CPI STAT	36.5243	0.3968	24.1941	6.0874
Temperature [C] STAT	249	39	49	41.5000
Energy [J] STAT	40.4858	0	40.4858	6.7476
Power [W] STAT	20.5715	0	20.5715	3.4286
Energy PPO [J] STAT	39.1853	0	39.1853	6.5309
Power PPO [W] STAT	19.9106	0	19.9106	3.3184
Energy PP1 [J] STAT	0	0	0	0
Power PP1 [W] STAT	0	0	0	0
Energy DRAM [J] STAT	1.9736	0	1.9736	0.3289
Power DRAM [W] STAT	1.0028	0	1.0028	0.1671

Metric	Sum	Min	Max	Avg
Runtime (RDTSC) [s] STAT	43.8276	7.3046	7.3046	7.3046
Runtime unhalted [s] STAT	2.3623	3.218655e-06	2.3620	0.3937
Clock [MHz] STAT	6822.7683	903.2673	1197.0151	1137.1281
CPI STAT	20.0735	0.3968	12.4175	3.3456
Temperature [C] STAT	218	36	37	36.3333
Energy [J] STAT	16.6005	0	16.6005	2.7668
Power [W] STAT	2.2726	0	2.2726	0.3788
Energy PPO [J] STAT	11.7680	0	11.7680	1.9613
Power PPO [W] STAT	1.6110	0	1.6110	0.2685
Energy PP1 [J] STAT	0	0	0	0
Power PP1 [W] STAT	0	0	0	0
Energy DRAM [J] STAT	7.3173	0	7.3173	1.2196
Power DRAM [W] STAT	1.0017	0	1.0017	0.1670

Power consumption to light on all transistors

Chip						
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1

=49W

Dennardian Scaling

Chip						
0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5

=50W

Dennardian Broken

Chip						
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1

On ~ 50W
Off ~ 0W
Dark!

=100W!

Recap: Speedup

- Assume that we have an application composed with a total of 500000 instructions, in which 20% of them are the load/store instructions with an average CPI of 6 cycles, and the rest instructions are integer instructions with average CPI of 1 cycle when using a 2GHz processor.
 - If we double the CPU clock rate to 4GHz that helps to accelerate all instructions by 2x except that load/store instruction cannot be improved — their CPI will become 12 cycles. What's the performance improvement after this change?

A. No change

$$ET = IC \times CPI \times CT$$

B. 1.25

$$ET_{baseline} = (5 \times 10^5) \times (20\% \times 6 + 80\% \times 1) \times \frac{1}{2 \times 10^{-9}} sec = 5^{-3}$$

C. 1.5

$$ET_{enhanced} = (5 \times 10^5) \times (20\% \times 12 + 80\% \times 1) \times \frac{1}{4 \times 10^{-9}} sec = 4^{-3}$$

D. 2

$$Speedup = \frac{Execution\ Time_{baseline}}{Execution\ Time_{enhanced}}$$

E. None of the above

$$= \frac{5}{4} = 1.25$$

The “power/energy cost” of doubling the clocking rate

$$Power_{new} = Power_{old} \times \left(\frac{f_{new}}{f_{old}}\right)^3$$

$$Power_{new} = Power_{old} \times (2)^3 = Power_{old} \times 8$$

$$Speedup = \frac{Execution\ Time_{baseline}}{Execution\ Time_{enhanced}} = \frac{5}{4} = 1.25$$

$$\begin{aligned} Energy_{new} &= Power_{new} \times ET_{new} \\ &= Power_{new} \times \frac{ET_{old}}{Speedup} \\ &= Power_{old} \times 8 \times \frac{ET_{old}}{1.25} = 6.4 \times Power_{old} \times ET_{old} \\ &= 6.4 \times Energy_{old} \end{aligned}$$

Power consumption & power density

- The power consumption due to the switching of transistor states
- Dynamic power per transistor:

$$P_{dynamic} \sim \alpha \times C \times V^2 \times f \times N$$

- α : average switches per cycle
- C : capacitance
- V : voltage
- f : frequency, usually linear with V
- N : the number of transistors

- Power density:

$$P_{density} = \frac{P}{area}$$

Moore's Law allows higher frequencies as transistors are smaller
Moore's Law makes this smaller

We cannot make chips always operating at very high frequencies

The “power” of doubling the clocking rate v.s. doubling the number of cores

$$P_{dynamic} \sim \alpha \times C \times V^2 \times f \times N$$

Doubling the clocking rate:

$$Power_{new} = Power_{old} \times \left(\frac{f_{new}}{f_{old}}\right)^3$$

$$Power_{new} = Power_{old} \times (2)^3 = Power_{old} \times 8$$

Doubling the number of cores:

$$Power_{new} = Power_{old} \times number_of_cores = Power_{old} \times 2$$

Recap: Amdahl's Law on Multicore Architectures

- Symmetric multicore processor with n cores (if we assume the processor performance scales perfectly)

$$\text{Speedup}_{\text{parallel}}(f_{\text{parallelizable}}, n) = \frac{1}{(1 - f_{\text{parallelizable}}) + \frac{f_{\text{parallelizable}}}{n}}$$

What if we double the number of cores?

$$Power_{new} = Power_{old} \times \text{number_of_cores} = Power_{old} \times 2$$

Assume 40% of execution time can be parallelized

$$\begin{aligned} Speedup_{parallel}(f_{parallelizable}, n) &= \frac{1}{(1 - f_{parallelizable}) + \frac{f_{parallelizable}}{n}} \\ &= \frac{1}{(1 - 40\%) + \frac{40\%}{2}} = 1.25 \end{aligned}$$

$$\begin{aligned} Energy_{new} &= Power_{new} \times ET_{new} \\ &= Power_{new} \times \frac{ET_{old}}{Speedup} \\ &= Power_{old} \times 2 \times \frac{ET_{old}}{1.25} = 1.6 \times Power_{old} \times ET_{old} \end{aligned}$$

A better deal in terms of energy!

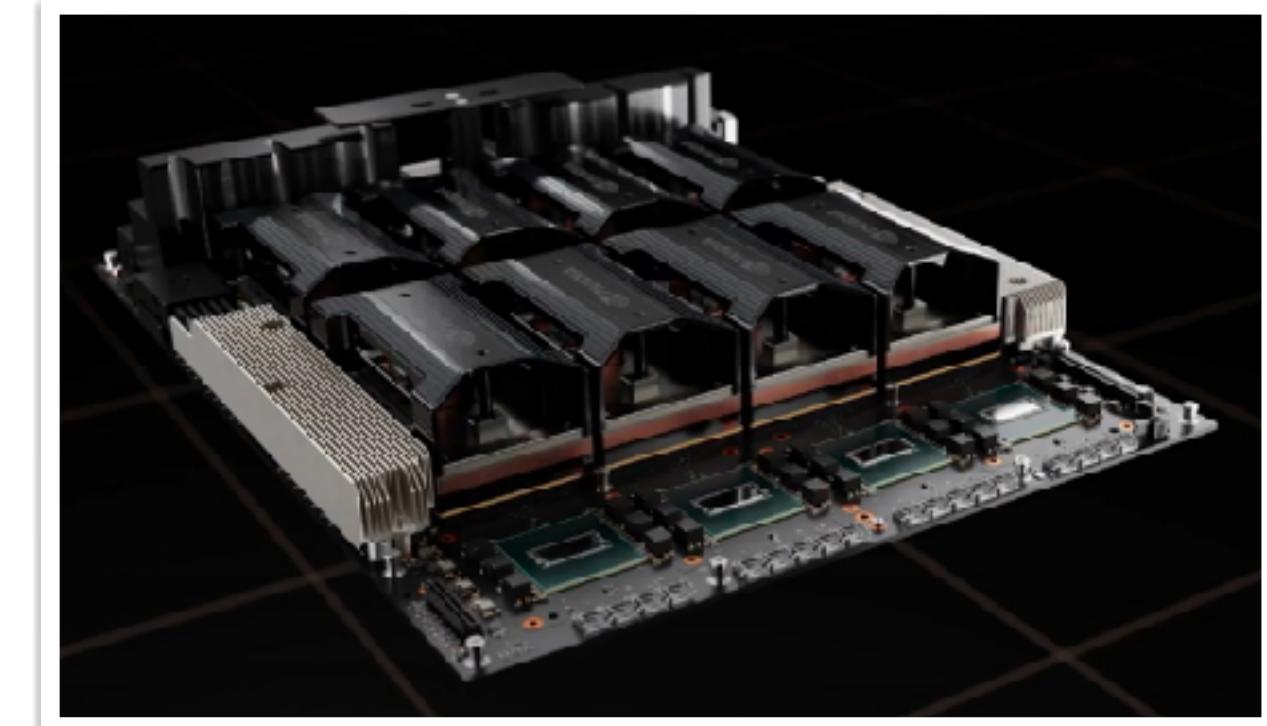
$$= 1.6 \times Energy_{old}$$

If you can add power budget...

NVIDIA Accelerator Specification Comparison			
	H100	A100 (80GB)	V100
FP32 CUDA Cores	16896	6912	5120
Tensor Cores	528	432	640
Boost Clock	~1.78GHz (Not Finalized)	1.41GHz	1.53GHz
Memory Clock	4.8Gbps HBM3	3.2Gbps HBM2e	1.75Gbps HBM2
Memory Bus Width	5120-bit	5120-bit	4096-bit
Memory Bandwidth	3TB/sec	2TB/sec	900GB/sec
VRAM	80GB	80GB	16GB/32GB
FP32 Vector	60 TFLOPS	19.5 TFLOPS	15.7 TFLOPS
FP64 Vector	30 TFLOPS	9.7 TFLOPS (1/2 FP32 rate)	7.8 TFLOPS (1/2 FP32 rate)
INT8 Tensor	2000 TOPS	624 TOPS	N/A
FP16 Tensor	1000 TFLOPS	312 TFLOPS	125 TFLOPS
TF32 Tensor	500 TFLOPS	156 TFLOPS	N/A
FP64 Tensor	60 TFLOPS	19.5 TFLOPS	N/A
Interconnect	NVLink 4 18 Links (900GB/sec)	NVLink 3 12 Links (600GB/sec)	NVLink 2 6 Links (300GB/sec)
GPU	GH100 (814mm ²)	GA100 (826mm ²)	GV100 (815mm ²)
Transistor Count	80B	54.2B	21.1B
TDP	700W	400W	300W/350W
Manufacturing Process	TSMC 4N	TSMC 7N	TSMC 12nm FFN
Interface	SXM5	SXM4	SXM2/SXM3
Architecture	Hopper	Ampere	Volta



<https://www.workstationspecialist.com/product/nvidia-tesla-a100/>



<https://www.servethehome.com/wp-content/uploads/2022/03/NVIDIA-GTC-2022-H100-in-HGX-H100.jpg>