review the history of CPU

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Abstract CPU is the abbreviation of Central Processing Unit, and it is one of the most important part of a computer. Principal components of a CPU include the arithmetic logic unit (ALU) that performs arithmetic and logic operations, hardware registers that supply operands to the ALU and store the results of ALU operations, and a control unit that fetches instructions from memory and "executes" them by directing the coordinated operations of the ALU, registers and other components. The development of CPU is quite rapid, the CPU within personal computer takes only twenty years upgraded from 8088(XT) to current Core series. During this period, according to the processing word length, CPU can be divided into: 4-bit microprocessor, 8-bit microprocessor, 16-bit microprocessor, 32-bit microprocessors and 64-bit microprocessor. One can say that the history of personal computers is the development of CPU. In recent years, it developed from single-core to multi-core, and all of these changes are contributing to the competitive relation between two giant CPU manufacturers Intel and amd. Although they are competing, but this does not hinder the pace of development of the CPU, the upgrade of CPU is actually instead promoted. Nowadays, the implementation of CPU is not only limited to computers and some electronic devices, it is also used on the cell-phone, which makes its functions more powerful.

Key Words Central Processing Unit, Mononuclear, Multinuclear, Microprocessor

Contents

1 Introduction

Generally speaking, CPU (Central Processing Unit), internal storage memory and I/O device are three core components of one computer. Indeed CPU is the core of core among these three components, it is both a operation center and a control center. Its main job is to interpret computer instructions and process incoming data from software following the way specified by the instructions. CPU is constructed by ALU (arithmetic logic unit), hardware registers, the control unit and the bus between them. The principle operations performed by CPU can be concluded into four steps: Fetch, Decode, Execute and Write-back.

1.1 Working Principle

CPU fetches instructions from memory or cache into instruction registers, and performs decoding there. The commands are divided into a series of micro-operations, which will be executed according to the micro-operations which are issued by CPU, thus is the completion of execution of an instruction. Instruction, which is the basic operation type of a computer, includes the address of the operation code, one or more operand address, some machine status fields and signature. Some instructions also directly include operand itself.

1.1.1 fetch

The first step, fetch, involves retrieving an instruction (which is represented by a number or sequence of numbers) from program memory. The instruction's location (address) in program memory is determined by a program counter (PC), which stores a number that identifies the address of the next instruction to be fetched. After an instruction is fetched, the PC is incremented by the length of the instruction so that it will contain the address of the next instruction in the sequence. Often, the instruction to be fetched must be retrieved from relatively slow memory, causing the CPU to stall while waiting for the instruction to be returned. This issue is largely addressed in modern processors by caches and pipeline architectures.

1.1.2 decode

The instruction that the CPU fetches from memory determines what the CPU has to do. In the decode step, the instruction is broken up into parts that have significance to other portions of the CPU. The way in which the numerical instruction value is interpreted is defined by the CPU's instruction set architecture (ISA). Often, one group of numbers in the instruction, called the opcode, indicates which operation to perform. The remaining parts of the number usually provide information required for that instruction, such as operands for an addition operation. Such operands may be given as a constant value (called an immediate value), or as a place to locate a value: a register or a memory address, as determined by some addressing mode.

In some CPU designs the instruction decoder is implemented as a hardwired, unchangeable circuit. In others, a microprogram is used to translate instructions into sets of CPU configuration signals that are applied sequentially over multiple clock pulses. In some cases the memory that stores the microprogram is rewritable, making it possible to change the way in which the CPU decodes instructions.

1.1.3 execute

After the fetch and decode steps, the execute step is performed. Depending on the CPU architecture, this may consist of a single action or a sequence of actions. During each action, various parts of the CPU are electrically connected so they can perform all or part of the desired operation and then the action is completed, typically in response to a clock pulse. Very often the results are written to an internal CPU register for quick access by subsequent instructions. In other cases results may be written to slower, but less expensive and higher capacity main memory.

For example, if an addition instruction is to be executed, the arithmetic logic unit (ALU) inputs are connected to a pair of operand sources (numbers to be summed), the ALU is configured to perform an addition operation so that the sum of its operand inputs will appear at its output, and the ALU output is connected to storage (e.g., a register or memory) that will receive the sum. When the clock pulse occurs, the sum will be transferred to storage and, if the resulting sum is too large (i.e., it is larger than the ALU's output word size), an arithmetic overflow flag will be set.

1.1.4 Write-back

The final step is Write-back, which simply writeback the result of the execute phase in certain form. Some instructions manipulate the program counter rather than producing result data directly; such instructions are generally called "jumps" and facilitate program behavior like loops, conditional program execution (through the use of a conditional jump), and existence of functions. In some processors, some other instructions change the state of bits in a "flags" register. These flags can be used to influence how a program behaves, since they often indicate the outcome of various operations. For example, in such processors a "compare" instruction evaluates two values and sets or clears bits in the flags register to indicate which one is greater or whether they are equal; one of these flags could then be used by a later jump instruction to determine program flow.

After the execution of an instruction, the entire process repeats, with the next instruction cycle normally fetching the next-in-sequence instruction because of the incremented value in the program counter. If a jump instruction was executed, the program counter will be modified to contain the address of the instruction that was jumped to and program execution continues normally.

In more complex CPUs, multiple instructions can be fetched, decoded, and

executed simultaneously. This section describes what is generally referred to as the "classic RISC pipeline", which is quite common among the simple CPUs used in many electronic devices (often called microcontroller). It largely ignores the important role of CPU cache, and therefore the access stage of the pipeline.

1.2 CPU Construction

Generally speaking, CPU contains three main components: ALU, Registers and CU. [1]

1.2.1 ALU

The arithmetic logic unit (ALU) is a digital circuit within the processor that performs integer arithmetic and bitwise logic operations. The inputs to the ALU are the data words to be operated on (called operands), status information from previous operations, and a code from the control unit indicating which operation to perform. Depending on the instruction being executed, the operands may come from internal CPU registers or external memory, or they may be constants generated by the ALU itself.

When all input signals have settled and propagated through the ALU circuitry, the result of the performed operation appears at the ALU's outputs. The result consists of both a data word, which may be stored in a register or memory, and status information that is typically stored in a special, internal CPU register reserved for this purpose.

1.2.2 Register

Registers are normally measured by the number of bits they can hold, for example, an "8-bit register" or a "32-bit register". A processor often contains several kinds of registers, that can be classified according to their content or instructions that operate on them:

User-accessible registers – instructions that can be read or written by machine instructions. The most common division of user-accessible registers is into data registers and address registers. *Data registers* can hold numeric values such as integer and, in some architectures, floating-point values, as well as characters, small bit arrays and other data. In some older and low end CPUs, a special data register, known as the accumulator, is used implicitly for many operations. *Address registers* hold addresses and are used by instructions that indirectly access primary memory.

General purpose registers (GPRs) can store both data and addresses, i.e., they are combined Data/Address registers and rarely the register file is unified to include floating point as well. Conditional registers hold truth values often used to determine whether some instruction should or should not be executed. Floating point registers (FPRs) store floating point numbers in many architectures. Constant registers hold read-only values such as zero, one, or pi. Vector registers hold data for vector processing done by SIMD instructions

(Single Instruction, Multiple Data).

Special purpose registers (SPRs) hold program state; they usually include the program counter, also called the instruction pointer, and the status register; the program counter and status register might be combined in a program status word (PSW) register. The aforementioned stack pointer is sometimes also included in this group. Embedded microprocessors can also have registers corresponding to specialized hardware elements. In some architectures, model-specific registers (also called machine-specific registers) store data and settings related to the processor itself. Because their meanings are attached to the design of a specific processor, they cannot be expected to remain standard between processor generations.

Internal registers – registers not accessible by instructions, used internally for processor operations. Instruction register, holding the instruction currently being executed. Registers related to fetching information from RAM, a collection of storage registers located on separate chips from the CPU: Memory buffer register (MBR), Memory data register (MDR) and Memory address register (MAR).

Hardware registers are similar, but occur outside CPUs.

1.2.3 CU

The control unit (CU) is a component of a computer's central processing unit (CPU) that directs operation of the processor. It tells the computer's memory, arithmetic/logic unit and input and output devices how to respond to a program's instructions.[2]

It directs the operation of the other units by providing timing and control signals. Most computer resources are managed by the CU. It directs the flow of data between the CPU and the other devices. John von Neumann included the control unit as part of the von Neumann architecture. In modern computer designs, the control unit is typically an internal part of the CPU with its overall role and operation unchanged since its introduction. [3]

2 CPU design

2.1 Integer range

Every CPU represents numerical values in a specific way. For example, some early digital computers represented numbers as familiar decimal (base 10) numeral system values, and others have employed more unusual representations such as ternary (base three). Nearly all modern CPUs represent numbers in binary form, with each digit being represented by some two-valued physical quantity such as a "high" or "low" voltage.

A six-bit word containing the binary encoded representation of decimal value 40. Most modern CPUs employ word sizes that are a power of two, for example eight, 16, 32 or 64 bits.

Related to numeric representation is the size and precision of integer numbers that a CPU can represent. In the case of a binary CPU, this is measured by the number of bits (significant digits of a binary encoded integer) that the CPU can process in one operation, which is commonly called "word size", "bit width", "data path width", "integer precision", or "integer size". A CPU's integer size determines the range of integer values it can directly operate on. For example, an 8-bit CPU can directly manipulate integers represented by eight bits, which have a range of 256 (2^8) discrete integer values.

Integer range can also affect the number of memory locations the CPU can directly address (an address is an integer value representing a specific memory location). For example, if a binary CPU uses 32 bits to represent a memory address then it can directly address 2^{32} memory locations. To circumvent this limitation and for various other reasons, some CPUs use mechanisms (such as bank switching) that allow additional memory to be addressed.

CPUs with larger word sizes require more circuitry and consequently are physically larger, cost more, and consume more power (and therefore generate more heat). As a result, smaller 4- or 8-bitmicrocontrollers are commonly used in modern applications even though CPUs with much larger word sizes (such as 16, 32, 64, even 128-bit) are available. When higher performance is required, however, the benefits of a larger word size (larger data ranges and address spaces) may outweigh the disadvantages.

To gain some of the advantages afforded by both lower and higher bit lengths, many CPUs are designed with different bit widths for different portions of the device. For example, the IBM System/370 used a CPU that was primarily 32 bit, but it used 128-bit precision inside its floating point units to facilitate greater accuracy and range in floating point numbers.[4] Many later CPU designs use similar mixed bit width, especially when the processor is meant for general-purpose usage where a reasonable balance of integer and floating point capability is required.

2.2 Clock rate

Most CPUs are synchronous circuits, which means they employ a clock signal to pace their sequential operations. The clock signal is produced by an external oscillator circuit that generates a consistent number of pulses each second in the form of a periodic square wave. The frequency of the clock pulses determines the rate at which a CPU executes instructions and, consequently, the faster the clock, the more instructions the CPU will execute each second.

To ensure proper operation of the CPU, the clock period is longer than the maximum time needed for all signals to propagate (move) through the CPU. In setting the clock period to a value well above the worst-case propagation delay, it is possible to design the entire CPU and the way it moves data around the "edges" of the rising and falling clock signal. This has the advantage of

simplifying the CPU significantly, both from a design perspective and a component-count perspective. However, it also carries the disadvantage that the entire CPU must wait on its slowest elements, even though some portions of it are much faster. This limitation has largely been compensated for by various methods of increasing CPU parallelism.

However, architectural improvements alone do not solve all of the drawbacks of globally synchronous CPUs. For example, a clock signal is subject to the delays of any other electrical signal. Higher clock rates in increasingly complex CPUs make it more difficult to keep the clock signal in phase (synchronized) throughout the entire unit. This has led many modern CPUs to require multiple identical clock signals to be provided to avoid delaying a single signal significantly enough to cause the CPU to malfunction. Another major issue, as clock rates increase dramatically, is the amount of heat that is dissipated by the CPU. The constantly changing clock causes many components to switch regardless of whether they are being used at that time. In general, a component that is switching uses more energy than an element in a static state. Therefore, as clock rate increases, so does energy consumption, causing the CPU to require more heat dissipation in the form of CPU cooling solutions.

One method of dealing with the switching of unneeded components is called clock gating, which involves turning off the clock signal to unneeded components (effectively disabling them). However, this is often regarded as difficult to implement and therefore does not see common usage outside of very low-power designs. One notable recent CPU design that uses extensive clock gating is the IBM PowerPC-based Xenon used in the Xbox 360; that way, power requirements of the Xbox 360 are greatly reduced. Another method of addressing some of the problems with a global clock signal is the removal of the clock signal altogether. While removing the global clock signal makes the design process considerably more complex in many ways, asynchronous (or clockless) designs carry marked advantages in power consumption and heat dissipation in comparison with similar synchronous designs. While somewhat uncommon, entire asynchronous CPUs have been built without utilizing a global clock signal. Two notable examples of this are the ARM compliant AMULET and the MIPS R3000 compatible MiniMIPS.

Rather than totally removing the clock signal, some CPU designs allow certain portions of the device to be asynchronous, such as using asynchronous ALUs in conjunction with superscalar pipelining to achieve some arithmetic performance gains. While it is not altogether clear whether totally asynchronous designs can perform at a comparable or better level than their synchronous counterparts, it is evident that they do at least excel in simpler math operations. This, combined with their excellent power consumption and heat dissipation properties, makes them very suitable for embedded computers. [5]

2.3 Parallelism

The description of the basic operation of a CPU offered in the previous section describes the simplest form that a CPU can take. This type of CPU, usually referred to as subscalar, operates on and executes one instruction on one or two pieces of data at a time.

This process gives rise to an inherent inefficiency in subscalar CPUs. Since only one instruction is executed at a time, the entire CPU must wait for that instruction to complete before proceeding to the next instruction. As a result, the subscalar CPU gets "hung up" on instructions which take more than one clock cycle to complete execution. Even adding a second execution unit does not improve performance much; rather than one pathway being hung up, now two pathways are hung up and the number of unused transistors is increased. This design, wherein the CPU's execution resources can operate on only one instruction at a time, can only possibly reach scalar performance (one instruction per clock). However, the performance is nearly always subscalar (less than one instruction per cycle).

Attempts to achieve scalar and better performance have resulted in a variety of design methodologies that cause the CPU to behave less linearly and more in parallel. When referring to parallelism in CPUs, two terms are generally used to classify these design techniques. Instruction level parallelism (ILP) seeks to increase the rate at which instructions are executed within a CPU (that is, to increase the utilization of on-die execution resources), and thread level parallelism (TLP) purposes to increase the number of threads (effectively individual programs) that a CPU can execute simultaneously. Each methodology differs both in the ways in which they are implemented, as well as the relative effectiveness they afford in increasing the CPU's performance for an application.

2.3.1 Instruction-level parallelism

One of the simplest methods used to accomplish increased parallelism is to begin the first steps of instruction fetching and decoding before the prior instruction finishes executing. This is the simplest form of a technique known as instruction pipelining, and is utilized in almost all modern general-purpose CPUs. Pipelining allows more than one instruction to be executed at any given time by breaking down the execution pathway into discrete stages. This separation can be compared to an assembly line, in which an instruction is made more complete at each stage until it exits the execution pipeline and is retired.

Pipelining does, however, introduce the possibility for a situation where the result of the previous operation is needed to complete the next operation; a condition often termed data dependency conflict. To cope with this, additional care must be taken to check for these sorts of conditions and delay a portion of the instruction pipeline if this occurs. Naturally, accomplishing this requires additional circuitry, so pipelined processors are more complex than subscalar

ones (though not very significantly so). A pipelined processor can become very nearly scalar, inhibited only by pipeline stalls (an instruction spending more than one clock cycle in a stage).

Further improvement upon the idea of instruction pipelining led to the development of a method that decreases the idle time of CPU components even further. Designs that are said to be superscalar include a long instruction pipeline and multiple identical execution units.[6] In a superscalar pipeline, multiple instructions are read and passed to a dispatcher, which decides whether or not the instructions can be executed in parallel (simultaneously). If so they are dispatched to available execution units, resulting in the ability for several instructions to be executed simultaneously. In general, the more instructions a superscalar CPU is able to dispatch simultaneously to waiting execution units, the more instructions will be completed in a given cycle.

Most of the difficulty in the design of a superscalar CPU architecture lies in creating an effective dispatcher. The dispatcher needs to be able to quickly and correctly determine whether instructions can be executed in parallel, as well as dispatch them in such a way as to keep as many execution units busy as possible. This requires that the instruction pipeline is filled as often as possible and gives rise to the need in superscalar architectures for significant amounts of CPU cache. It also makes hazard-avoiding techniques like branch prediction, speculative execution, and out-of-order execution crucial to maintaining high levels of performance. By attempting to predict which branch (or path) a conditional instruction will take, the CPU can minimize the number of times that the entire pipeline must wait until a conditional instruction is completed. Speculative execution often provides modest performance increases by executing portions of code that may not be needed after a conditional operation completes. Out-of-order execution somewhat rearranges the order in which instructions are executed to reduce delays due to data dependencies. Also in case of Single Instructions Multiple Data — a case when a lot of data from the same type has to be processed, modern processors can disable parts of the pipeline so that when a single instruction is executed many times, the CPU skips the fetch and decode phases and thus greatly increases performance on certain occasions, especially in highly monotonous program engines such as video creation software and photo processing.

In the case where a portion of the CPU is superscalar and part is not, the part which is not suffers a performance penalty due to scheduling stalls. The Intel P5 Pentium had two superscalar ALUs which could accept one instruction per clock each, but its FPU could not accept one instruction per clock. Thus the P5 was integer superscalar but not floating point superscalar. Intel's successor to the P5 architecture, P6, added superscalar capabilities to its floating point features, and therefore afforded a significant increase in floating point instruction performance.

Both simple pipelining and superscalar design increase a CPU's ILP by allowing a single processor to complete execution of instructions at rates surpassing one instruction per cycle (IPC). Most modern CPU designs are at least somewhat superscalar, and nearly all general purpose CPUs designed in the last decade are superscalar. In later years some of the emphasis in designing high-ILP computers has been moved out of the CPU's hardware and into its software interface, or ISA. The strategy of the very long instruction word (VLIW) causes some ILP to become implied directly by the software, reducing the amount of work the CPU must perform to boost ILP and thereby reducing the design's complexity.

2.3.2 Thread-level parallelism

Another strategy of achieving performance is to execute multiple programs or threads in parallel. This area of research is known as parallel computing. In Flynn's taxonomy, this strategy is known as Multiple Instructions-Multiple Data or MIMD.

One technology used for this purpose was multiprocessing (MP). The initial flavor of this technology is known as symmetric multiprocessing (SMP), where a small number of CPUs share a coherent view of their memory system. In this scheme, each CPU has additional hardware to maintain a constantly up-to-date view of memory. By avoiding stale views of memory, the CPUs can cooperate on the same program and programs can migrate from one CPU to another. To increase the number of cooperating CPUs beyond a handful, schemes such as non-uniform memory access (NUMA) and directory-based coherence protocols were introduced in the 1990s. SMP systems are limited to a small number of CPUs while NUMA systems have been built with thousands of processors. Initially, multiprocessing was built using multiple discrete CPUs and boards to implement the interconnect between the processors. When the processors and their interconnect are all implemented on a single silicon chip, the technology is known as a multi-core processor.

It was later recognized that finer-grain parallelism existed with a single program. A single program might have several threads (or functions) that could be executed separately or in parallel. Some of the earliest examples of this technology implemented input/output processing such as direct memory access as a separate thread from the computation thread. A more general approach to this technology was introduced in the 1970s when systems were designed to run multiple computation threads in parallel. This technology is known as multi-threading (MT). This approach is considered more cost-effective than multiprocessing, as only a small number of components within a CPU is replicated to support MT as opposed to the entire CPU in the case of MP. In MT, the execution units and the memory system including the caches are shared among multiple threads. The downside of MT is that the hardware support for multithreading is more visible to software than that of MP and thus supervisor

software like operating systems have to undergo larger changes to support MT. One type of MT that was implemented is known as block multithreading, where one thread is executed until it is stalled waiting for data to return from external memory. In this scheme, the CPU would then quickly switch to another thread which is ready to run, the switch often done in one CPU clock cycle, such as the UltraSPARC Technology. Another type of MT is known as simultaneous multithreading, where instructions of multiple threads are executed in parallel within one CPU clock cycle.

For several decades from the 1970s to early 2000s, the focus in designing high performance general purpose CPUs was largely on achieving high ILP through technologies such as pipelining, caches, superscalar execution, out-of-order execution, etc. This trend culminated in large, power-hungry CPUs such as the Intel Pentium 4. By the early 2000s, CPU designers were thwarted from achieving higher performance from ILP techniques due to the growing disparity between CPU operating frequencies and main memory operating frequencies as well as escalating CPU power dissipation owing to more esoteric ILP techniques.

CPU designers then borrowed ideas from commercial computing markets such as transaction processing, where the aggregate performance of multiple programs, also known as throughput computing, was more important than the performance of a single thread or program.

This reversal of emphasis is evidenced by the proliferation of dual and multiple core CMP (chip-level multiprocessing) designs and notably, Intel's newer designs resembling its less superscalar P6 architecture. Late designs in several processor families exhibit CMP, including the x86-64 Opteron and Athlon 64 X2, the SPARC UltraSPARC T1, IBM POWER4 and POWER5, as well as several video game console CPUs like the Xbox 360's triple-core PowerPC design, and the PS3's 7-core Cell microprocessor.

2.3.3 Data parallelism

A less common but increasingly important paradigm of CPUs (and indeed, computing in general) deals with data parallelism. The processors discussed earlier are all referred to as some type of scalar device. As the name implies, vector processors deal with multiple pieces of data in the context of one instruction. This contrasts with scalar processors, which deal with one piece of data for every instruction. Using Flynn's taxonomy, these two schemes of dealing with data are generally referred to as SIMD (single instruction, multiple data) and SISD (single instruction, single data), respectively. The great utility in creating CPUs that deal with vectors of data lies in optimizing tasks that tend to require the same operation (for example, a sum or a dot product) to be performed on a large set of data. Some classic examples of these types of tasks are multimedia applications (images, video, and sound), as well as many types of scientific and engineering tasks. Whereas a scalar CPU must complete the entire

process of fetching, decoding, and executing each instruction and value in a set of data, a vector CPU can perform a single operation on a comparatively large set of data with one instruction. Of course, this is only possible when the application tends to require many steps which apply one operation to a large set of data.

Most early vector CPUs, such as the Cray-1, were associated almost exclusively with scientific research and cryptography applications. However, as multimedia has largely shifted to digital media, the need for some form of SIMD in general-purpose CPUs has become significant. Shortly after inclusion of floating point execution units started to become commonplace in general-purpose processors, specifications for and implementations of SIMD execution units also began to appear for general-purpose CPUs. Some of these early SIMD specifications like HP's Multimedia Acceleration eXtensions (MAX) and Intel's MMX were integer-only. This proved to be a significant impediment for some software developers, since many of the applications that benefit from SIMD primarily deal with floating point numbers. Progressively, these early designs were refined and remade into some of the common, modern SIMD specifications, which are usually associated with one ISA. Some notable modern examples are Intel's SSE and the PowerPC-related AltiVec (also known as VMX).

3 CPU development history

3.1 Intel

Intel Corporation is an American multinational corporation headquartered in Santa Clara, California. Intel is one of the world's largest and highest valued semiconductor chip makers, based on revenue. It is the inventor of the x86 series of microprocessors, the processors found in most personal computers.

Intel Corporation, founded on July 18, 1968, is a portmanteau of Integrated Electronics (the fact that "intel" is the term for intelligence information also made the name appropriate). Intel also makes motherboard chipsets, network interface controllers and integrated circuits, flash memory, graphic chips, embedded processors and other devices related to communications and computing. Founded by semiconductor pioneers Robert Noyce and Gordon Moore and widely associated with the executive leadership and vision of Andrew Grove, Intel combines advanced chip design capability with a leading-edge manufacturing capability. Though Intel was originally known primarily to engineers and technologists, its "Intel Inside" advertising campaign of the 1990s made it a household name, along with its Pentium processors.

Intel was an early developer of SRAM and DRAM memory chips, and this represented the majority of its business until 1981. Although Intel created the world's first commercial microprocessor chip in 1971, it was not until the success of the personal computer (PC) that this became its primary business. During the 1990s, Intel invested heavily in new microprocessor designs fostering the rapid

growth of the computer industry. During this period Intel became the dominant supplier of microprocessors for PCs, and was known for aggressive and sometimes illegal tactics in defense of its market position, particularly against Advanced Micro Devices (AMD), as well as a struggle with Microsoft for control over the direction of the PC industry. [7]

1971: 4004 microprocessor

as a project in 1969, develop the first microprocessor for the Japanese computer manufacturer Busicom, Intel did a series of research on a variety of programmable computer chips. Eventually, in November 15, 1971, the Intel 4004 microprocessor was introduced to the global market, at the time, its market sale price is $ 200 per chip. 4004, which is Intel's first microprocessor, lays the foundation for the future development of the intelligent functions and PC systems, the number of transistors is about two thousand three hundred.

1972: 8008 microprocessor

1972, Intel launched the 8008 microprocessor, its computing power is twice as of 4004. in 1974, Radio Electronics published an article which introduced a device embedded with the Mark-8 8008. This device is recognized as the first home computer. For the standard at that time, this computer is quite difficult in the part of manufacturing, maintenance, and operational aspects. the number of Intel 8008 transistors is about three thousand and five hundred.

1974: 8080 microprocessor

1974, Intel launched the 8080 processor, which performed as the core of Altair personal computer. Altair is the spacecraft's destination business in the 'Star Trek' television series. Computer fans is available to but a set of Altair's suite at price of $ 395 at that time. It sold tens of thousands units in a few months, which became the first models manufacturing after paragraph. The number of Intel 8080 transistors was about six thousand.

1978: 8086, 8088 microprocessor

This microprocessor got significant sales contracts, when the PC division of IBM was newly established, Intel 8088 processor become the best-selling new products in IBM, called as IBM 'PC's brain. The success of the Intel 8088 processor push Intel onto the Fortune 500 companies list, Fortune magazine rated Intel as one of '70s most successful companies'. The number of Intel 8088 was about 29,000.

1982: 80286 microprocessor

80286 (also known as 286) is Intel's first processor capable of performing all the old proprietary software processor, the software compatibility became the registered trademark of Intel microprocessors in the following years. in the nearest 6-year sales phase, Intel estimated to install 286 on 15 million PC at total

worldwide. The number of Intel 80286 processor transistors was 134,000.

1985: 80386 microprocessor

Intel 80386 microprocessor containing 275,000 transistors - more than 100 times faster than the original 4004, this 32 bit for the first time to support multi-task processor design that can execute multiple programs simultaneously. The number of transistors is about Intel 80386 270 005 one thousand.

1989: Intel 80486 microprocessor

Intel 80486 processor generations make the transition from a command to a computer column-and-click (point to click) graphical operating environment, according to the Smithsonian Museum of American History of science and technology historian David K. Allison recalls: "I have first Ministry color screen computers can begin to significantly accelerate the speed of desktop publishing work. "Intel 80486 processor built-in math coprocessor lead, due to play a central processor complex mathematical calculations, and therefore able to speed up the whole operation. Intel 80486 to 1.2 million the number of transistors.

1993: Intel Pentium processor

Pentium is Intel's first named to abandon the use of digital processors, a breakthrough in micro-architecture, let the computer easier to deal with the "real world" data, such as voice, sound, writing, and photo images. From comics and television talk show Pentium, asked the city immediately after becoming a household name, Intel Pentium processor number to 3.1 million transistors.

1996: Intel Pentium Pro processor

Initially occupies a part of the market INTEL CPU did not stop their own pace, in other companies are constantly catching their Pentium occasion, has introduced the latest generation of the sixth generation of X86 series CPU P6 date in 1996. P6 just its research code, the listing P6 has a very famous name dates PentimuPro. Internal PentimuPro containing up to 5.5 million transistors, the internal clock frequency is 133MHZ, almost twice the processing speed of 100MHZ PENTIUM of. PentimuPro level (on-chip) 8KB instruction cache and 8KB data. It is noteworthy that in one package in addition to the PentimuPro chip also includes a 256KB secondary cache chips, internal communication between the two chips high-bandwidth interconnect bus, processor and cache the connection lines are also placed In this package, thus making it easier for the cache to run at a higher frequency. The L2CACHE PentiumPro 200MHZ CPU is running at 200MHZ, which is working on the same frequency as the processor. This design led PentiumPro achieve maximum performance. And PentimuPro most striking is that it has an innovative technology called "dynamic execution", which is the second PENTIUM achieve real break in the superscalar architecture after another leap forward. PentimuPro operating frequency is 150/166/180/200 series, a cache is 16KB, while the first three have a 256KB secondary cache, as

the frequency of the CPU 200 is also divided into three versions, different is that they The built-in cache are 256KB, 512KB, 1MB.

1997: Intel Pentium II

Processor contains 7.5 million transistors Pentium II processor incorporates Intel MMX technology, able to deal with very high efficiency video, audio, and graphics data, for the first time using the Single Edge Contact (SEC) cartridge package, built-in high-speed cache memory. This chip allows computer users to capture, edit, and share digital photos through the Internet and friends, edit and add text, music or making home movies of transition effects, as well as through the use of video telephony standard telephone line and Internet network transmission movie, Intel Pentium II processor number to 7.5 million transistors.

1998: Intel Celeron processor

1998, AMD's low-cost policy work, while the price of 1/3 on the Intel processor clock, successful invasion of low-cost processor market, then the basic type of computer (NT $: 30,000 ~ 25,000-) popular, plus AMD's K6-2 processor itself superior integer arithmetic capability, ideal for the basic needs of an average family, the major works have introduced low-cost computer Socket-7 platform. During this period, Intel processors in order to completely dominate the next generation, to renounce the Socket-7 architecture, and National Semiconductor jointly issued a new generation architecture - Slot-1, and launched a new processor architecture - Pentium II, although this processor, success into the mainstream market, but expensive Pentium II, plus expensive motherboard, making low-cost Intel completely lost piece of the pie of the market. To invade this market, the introduction of new low-cost processor battlefield, is a must, but the design of a new processor, the required initial investment is very high R & D costs, so from the original intention Intel Pentium II processor started in March 1998 when, Intel officially launched the new processors - Celeron. Had launched Celeron processor, the architecture and maintain the same Pentium II (Deschutes), using Slot-1, and the Pentium II core architecture is the same as with MMX multimedia instruction set, but the original Pentium II in the two L2 cache body is canceled. Intel removed L2 cache, in addition to reducing costs, and then the most important is to be different from the mainstream Pentium II in the performance, in addition to L2 cache, the processor's external operating frequency (Front Side BUS), but also Intel used to distinguish between mainstream and low-cost processors watershed: it was Intel Pentium II processor FSB is 100 MHz (the earliest Pentium II 350), and are cheap Celeron is to maintain the traditional 66 MHz Celeron core architecture, and Pentium II are identical, but less L2 cache, which affects the overall effectiveness of the right, in the end not so big? P3c we look at today's mentality should have a bottom up, for example, the core Likewise for the clock to 500 MHz P3 processor FSB under the same state, On-Die 256K L2 cache full of P3 500E, on the effectiveness of literally half speed than P3 500 512K L2 cache to

come quickly, Light speed L2 cache, there is such a great influence (first and ASB aside ATC), not to mention a 'no' L2 cache. Cache-less in the low-cost Celeron processor, has just launched, the target on the low-cost computers, thanks to Slot-1 architecture, then can be used with only 440 LX motherboard and chipset 440BX, but this type of motherboard, are to match the Pentium II-based, it is difficult to drive down the price, plus the Cache-Less's Celeron processor, Winstone tests, poor low score, so, Intel introduced the first Celeron 266/300 MHz, the effectiveness of the has been cast aside for

1998: Intel Celeron 300A processor

August 24, 1998, such an unforgettable date for hardware fans, Intel introduced the Celeron is equipped with two A processor cache, which is in the future by many DIYer Lift altar Celeron 300A, one can no longer make classic models. Celeron 300A, in a sense already a second generation Intel Celeron processor. The first generation Celeron processor only has 266MHz, 300MHz versions, the first generation of Celeron processor because they do not own any of the secondary cache, while effectively reducing the cost, but the performance cannot be satisfactory. To compensate for lack of performance, Intel Celeron processor has finally debuted with the secondary cache - using Mendocino core Celeron300A, 333,366. Classic, was born. Classic Celeron 300A, and not just because it's overclocked (most Celeron 300A can be easily overclocked to 550MHZ), but also that the Celeron 300A overclocking almost a specially created for it born chain, motherboards, turn access card ..... how many such products would be born to a Celeron 300A. For a time, newspapers and magazines, online media are discussing this Celeron300A overclocking mode, techniques, with the motherboard, memory and so on. DIY overclocking era official to face.

1999: Intel Pentium III processor

Intel Pentium III processor adds 70 new instructions, adding Internet streaming SIMD extension set called MMX, can significantly enhance the advanced imaging, application performance 3D, streaming music, videos, voice recognition and so on, it can significantly enhance the Internet the experience, allowing users to browse realistic online museums and shops, as well as download high-quality video, Intel first introduced into 0.25-micron technology, Intel Pentium III transistor number about 9.5 million.

2000: Intel Pentium 4 processor

Pentium 4 processors built using 42 million transistors, and 0.18 micron circuits, the operation frequency of Intel's first microprocessor 4004 is 108KHz, Pentium 4 version of the speed of the initial launch of up to 1.5GHz, if the vehicle speed at the same period at the same rate upward, driving from San Francisco to New York just 13 seconds, the number of transistors Pentium 4 processor is about 42 million, the following year in August, Pentium 4 2 GHz

processing management reached a milestone.

2002: Intel Pentium 4 HT processor

Intel introduced the new Intel Pentium 4 processor contains innovative Hyper-Threading (HT) Hyper-Threading technology. Hyper-Threading technology to create a new class of high-performance desktop computers that can simultaneously perform multiple computing applications quickly, or result in higher performance for multi-threaded software support. Hyper-Threading technology allows computer performance increase of 25%. In addition to providing Hyper-Threading Technology for desktop computer users, Intel also reached another milestone computers that operate at frequencies up to 3.06 GHz introduced the Pentium 4 processor, is the first commercial implementation of micro 3 billion operations per cycle processor, so thanks to excellent performance was the industry's most advanced 0.13-micron process technology, the following year, the built-in Hyper-Threading technology, Intel Pentium 4 processor frequency of 3.2 GHz.

2003: Intel Pentium M

New mobile CPU processor designed by the Israeli group, Pentium M, Intel's x86 microprocessor architecture for notebook PCs, was also part of the Centrino, launched in March 2003. Announced the following speeds: standard 1.6GHz, 1.5GHz, 1.4GHz, 1.3GHz, low voltage 1.1GHz, ultra-low voltage 900MHz. In order to get high performance at low speeds, Banias make optimized so that the number of instructions that can be executed per clock more, and through advanced branch prediction to reduce the error rate prediction. Another improvement is the most prominent L2 cache increased to 1MB (P3-M and P4-M have only 512KB), the estimated number of Banias up to 77 million transistors on most of it is used in this. There are also a series of design-related reduction in power consumption: Enhanced Speedstep technology is essential, and with multiple supply voltage and frequency is calculated, so that the performance can better meet the application requirements. Intelligent power distribution system can be concentrated to the local processor power needed, and closes an idle application; Mobile Voltage Positioning (MVPIV) technology dynamically reduces voltage based on processor activity to support a lower thermal design power and more compact shape design; optimized power 400MHz system bus; Micro-opsfusion micro-op instruction fusion, in the presence of a plurality of instructions can be simultaneously executed, these instructions into one instruction, in order to improve performance and power efficiency. Dedicated Stack Manager, use the recorded internal operation of dedicated hardware, the processor can execute the program without interruption. Banias corresponding chipset 855 series, 855 chipset consists of Northbridge and Southbridge 855 ICH4-M composition, Northbridge into 855PM without built-in graphics cards (codenamed Odem) with built-in graphics and 855GM (codenamed Montara-GM), supports up to 2GB of DDR266 / 200 memory, AGP4X, USB2.0, two

ATA-100, AC97 sound and Modem. 855GM which is three-dimensional and display engine optimization InternalClockGating, it can be a three-dimensional display engine power when needed, thereby reducing the power chipset.

2005: Intel Pentium D processor

The first contains two processing cores Intel Pentium D processor debut, officially opened the era of multi-core x86 processor.

2006: Intel Core 2 Duo processor

Core desktop processor microarchitecture, codenamed Conroe will be named Core 2 Duo / Extreme family, its E6700 2.6GHz models previously introduced the most powerful Intel Pentium D 960 (3.6GHz) processor, the performance improved by 40% , energy efficiency is also increased 40%, Core 2 Duo processor contains 291 million transistors.

2008: Intel Atom processor

June 3, 2008, Intel introduced to the media in Beijing and Taipei computer show their simultaneous launch of Atom processors Atom. Intel Atom processing using 45-nanometer manufacturing process, 2.5 watt low power consumption, low cost, and performance to meet basic needs, mainly for netbooks (Netbook) and nettops (Nettop) use. As a simple-to-use, affordable new Internet devices - new netbook and nettop computers, they mainly have better Internet capabilities, can also be learning, entertainment, pictures, video and other applications, is a combination of economic and portability products. Its most representative products for six months before the launch of the Asus Eee PC pioneered computer, and now Dell, Acer, HP and many other manufacturers have also launched similar products, the industry outlook for the market. The launch of the Intel Atom processor is divided into two, designed for netbooks with Atom N270 designed for nettop Atom 230, with the 945GM chipset to meet basic video, graphics, browsing needs, and compact , while prices can be controlled in less than mainstream computer price. According to Intel accounted for using the Atom processor netbook can do up to about $ 250, while the nettop will not exceed $ 300. Intel demonstrated at the Great Wall, Haier, Tongfang represented nettop and netbook devices. Where the Internet is priced the same side of an expected around 1999 yuan, mainly used to connect an LCD TV, Internet access and a variety of digital applications through the remote control, and the ability to install XP system computer applications. The number of domestic price has not announced a netbook, but the estimated price will be around 2999 yuan to win the market.

2008: Intel Core i7 processor

Intel officially confirmed, based on the new Nehalem architecture for a new generation of desktop processors will follow the "Core" (Core) name, named as "Intel Core i7" series, Extreme Edition is the name "Intel Core i7 Extreme" series.

Core i7 (Chinese: Core i7, Core code: (Bloomfield) processor is Intel launched in 2008 64 quad-core CPU, follow the x86-64 instruction set, and Intel Nehalem micro-architecture, replace Intel Core 2 series processor .Nehalem once Pentium 4 10 GHz version of the code .Core i7's name and no special meaning, Intel i7 means to take this name only because it sounds sweet, "i" means intelligence (intelligence initials) , and 7 no particular meaning, but does not refer to the 7th generation of products. the Core is a continuation of the successful generation of Core processors, some people will be "wife" of the nickname. the official launch date is November 2008 on the 17th. As early as November 3, the official has announced prices of related products, online evaluation will have to be re-opened.

2009: Intel Core i5 processor

Intel Core i5 processor is a product, also based on Intel Nehalem microarchitecture. And Core i7 triple channel memory support different, Core i5 only integrated dual-channel DDR3 memory controller. In addition, Core i5 will integrate some Northbridge functions will be integrated PCI-Express controller. Interface also with the LGA 1366 Core i7 different, Core i5 with a new LGA 1156. Processor core, the code Lynnfiled, using 45-nanometer process will be four core i5 does not support Hyper-Threading technology, providing a total of only four threads. L2 cache memory areas, each core has its own separate 256KB, and up to 8MB of L3 share a memory buffer. Chipset, will use Intel P55 (Code: IbexPeak). In addition to its support Lynnfield, it will also support Havendale processors. The latter, although only two processor cores, but integrated graphics core. P55 will use a single-chip design, functionality similar to traditional Southbridge, supports SLI and Crossfire technology. However, with the high-end X58 chipset different, P55 does not use the newer QPI connection, but will DMI using conventional techniques . Interfaces can be compatible with other 5 Series Chipset. It will replace the P45 chipset.

2010: Intel Core i3 processor

As a Core i3 Core i5 further Lite is for mainstream users CPU family identity. Has Clarkdale (2010), Arrandale (2010), Sandy Bridge (2011) and other variety of sub-series.

2011: Intel Sandy Bridge processor

SNB (Sandy Bridge) is a next-generation processor microarchitecture Intel released in early 2011, the greatest significance of this framework than to redefine the concept of "integrated platform", with the processor "seamless integration" of the "Core Graphics "The End of the" integrated graphics "era. This initiative benefited from the new 32nm manufacturing process. Since under the Frame Processor Sandy Bridge uses than the previous 32nm 45nm process more advanced manufacturing technology, in theory, to achieve a further reduced, and the circuit size significantly optimize power consumption and performance

of the CPU, which is the integrated graphics core (core Graphics) and the CPU package on the same piece of substrate to create favorable conditions. In addition, the second-generation Core also added a new high-definition video processing unit. Video to decode high and low speed is a direct relationship with the processor, because the video processing time adding high-definition video processing unit, a new generation of Intel Core processors than the old processor upgrade at least 30%.

2012: Intel ivy Bridge processor

In the April 24, 2012 in the afternoon Beijing Planetarium, intel released the ivy bridge (IVB) processors. Number of 22nm Ivy Bridge will double execution units, reaching a maximum of 24, it will bring a further leap in performance. Ivy Bridge will add support for DX11 in integrated graphics. Also newly added XHCI USB 3.0 controller is shared among four channels, providing up to four USB 3.0, to support native USB3.0. CPU making use of 3D transistor technology CPU power consumption will be reduced by half.

3.2 AMD

In 1981, AMD 287 FPU, use Intel80287 core. Market positioning and performance of products and Intel80287 basically the same. AMD is so far the only company producing over FPU product, very rare.

AMD 8080 (1974), 8085 (1976), 8086 (1978), 8088 (1979), 80186 (1982), 80188,80286 microprocessor core using Intel8080. Market positioning and performance with Intel namesake product is basically the same.

1991 AMD 386 microprocessor, the core code P9, there SX and DX points, respectively, and is compatible with Intel80386SX DX microprocessor. AMD 386DX with Intel 386DX with 32-bit processors. AMD 386SX is different is a full 16-bit processor, and Intel 386SX is a quasi 32-bit processor (internal bus 32, the external 16-bit). AMD 386DX performance and Intel80386DX no difference between himself, the same time as one of the mainstream products. AMD has developed a 386 DE 386 and other models based on the core of embedded products.

1993 AMD 486DX microprocessor, the core code P4, AMD designed and produced the first generation of 486 products. Then rolled out to other 486-level products, common models are: 486DX2, codenamed P24; 486DX4, codenamed P24C; 486SX2, codenamed P23 and so on. Other derivative models also 486DE, 486DXL2 etc., are relatively rare. AMD 486 is the highest frequency 120MHz (DX4-120), this is the first time in the frequency beyond the powerful rival Intel.

AMD 5X86 1995 microprocessor, the core code X5, AMD Company weapon in 486 markets. Post-486 era, TI (Texas Instruments) has launched a cost-effective TI486DX2-80, soon occupied the low-end market, Intel also introduced a high-end Pentium series. AMD vacancies in order to seize the

market, has launched a 5x86 series CPU (almost simultaneously launched with Cyrix 5x86). It is the most high-frequency products 486 ---- 33 * 4,133MHz, 0.35-micron manufacturing process, a built-in 16KB write-back cache, the performance directed Pentium75, and the power consumption is less than the Pentium.

1997 AMD K5 microprocessor, 1997 release. Because research and development issues, and its time to market later than competitors, Intel's "Pentium" a lot, plus the performance is not very good, the product was unsuccessful AMD makes a lot of loss of market share. K5 performance is very general, integer arithmetic capabilities compare Cyrix x86, but better than "Pentium" slightly stronger; floating point capability is far less than the budget "Pentium", but slightly stronger than the Cyrix 6x86. On the whole, K5 belong compare the average strength of the product, and listed at the beginning of the low prices to attract more customers than its performance. In addition, most high-end K5-RP200 production is small, and there is no sales in mainland China.

1997 AMD K6 processor with Intel PentiumMMX same grade products. AMD's acquisition of NexGen, integrate advanced NexGen 686 technical masterpiece after that time. It also contains the MMX instruction set as well as a whole than the Pentium MMX twice as large cache of 64KB of L1! Overall comparison, K6 is a successful work, but in terms of performance, floating point capability is still lower than the Pentium MMX.

1998 was the AMD K6-2 microprocessor series of competitive products, and now we call it classic. In order to defeat rival Intel, AMD K6-2 family of microprocessors based on the K6 made significant improvements, the most important is the inclusion of "3DNow!" Command support. "3DNow!" Command is a major breakthrough for the X86 system, the benefits of this technology is greatly enhanced 3D processing power of the computer, give us really good 3D performance. When you use a special "3DNow!" Optimizing the software can be found, what is the great potential of K6-2. And most of the K6-2 and no-locked, with 0.25-micron manufacturing process gives us the low heat, can easily overclock. That is, from the beginning K6-2, Intel's overclocking is no longer a proper noun. Meanwhile, K6-2 also inherited AMD has always been the tradition, the same frequency than the Intel model price is about 25% lower, market sales amazing. K6-2 series listed at the beginning of the use of the "K6 3D" name ("3D" that "3DNow!"), Just to name until officially listed as "K6-2". Because of this, most of the K6 3D for ES (a small amount of the official version, after all, no mass production). K6 3D had a non-standard 250MHz product, but did not appear in the official K6-2 series. The lowest frequency for K6-2 200MHz, up to 550MHz.

1999 AMD launched in February 1999, codenamed "Sharptooth" (teeth) of K6-3 (1998) series microprocessor, which is a support AMD launched last Super architecture and CPGA package of CPU. K6-3 uses a 0.25-micron manufacturing

process, integrated 256KB secondary cache (rival Intel's new Celeron is 128KB), and clock speed of the CPU operation. And once it was K6-3 Socket L2 point automatic recognition for L3, which for the high frequency of CPU is undoubtedly very edge 7 on the motherboard, although still far from satisfactory K6-3 floating-point operations. For various reasons, K6-3 after the market hard to find, the price is not approachable, even after the emergence of more advanced K6-3 +.

2001 AMD in October 2001 launched the K8 architecture. Although K8 and K7 uses the same number of floating-point scheduler window (scheduling window), but the integer unit of 18 from K7 expanded to 24, in addition, AMD K7 in the branch prediction unit has been improved. global history counter buffer (for the record CPU access to data within a certain period of time, called the entire history buffer count) compared to full big Athlon 4 times, and in measuring the wrong branch before the pipeline can accommodate more more than the number of instructions, AMD improvements in integer scheduler lets pipeline depth K8 Athlon more than two. Increased levels conduit aims to enhance the depth of the K8 core frequency. In the K8, AMD increased the reserve conversion buffer, which is to deal with Opteron server applications in large memory requirements.

2007 AMD launched the K10 architecture in the second half. K10 architecture using Barcelona quad-core and have 463 million transistors. Barcelona is AMD's first quad-core processor, the native architecture is based on 65nm process technology. And Intel Kentsfield quad-core difference is that, Barcelona is not the two dual-core package together, but true single-chip quad-core.

3 Multi-core

A multi-core processor is a single computing component with two or more independent actual processing units (called "cores"), which are the units that read and execute program instructions. The instructions are ordinary CPU instructions such as add, move data, and branch, but the multiple cores can run multiple instructions at the same time, increasing overall speed for programs amenable to parallel computing. Manufacturers typically integrate the cores onto a single integrated circuit die (known as a chip multiprocessor or CMP), or onto multiple dies in a single chip package.

3.1 dual core processor

Dual-core refers to a CPU that includes two complete execution cores per physical processor. It has combined two processors and their caches and cache controllers onto a single integrated circuit (silicon chip). Dual-core processors are well-suited for multitasking environments because there are two complete execution cores instead of one, each with an independent interface to the frontside bus. Since each core has its own cache, the operating system has sufficient resources to handle most compute intensive tasks in parallel.

Support for dual-CPU software, such as the commonly used MAX, PS, MAYA, etc., dual CPU can indeed accelerate the rendering speed. And the theory is twice on a single CPU. Only the actual application process failed to reach, because some of the data in the middle of the distribution of computing also requires CPU resources.

For the software does not support dual CPU, like most games, word processing software, dual CPU and single CPU and no difference.

The so-called dual-core processor, simply put, is on a two processor cores integrated CPU board, and by the parallel bus connecting each processor core. Dual-core is not a new concept, but rather CMP (Chip Multi Processors, single-chip multi-processor) basic and easiest type easiest to implement.

In other words dual core processor is a processor based on a single semiconductor that has two functions of the same processor core. This will be two physical processor cores integrated into a core, when the task is arduous, two cores can cooperate with each other to allow the CPU to maximize effectiveness. Two complementary core can run up and performance is very good, for example, using Intel Pentium D dual-core processor is equivalent to that you have two hosts using the Pentium 4. If Hyper-Threading is to use software to simulate the effect of dual-core, so we are talking about dual core is the true sense of the two cores. He made up for hyper threading less applicable system shortcomings, can be widely used for multiple versions of windows operating system; he also effectively solve the dual-core computing appear in separate data cache conflict error problem.

3.2 Multi core processor

Held in San Francisco Fall 2006 Intel Developer Forum (IDF), Intel President and CEO Paul Otellini announced • Intel will deliver the world's first general-purpose server for the PC and quad-core processors in November, and this when Intel introduced dual-core processors from the time is not yet a year, not only that, Intel also made clear that the current can be 80 nuclear integrated onto a single chip, the "hundred nuclear program" is also a laboratory in full swing . It seems, in the lead industry into the dual-core from a single-core, Intel will more quickly towards the "quad", or even higher.

Intel announced at IDF revealed new plans, the first quad-core processor will be shipped in November this year, the mainstream Intel Core 2 Quad processor will ship in the first quarter of 2007. Among them, the target user's PC market is enthusiastic crowd computer games and content creators, named for Intel Core 2 Quad processor Extreme Edition. Intel claims that, compared with the current Intel Core 2 Duo processor Extreme Edition, the new processor performance will increase 67%. In the server side, two-way quad-core Intel Xeon processor server 5300 (codenamed Kentsfield) series will also be shipped this year. The blade server designed for 50-watt, low-power quad-core Intel Xeon processor L5310

will be shipped in the first quarter next year.

4 Performance

The performance or speed of a processor depends on, among many other factors, the clock rate (generally given in multiples of hertz) and the instructions per clock (IPC), which together are the factors for the instructions per second (IPS) that the CPU can perform. Many reported IPS values have represented "peak" execution rates on artificial instruction sequences with few branches, whereas realistic workloads consist of a mix of instructions and applications, some of which take longer to execute than others. The performance of the memory hierarchy also greatly affects processor performance, an issue barely considered in MIPS calculations. Because of these problems, various standardized tests, often called "benchmarks" for this purpose—such as SPECint – have been developed to attempt to measure the real effective performance in commonly used applications.

Processing performance of computers is increased by using multi-core processors, which essentially is plugging two or more individual processors (called cores in this sense) into one integrated circuit. Ideally, a dual core processor would be nearly twice as powerful as a single core processor. In practice, the performance gain is far smaller, only about 50%, due to imperfect software algorithms and implementation. Increasing the number of cores in a processor (i.e. dual-core, quad-core, etc.) increases the workload that can be handled. This means that the processor can now handle numerous asynchronous events, interrupts, etc. which can take a toll on the CPU when overwhelmed. These cores can be thought of as different floors in a processing plant, with each floor handling a different task. Sometimes, these cores will handle the same tasks as cores adjacent to them if a single core is not enough to handle the information.

Due to specific capabilities of modern CPUs, such as hyper-threading and uncore, which involve sharing of actual CPU resources while aiming at increased utilization, monitoring performance levels and hardware utilization gradually became a more complex task. As a response, some CPUs implement additional hardware logic that monitors actual utilization of various parts of a CPU and provides various counters accessible to software; an example is Intel's Performance Counter Monitor technology.

5 Other applications

5.1 Cell-phone CPU

Phone CPU, one of the mobile phone performance in their daily lives are being ignored by shoppers, in fact, a remarkable performance smartphone is certainly the most important is its "core" is the CPU, as the computer CPU, as it the entire central nervous system control of mobile phones, but also the central part of the logic control. By calling microprocessor and memory database software running within memory, control purposes.

5.1.1 Quidway

Hass K3V2, was in 2012 the industry's smallest quad-core A9 processor architecture. He is a high-performance CPU, clocked at 1.2GHz and is divided into 1.5GHz, Huawei independent design, the use of the ARM architecture 35NM, 64-bit memory bus, which is twice Tegra 3 memory bus. The processor appears ended China-made mobile phones, "lack of core small core" of the situation, so that after Huawei, Samsung and Apple to become the third independent manufacturers produce chips.

5.1.2 TI OMAP

Texas Instruments (TexasInstruments) position in the mobile CPU market like Nokia in the mobile phone market, a well-deserved big brother. Its OMAP family of processors has been Nokia, HTC and Palm Queen CPU, can be compatible with Linux, Windows CE, Palm, Symbian S60, WindowsMobile mainstream operating systems. From the initial clocked at 132 OMAP710, until now clocked at 1.5GHz ARM Cortex-A9 integrated dual-core OMAP4440 processor type and frequency of 2GHz integrated multi-core ARM Cortex-A15 processor type of OMAP543x, Texas has been at the forefront of the development of mobile CPU, from the list below, we can see a more detailed models of Texas Instruments CPU configuration and representative models.

5.1.3 Intel&Marvell

Speaking of Intel, we are not unfamiliar, we know from the outset for Intel computers are familiar with the different computers in a flourishing industry in mobile CPU market always reach the peak, but still stumbling along the way. PXA210 from Intel's first market, with its high frequency, very good deal for the 3D effect, won a lot of manufacturers of all ages, while the next product on the clock speed and processing capabilities have been improved, but because of Intel's chip workmanship higher price than the same period of the corresponding products is much higher, the power consumption is greater, so the market reaction is not good, only to see the PXA series figure in Motorola and HTC's high-end machines, and after Intel Published clocked at 624MHz PXA272, at the time the highest frequency of mobile phone CPU, then got bigger vendors and the user's attention, in a good market prospects when, Intel Xscale was surprisingly sold to Marvell. That's why I put Intel, Marvell put together the reasons described, after the completion of the acquisition of Marvell PXA 3XX series launched, has used on many famous models, such as the Samsung I908 and so on.

5.1.4 Qualcomm

In July 1985, seven senior industry executives gathered to discuss Dr. Irwin Jacobs home in San Diego, an idea. These dreamers -FranklinAntonio, Adelia Coffman, Andrew Cohen, Klein Gilhousen, Irwin Jacobs, AndrewViterbi and HarveyWhite- decide they want to build "high-quality communications," and

developed a plan, and finally evolved the plan for the communications industry's greatest entrepreneurs One of the success stories: Qualcomm.

Degree from the name Qualcomm does not seem like the Texas Instruments, Intel so loud, players in the smart phone, Qualcomm favored much higher than the previous two. Qualcomm's mobile phone chipset includes MobileStationModems (MSM chipset), a single-chip (QSC) and the Snapdragon platform. Compatible with a variety of intelligent systems, we can find in the mainstream smartphone manufacturers whose figure, Qualcomm CPU is characterized by excellent performance, multimedia and strong analytical ability, depending on the location of the mobile phone, launched as economy, multimedia sex Enhanced and converged four different chips. Meanwhile Qualcomm CPU chip is the first to be compatible Android system, so what occupies Android mobile CPU half, Android is the trend of the future of intelligent systems, Qualcomm is like for this to prepare to take off Android plus wings, prospects for the future.

5.2 Nanotechnology

Introducing the world's first ready-volume production of three-dimensional transistor, 22nm: new technology and will achieve unprecedented performance and energy efficiency of Intel microprocessor family for the future introduction of a fundamentally different techniques: the use of 22-nanometer manufacturing process of three-dimensional transistor . These new crystal management makes Intel may continue the relentless pursuit of Moore's Law, the pace of technological progress to ensure consumers can expect to continue in the coming years.

So far, as a microprocessor core transistors are two-dimensional (plane) devices. Intel's tri-gate transistors and a three-dimensional volume manufacturing capability of the transistor computer chip marks a huge change in the basic structure. Learn more about the history of the transistor. This also means that Intel can continue to support the product - from the world's fastest supercomputers to mobile handheld devices are very small - is leading. The size and structure of the transistor is as small as possible to bring the benefits of Moore's Law, the core of the end user. The smaller the transistor size, the higher the energy efficiency, the better. Intel will continue to shrink in a predictable way in a series of "world first" in its manufacturing technology: 2007 45nm high dielectric constant / metal gate, 2009 32 nm, and now, in 2011 launched the world's first use of high-capacity 22nm logic process three-dimensional transistor. Use a smaller size three-dimensional transistors, Intel can design more energy-efficient and more powerful processors. This new technology will enable the realization of innovative micro-architecture, system-on-chip (SoC) designs and new products - from servers and PC to smart phones and innovative consumer products.

6 Conclusion

Coming of the Internet age, network communications, information security and information appliances will become increasingly popular, CPU is the essential component in all these devices. Due to the more and more advanced manufacturing technology, increasing numbers of electronic components are integrated and embedded. Tens of thousands, or even millions of tiny transistors constitute the internal structure of CPU. With the rapid development of technology in our age, CPU will become the most core technology and will also lead a better life for human beings.

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