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Introduction:

Supercomputing, sometimes called high performance computing, has become an essential part in computational science. Trillions of floating point operations are performed per second in supercomputers. In this paper, I am going to write about the history of supercomputing and Seymour Cray, founder of supercomputers. Then, I am going to explain the architecture of the supercomputers. In addition, I am going to write where the supercomputers are used, the general applications of supercomputers, and the fastest supercomputer in the world and its capability. Finally, I am going to conclude the paper with the future of supercomputers.

History of Supercomputing:

The history of supercomputing, sometimes called high performance computing (HPC), starts at the beginning of 1960. The first supercomputers are the Control Data Corporation (CDC), which was designed and architected by Seymour Cray, and the pilot Atlas, which was installed at the University of Manchester. [1][2] Both of them use computational parallelism to accomplish the high performance computing. [1] [2]

The Atlas Supervisor supercomputer was firstly introduced in the summer of 1962 and was a collaborative project between University of Manchester and Ferranti Ltd. [2] it was the fastest supercomputer at that time by operating one million instructions per second. It used germanium transistors. [2]

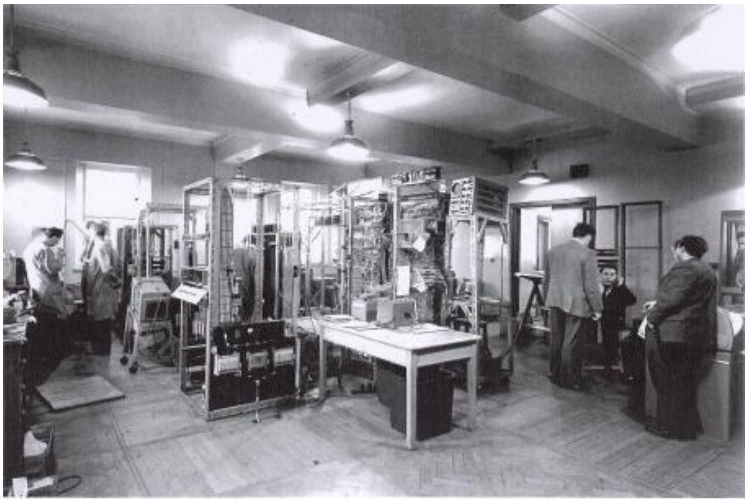

Figure 1. The pilot Atlas, University of Manchester [1]

The Control Data Corporation (CDC) 6600 was designed by Seymour Cray, the founder of the supercomputers, and released in 1664. It was considered as the fastest computer at that time, by ten times faster than fastest computers of the day. It had one CPU with ten parallel units; and performed three million floating point operations per second. [1] The CDC 6600 used silicon transistors instead of germanium transistors which made it three times faster than Atlas and IBM Stretch. [2]

CDC 6600 was innovative design and was the only supercomputer that use transistors instead of vacuum tubes. It included dense package, cooling, multiple parallel units, one processor to provide multiple processors, I/O Computers, and RISC (Reduced Instruction Set Computing). [1] The success of CDC 6600 leaded

Cray to sell one hundred of them at $8 million per each in the supercomputing market. [3]

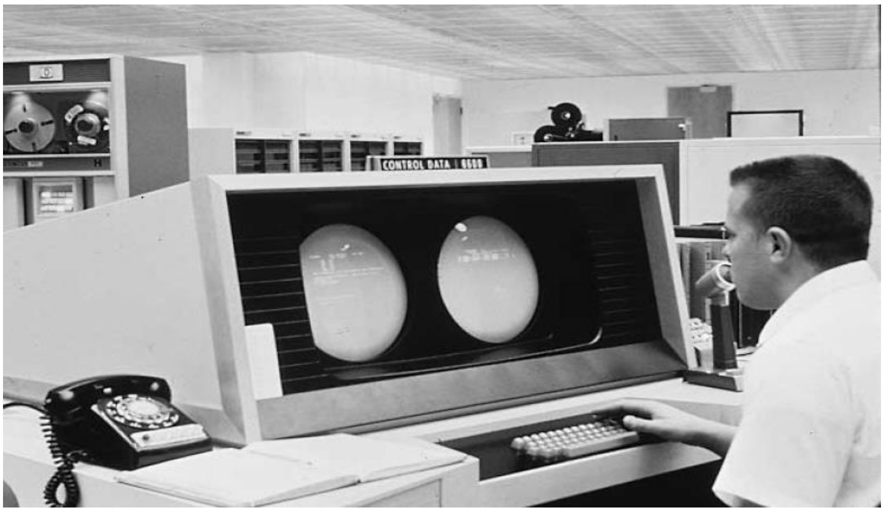

Figure 2. CDC 6600 by Seymour Cray [6]

In 1669, Cray design the CDC 7600 with the new concepts of pipelining that made it ran twenty times faster than CDC 6600. It ran at 36.4 MHz and delivered fifteen million floating point operations per second. [1][3] Cray left CDC management and decided to own his own Cray Research Company in 1972. [3]

In 1976, Cray designed the Cray-1, which had 80 MHz, in Cray Research and was the first practical vector processors, which performed one hundred million floating point instructions per second and executed 32 arithmetic operations at a time. [1][4] It was considered the most successful supercomputer in the world. [4] Nine years later, Cray-2 was released with eight processors computer cooling and performed 1.9 giga floating point operations per second and remained the world's fastest computer until 1990. [5] After that, Cray Research designed Cray-3 that used GaAs technology to faster the speed. [1]

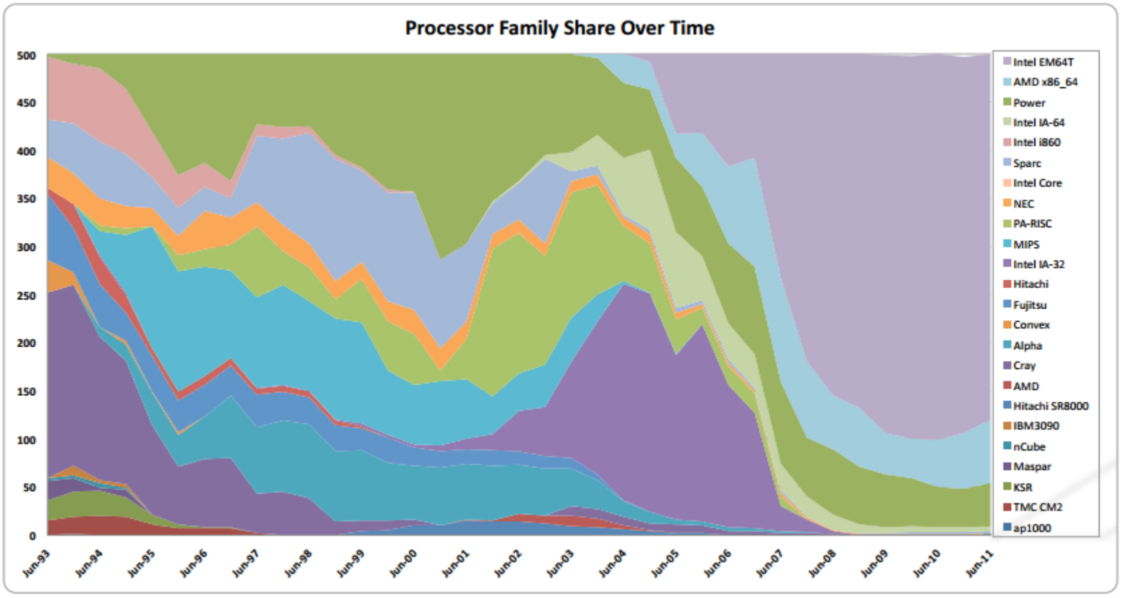

Figure 4. Processor Families in TOP500 Supercomputers [10]

In 1990, multiple computers with thousands of processors began to appear. [7] The National Aerospace Laboratory of Japan and Fujitsu designed a joint project and released the Numerical Wind Tunnel supercomputer that had 166 vector processors, two control processors, Crossbar Networks, and 256 MB main memory with high speed of 1.7 giga floating point operations per second for each processor. [8] After a while, another supercomputer appeared in Japan called the Hitachi SR2201 with 2048 processors that perform 600 giga floating point operations per second. [9] Nowadays, the Chinese supercomputer, named Tianhe-2, still the fastest computer in the world at 33.86 Petaflops or thousand trillion floating point operations per second. [11]

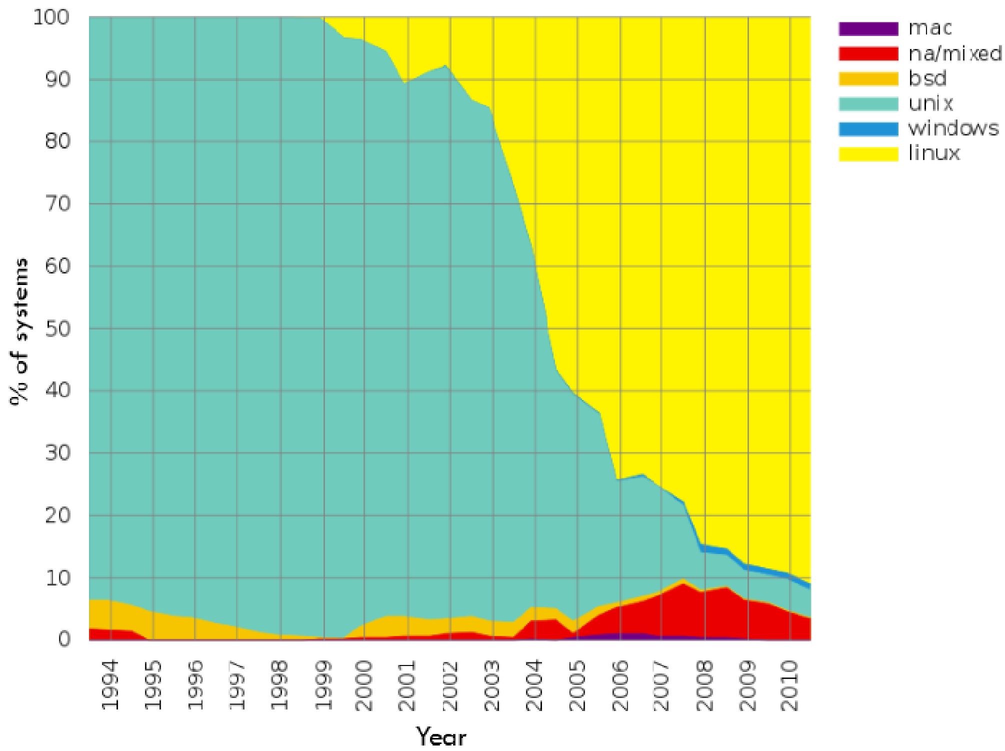

Figure 3. OS in TOP500 Supercomputers [10]

Architecture of Supercomputing:

To increase the performance, the hardware architecture determines the possibilities and impossibilities in increasing the speed of a computer system beyond the performance of a single CPU. In addition, the capability of compilers is the combination of CPUs and hardware that can be used to generate efficient code to be executed on the given hardware platform. For a long period of time, the categorization of high performance computers is useful from the Flynn's taxonomy 1966. Manipulating of instructions and data streams at the parallelism are the basic techniques for the categorization. Moreover, the categorization consists of four main types, which are single instruction, single date (SISD), single instruction, multiple date (SIMD), multiple instruction, single data (MISD), multiple instruction, multiple data (MIMD). [10][12]

SISD machines are the uniprocessor category where the systems contain only one CPU and can accommodate one instruction stream that is executed serially. Such examples of workstations that implement SISD class are Hewlett-Packard and IBM. [10][12]

SIMD systems have a large number of processing elements, from 1024 to 16384, that execute the same instruction on multiple data simultaneously. Thus, a single instruction may manipulate many data elements in parallel. The approach of this class is named data-level parallelism. For instances of SIMD machines in this class are Quadrics Apemille and CPP Gamma II. SIMD methods is returned in the last few years as a co-processor in HPC in the game markets with the significant growing of Graphical Processing Unit (GPU). They are used to build three-dimensional real-time virtual environments. [10][12][13]

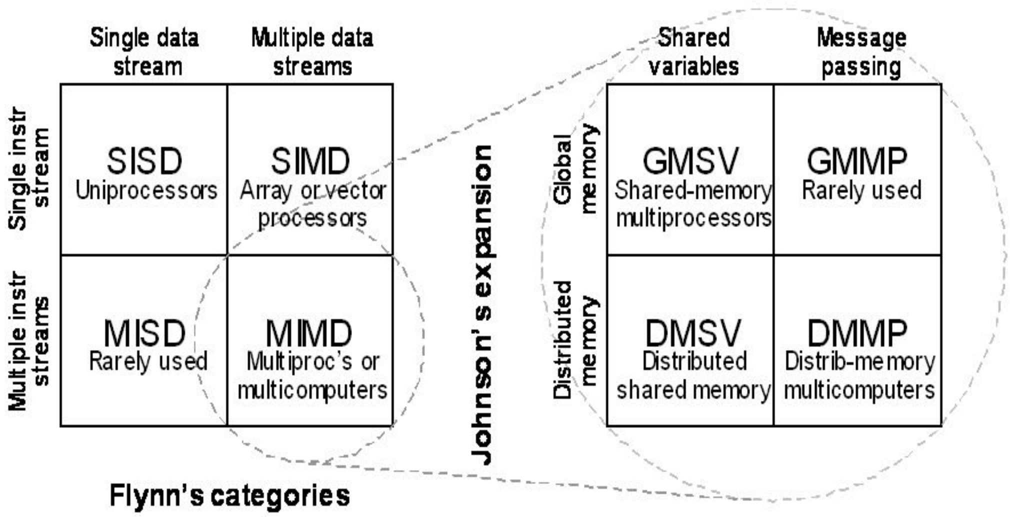

Figure 4. Flynn's Taxonomy [13]

MISD machines is a theoretical approach because multiprocessors with this features are not constructed yet. Multiple instructions should be processed on a single stream of data. [10][12]

MIMD systems execute many instructions in parallel on different data. The difference between multi-processors SISD machines and MIMD are the relationships between instructions and data because machines will execute several parts of the same task. MIMD machines will run many subtasks in parallel to shorten the execution time for the core task. This approach is called thread-level parallelism, which are more flexible than data-level parallelism used in SIMD. [10][12]

MIMD systems may function as single-user multiprocessors focusing on high performance for one application and can build on the cost-performance advantages of off-the-shelf processors. For examples, a system that use this approach is the 100 000-processor IBM Blue-Gene/P. [10][12][13]

Shared Memory Architecture:

Shared-Memory Architecture (SMA) have multiple Central Processing Units (CPUs), where several processors share the same memory address. This architecture is also called Uniform Memory Access (UMA), and is currently considered the most popular one. This means that the memory is equally shared to all processors with the same performance of access. Shared-Memory Architecture can be SIMD or MIMD. The major characteristics of SMA over different types of multi processors is that all processors share the same amount of memory. There are two main types of SMA: Uniform Memory Access (UMA) and cache-coherent Non Uniform Memory Access (ccNUMA). [12][13][14]

Uniform Memory Access (UMA) are used in parallel computers. In UMA, the same memory address is physically shared among all processors and equally available to them. The processors might be having a local memory space, called cache memory. In the UMA architecture, access time is independent from the memory location in which each processor creates a request, or in which memory chip contains the transferred data. The architecture of UMA is contrasted with the architecture of ccNUMA. This model is appropriate for general purposes and time sharing applications by multiple users. The UMA can be used to increase the execution speed of a single large program in critical time of applications. [10][12][13][14][15]

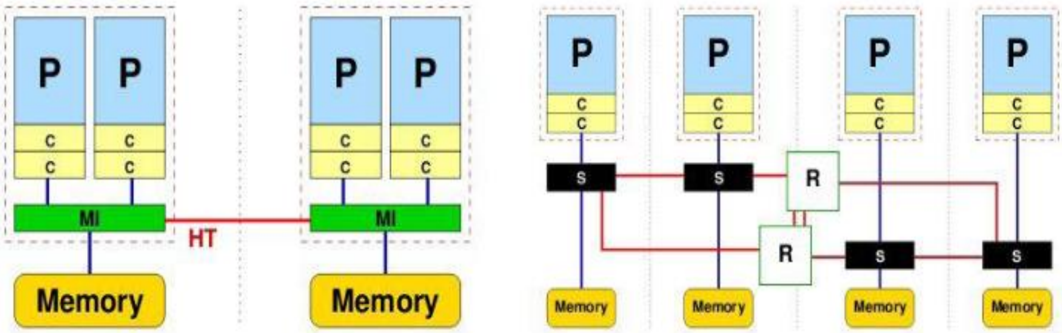

Figure 5. cache-coherent Non Uniform Memory Access (ccNUMA) [10]

In cache-coherent Non Uniform Memory Access (ccNUMA), the inner processors are used to communicate between cache controllers to keep consistent when more than cache memory use the same memory location. The memory is appeared as a single memory address space and distributed among processors. Because of this distribution, the ccNUMA machines cannot be guaranteed that the data that access operations will always be fulfilled within the same time. The ccNUMA performance differs between the local and remote access to the memory. All memory is directly accessible by all processors without transferring data explicitly; and is viewed and addressed globally. [12][13][14][15]

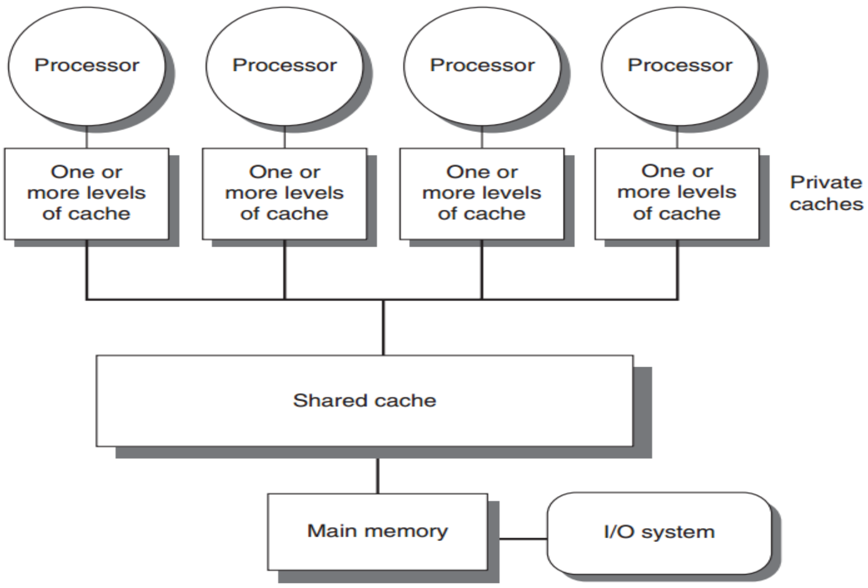

Figure 6. Basic structure of a centralized shared-memory multiprocessor [12]

Distributed Memory Architecture:

In distributed memory architecture, each processor has its own memory and they are connected to exclusive local memory throughout some networks in order to exchange the data between the corresponding memories. The users must be aware of the location of the data in the local memories and will have to distribute these data explicitly when needed. There are not global cache coherent shared with address spaces, which is called no remote memory access. [10] [12][13]

Distributed memory machines can be either SIMD or MIMD systems with a vector or scalar nodes. The data is exchanged over the available processors, named nodes, by sending a message throughout the network. There are two major parts of the distributed memory systems: Massively Parallel Processing (MPP) and cluster computing; each of them has its own programming model. The architecture for this type is similar to the architecture of the clusters but it has large shared memory processing. [10] [12][13][14]

Massively Parallel Processing (MPP) is the collaborative processing of the same program by two or more processors, each one handles different parts of the program, and each processor has its own dedicated memory and operating systems. MMP systems have very large numbers of processors linked together using a special purpose of processor-to-processor inter-connection. Messaging interface is required to allow the variant processors included in the MPP to arrange the communications.

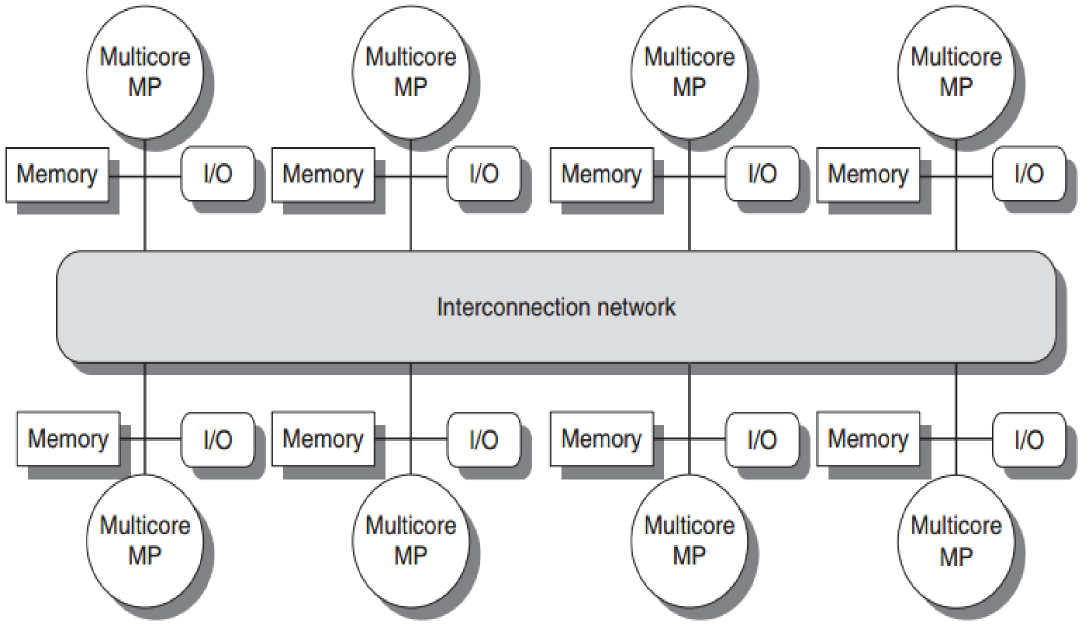

Figure 7. The basic architecture of a distributed-memory multiprocessor in 2011 [12]

MPP systems are considered to be better than shared memory processor systems for applications that allow a number of databases to be searched in parallel, including decision support system and data warehouse applications. [10] [12][13][14]

In Massively Parallel Processing (MPP), Over than two hundreds processors can work on the same application. An interconnection of data paths allows messages to be sent over all processors. The setup of MPP is more complicated, requiring about how to partition common databases among processors, and how to assign a mission among the processors. MPP systems are known as loosely coupled or shared nothing system. Special nodes can have peripherals, such as disks or a backup connection. [10] [12][13][14]

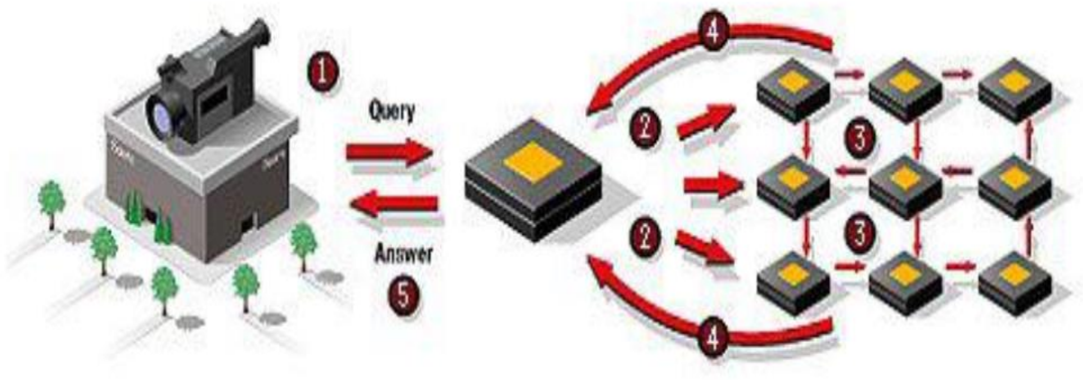

Figure 8. Massively Parallel Processing (MPP) [10]

Clusters are the important part in supercomputing architecture and can provide high available computing platforms. Cluster are a group of coordinated servers to provide scalable and high services actions. [23][24] Clusters are linked together through a network to work on one or more systems, but cannot access the memory of remote systems. [23]

There are two main types of supercomputing clusters: High Performance and High Throughput Clusters, which are used to increase the computer capability in the applications; and High availability Clusters, which are used to keep the clusters' services available without failing.

Cluster computing is a type of parallel or distributed processing systems that consists of collections of interconnected stand-alone computers cooperatively working together as a single computer, integrated computing resource. This means that it is a form of computing in which a group of computers are linked together to act as a single computer. Typical cluster computers consists of fast LANs network to faster and closer the connections, looser connection, and low latency communication protocols. Thus, it is relies heavily on network speed, and the upgrade is easily done with addition of new systems. [11][14][13]

Each node within a cluster in cluster computing is an independent system with its own file system. The processor of a computer cannot directly access to the memory of the other computers, programs, or software run on the clusters. Cluster nodes are accessible with 4 to 8 processors where each processor may have up to 12 processor cores. In addition, clusters have more than one servers that share the memory information together, and theses servers are connected to each other with fast local area networks. [11][12][13][14]

Hybrid Distributed-Shared Architecture:

The largest and fastest supercomputer in the world exploits both distributed and shared memory architectures. The distributed components is the networks of multiple shared memory processors whereas the shared memory components are a cache coherent shared memory processors. The network communications in the distributed memory components are needed to transfer data from one shared memory to another. [10][12]

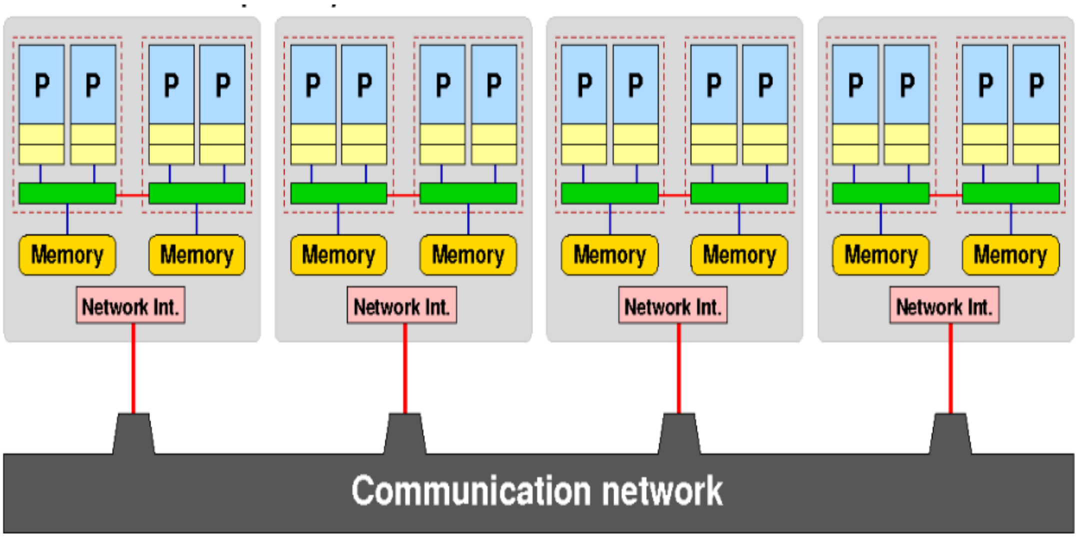

Figure 9. Hybrid Distributed-Shared Architecture [10]

Usage of Supercomputing:

The supercomputing is experiencing a lot of changes. It refers to the IT world's parts that require high performance systems for intensive of computation or intensive of data applications in technical computing. At present, the term high performance computing covers a wide range of platforms and computing environment, and the level of diversity is growing. The powerful off-the-shelf silicon, software, and networking technology is changing the landscape very quickly. This includes computational applications in bioinformatics, engineering, and climate.

The simulation with high performance computing can be a strength for the innovations of having answers to the challenges and opportunities. For example, "Farmers around the world are trying to cope with climate changes and need plant varieties that can withstand droughts, floods, diseases and insects. And many farmers are shifting to crops tailored for biofuels—that is, fuels made from renewable resources like cellulose, starch or other plant matter. But conducting experiments to determine the performance of new hybrids takes a long time, requiring many years to study the potential of new hybrids in thousands of experiments conducted in different farm management conditions." [16]

Another usage of HPC Supercomputers is in the changes the nature of biomedical research and innovation, from a science that depend on observation to a science that depend on HPC to achieve impossible quantitative results. For instance, ""It took high performance computing to reveal how limited our concept was of how synapses functioned," Sejnowski explains. "It appears there is a second channel outside the active zone of synapses that may be used to process different types of information. While we had been aware of these "extra-synaptic" receptors, we really had no idea until now what they were for. But now we are beginning to understand that there is a completely separate mode of neural communication, perhaps going on in parallel with the synapse, which was not apparent until we ran the supercomputer simulations." New experiments conducted by other researchers seem to support the Salk team's unconventional findings." [17]

An important use of HPC is trying to design a device that mechanically remove blood clots associated with a stroke. For example, "Medrad used HPC at two critical points in their research and development. Initially, it was employed to investigate the physics of the catheter intervention device in relation to the blood vessels (vasculature) where a clot had to be broken up or removed. In other words, Medrad used HPC to simulate the process of the catheter destroying the clots, adjusting the parameters again and again to ensure that the phenomenon was repeatable. This validated that the science behind the patent's theory was solid and that the device would do what its inventors claimed. Then HPC was used to mathematically refine the prototypes by simulating many different combinations of changes – more than could be done physically in the time frame or budget available – to arrive at the best design. "Using the PSC supercomputer," Kalafut says, "we have been able to look at multiple iterations of different design parameters without building numerous, expensive prototypes." . . . As a result, Medrad is confident that they can manufacture the device." [18]

Applications of Supercomputing:

Supercomputers are so powerful tool that can help researchers with different phenomena that help them to observe in their research laboratories, but they may take several months for some parts of the observation. The application software available for the supercomputers are very few, because the applications have to run in parallel which makes the programming for these supercomputers more difficult. [19]

Because of this limitation in the application of high performance computers, the developed applications that work for parallel computers are custom designed by the end users. These program applications are written in MATLAP, high level application. After that, programmers develop programs written in C or FORTRAN and message passing interface to let these programs work in parallel and use the communications between processors. At the end, the supercomputer can execute real data to test the results. Nowadays, many scientist and engineers are involved in the applications of the high performance computing [19]

Researchers are exploring additional applications of high performance computing. They are constantly investigating for new applications such as data mining, which is an application that look for hidden patterns. They try to use these data mining applications to discover the unknown relationships between information. [20]

The Fastest Supercomputer in the World:

“Every year, in June and in November, the Top500 list shows which supercomputers can crank out the most calculations per second.” [11] The top machine in the Top500.org’s list of supercomputers is Tianhe-2 that is installed at the National University of Defense Technology (NUDT) in Guangzhou, China. These days, this supercomputer is the world’s most powerful computer and is the technological

Figure 10. Tianhe-2 Supercomputer [11]

successor of Tianhe-1A, which was installed at National Supercomputer Center in Tianjin, China. [11][21]

Capability of the Chinese “Tianhe-2 Supercomputer”:

Tianhe-2 is also called the Milky Way-2, which consists of 16 000 nodes. Inside each node, two Intel Xeon Ivy Bridge processors and three Xeon Phi processors run the show, adding up to a total of 3.12 million computing cores. The machine is scheduled to be fully operational by the end of 2015. [11]

“Tianhe-2 consists of 16,000 nodes each of which has 2 Intel Xeon Ivy Bridge processors and 3 Xeon Phi co-processors, to accelerate the calculations. This makes a total of 3,120,000 computing cores, 384,000 Xeon Ive Bridge cores and 2,736,000 cores in the Phi coprocessors. It is a novelty that it has 3 coprocessors per node, usually there are one or two. These cores provide to Tianhe-2 a theoretical peak performance running mathematical operations of 54.9 PFLOPS (Peta = 10 ^ 15 Floating-point Operation Per Second, 1,000,000,000,000,000 mathematical operations per second) and with the LINPACK benchmark the real performance reaches 33 .9 PFLOPS, which almost doubles the previous record of the Titan supercomputer located at the Oak Ridge National Laboratory (ORNL) in Tennessee. [21]

In addition, “according to NUDT, Tianhe-2 will be used for simulation, analysis, and government security.” [22] “The interconnection network between the nodes, namely TH Express-2, is a proprietary design firstly installed in Tianhe-2 and tries to avoid communications bottlenecks thanks to its bidirectional bandwidth of 16 GB/s, low latency and fat tree topology. Tianhe-2 uses the Kylin operating system based on Linux optimized for high performance computing and also developed by the NUDT. Being based on a standard Linux Kylin gives great flexibility to run many codes without specifically reprogram them.” [21]

RANK	SITE	SYSTEM	CORES	RMAX (TFLOP/S)	RPEAK (TFLOP/S)	POWER (KW)
1	National Super Computer Center in Guangzhou China	**Tianhe-2 (MilkyWay-2)** - TH-IVB-FEP Cluster, Intel Xeon E5-2692 12C 2.200GHz, TH Express-2, Intel Xeon Phi 31S1P NUDT	3,120,000	33,862.7	54,902.4	17,808
2	DOE/SC/Oak Ridge National Laboratory United States	**Titan** - Cray XK7 , Opteron 6274 16C 2.200GHz, Cray Gemini interconnect, NVIDIA K20x Cray Inc.	560,640	17,590.0	27,112.5	8,209
3	DOE/NNSA/LLNL United States	**Sequoia** - BlueGene/Q, Power BQC 16C 1.60 GHz, Custom IBM	1,572,864	17,173.2	20,132.7	7,890
4	RIKEN Advanced Institute for Computational Science (AICS) Japan	K computer, SPARC64 VIIIfx 2.0GHz, Tofu interconnect Fujitsu	705,024	10,510.0	11,280.4	12,660
5	DOE/SC/Argonne National Laboratory United States	**Mira** - BlueGene/Q, Power BQC 16C 1.60GHz, Custom IBM	786,432	8,586.6	10,066.3	3,945
6	Swiss National Supercomputing Centre (CSCS) Switzerland	**Piz Daint** - Cray XC30, Xeon E5-2670 8C 2.600GHz, Aries interconnect , NVIDIA K20x Cray Inc.	115,984	6,271.0	7,788.9	2,325
7	Texas Advanced Computing Center/Univ. of Texas United States	**Stampede** - PowerEdge C8220, Xeon E5-2680 8C 2.700GHz, Infiniband FDR, Intel Xeon Phi SE10P Dell	462,462	5,168.1	8,520.1	4,510
8	Forschungszentrum Juelich (FZJ) Germany	**JUQUEEN** - BlueGene/Q, Power BQC 16C 1.600GHz, Custom Interconnect IBM	458,752	5,008.9	5,872.0	2,301
9	DOE/NNSA/LLNL United States	**Vulcan** - BlueGene/Q, Power BQC 16C 1.600GHz, Custom Interconnect IBM	393,216	4,293.3	5,033.2	1,972
10	Government United States	Cray XC30, Intel Xeon E5-2697v2 12C 2.7GHz, Aries interconnect Cray Inc.	225,984	3,143.5	4,881.3	

Figure 11. TOP 10 Supercomputers in 2014 [22]

Future of Supercomputers:

The future of high performance computers includes modeling and installing of the next generation of research for computational infrastructure and the introduction to the new architecture of supercomputing. Moreover, we have to find all possible ways that we need to assemble the multiple processors, distributed and shared memory, and communications parts in the supercomputers. The human desires to have the best capabilities to execute large numbers of floating point operations will continue to increase in the next generations. In addition, Supercomputing applications will be developed to achieve the required implementation. [20]

United States, Chinese, Japan, and Europe are racing to have the fastest computer in the world. In the United States, the Department of Energy are designing two supercomputers with a peak of 150 to 300 peta floating point operations per second, which is 300 quadrillion calculations per second. They named it “Summit” and it is five times faster than the fastest supercomputer in this day, Tianhe-2. This supercomputer will be installed at the Oak Ridge National Laboratory in Tennessee. [25]

In addition, the United States are also designing another supercomputing with a peak of more than 100 peta floating point operations per second. They called it “Sierra” and will be installed at Lawrence Livermore National Laboratory at IBM. These two supercomputers will cost $325 million to build and will be completed in 2017. They are 5 to 10 times faster than the performance of Tianhe-2, and will be used for the energy efficiency purposes. [25]

Conclusion:

To conclude, High performance computing is a significant branch in computer science field. In this paper, I starts with the history of supercomputers that derives what we have in these days. Seymour Cray was the founder for this new concept, and he designed more than two brilliant supercomputers. After that, I explained in detail the architecture of the highest performance computing, which are shared memory architecture (SMA), distributed memory architecture, and hybrid architecture; and the important feature for each one and how they work. Then, I demonstrated the common uses of the supercomputers. And then I briefly explained the applications used in the high performance computers. Next to that, I illustrated about the fastest supercomputer, Tianhe-2, in the world with its capability of performance. Finally, I wrote about the future supercomputers and their performance.

I am proud of reading about this topic and writing a term paper about it by using a lot of references including, books, papers, and websites. I learned new information about the supercomputing technology used in the world. I hope it is readable and understandable for non-professional readers.

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