Computer organization

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plan for the day

- computer organization
  - central processing unit
  - main memory
  - cache memory
- case study: matrix multiplication
- using Git
- `printf("hello, world\n");`

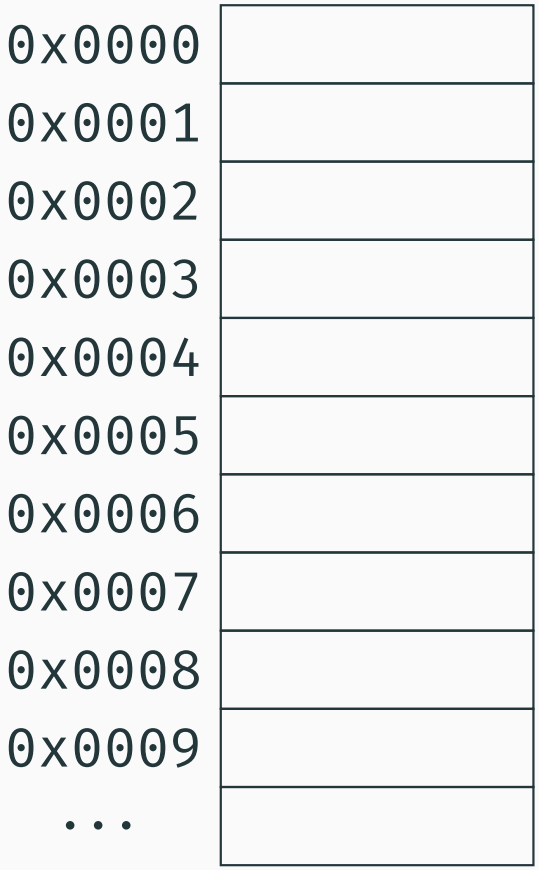
central processing unit (CPU)

what does memory look like?

memory organization

- memory is organized sequentially

memory organization



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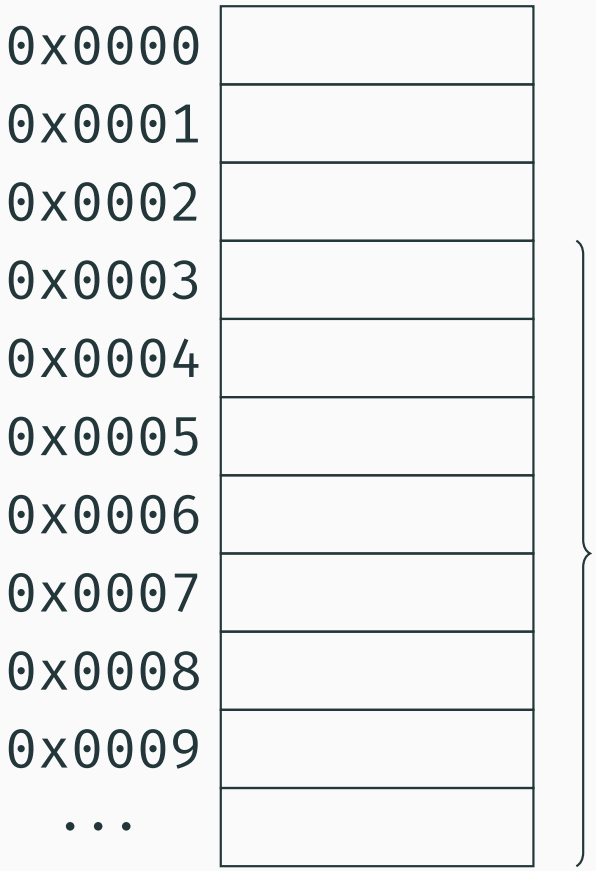
- memory is addressed starting from the *top*
    - granularity is a byte

memory organization



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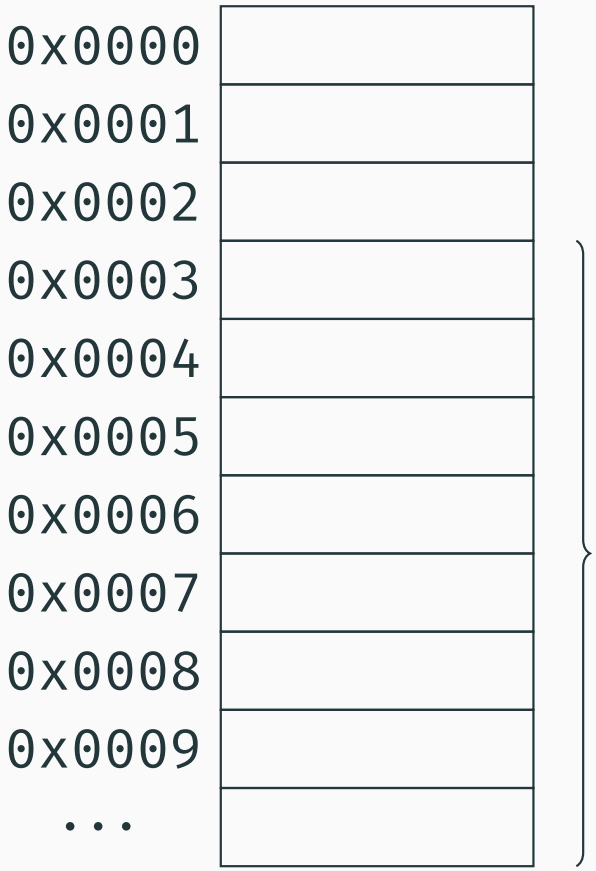
memory organization



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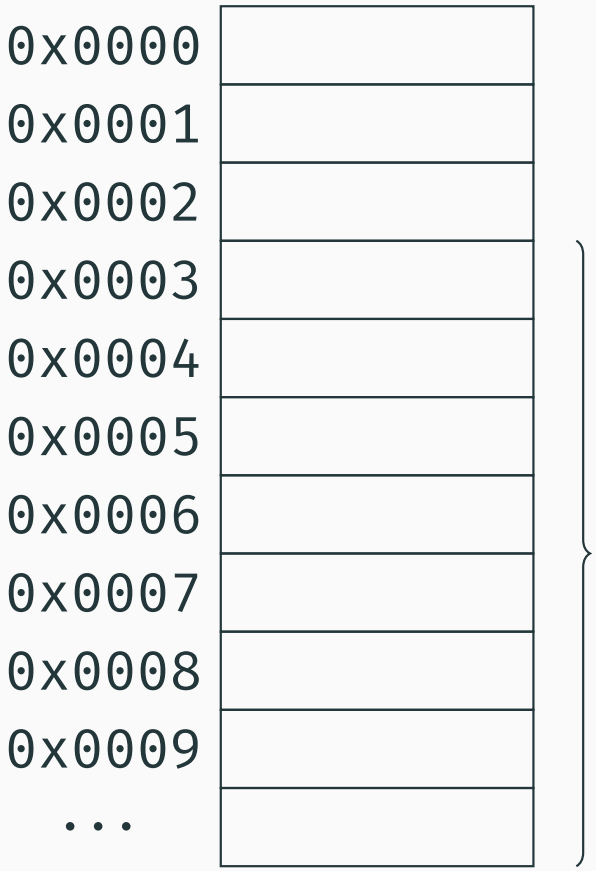
memory organization



- memory is organized sequentially
- memory is addressed starting from the *top*
  - granularity is a byte
- a process and its data can be stored anywhere in memory
  - physical vs. logical addressing
  - each process has its own *address space*

cache memory

- what is it?

cache memory

- a high-speed memory co-located with the CPU on the chip

cache memory

- a high-speed memory co-located with the CPU on the chip
- what problem is cache addressing?

cache memory

- a high-speed memory co-located with the CPU on the chip
- CPU can compute faster than memory can be fetched
  - many problems reuse data or use data that is stored near each other in memory, known as *temporal* and *spatial* locality, respectively

cache memory

- a high-speed memory co-located with the CPU on the chip
- CPU can compute faster than memory can be fetched
  - many problems reuse data or use data that is stored near each other in memory, known as *temporal* and *spatial* locality, respectively
- how does it work?

cache memory

- a high-speed memory co-located with the CPU on the chip
- CPU can compute faster than memory can be fetched
  - many problems reuse data or use data that is stored near each other in memory, known as *temporal* and *spatial* locality, respectively
- when memory load is issued, cache is checked to see if the data exists there. if not, it is loaded from main memory and stored in cache. when cache becomes full, old data is evicted to make room for new.

cache memory

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- how much is there?

cache memory

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- CPU can compute faster than memory can be fetched
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- multiple levels of cache, each larger than the previous, but all much smaller than main memory

cache performance

From Intel Performance Analysis Guide:

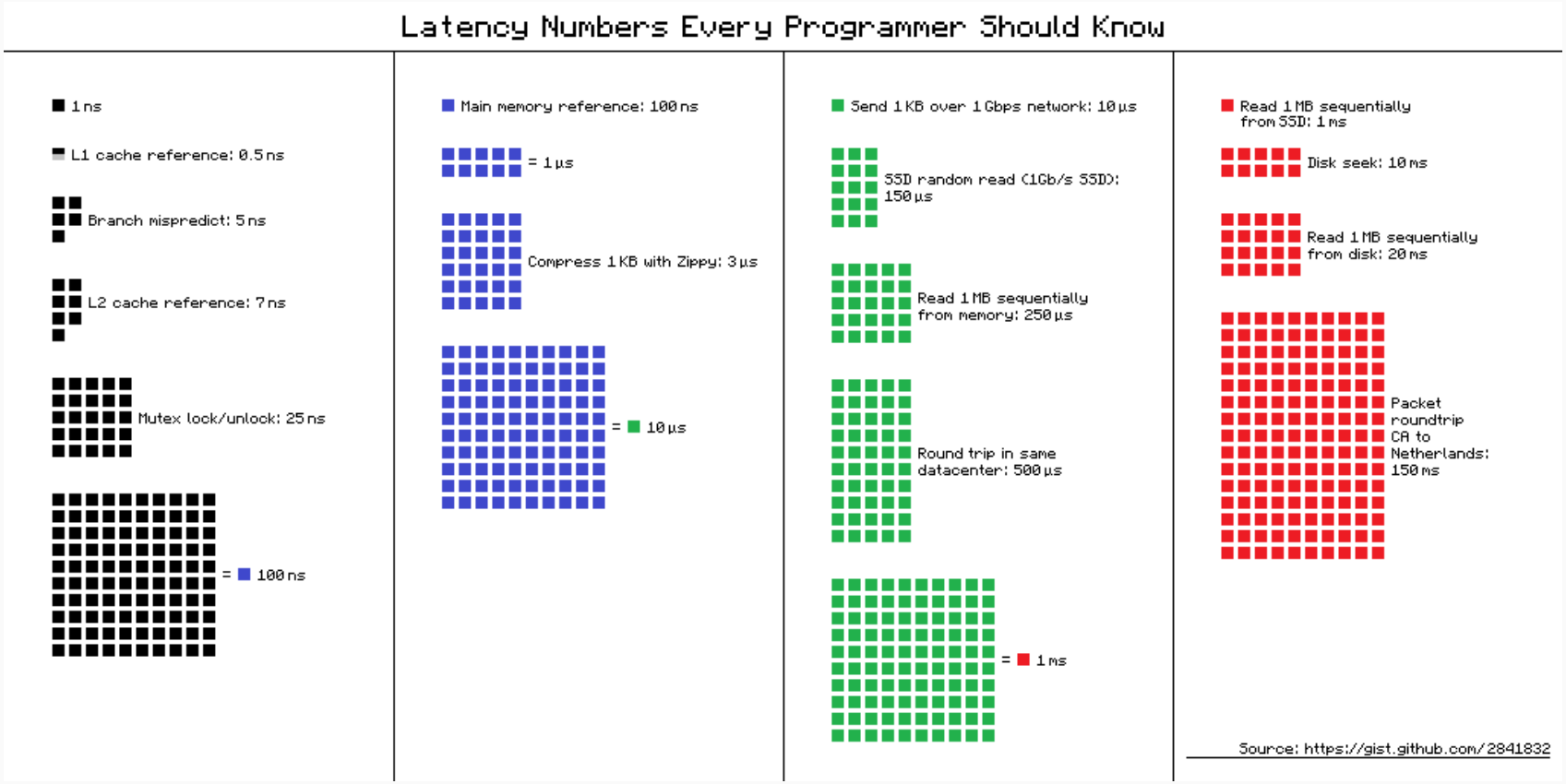
```
Core i7 Xeon 5500 Series Data Source Latency (approximate)              [Pg. 22]

local  L1 CACHE hit,                                ~4 cycles (   2.1 -  1.2 ns )
local  L2 CACHE hit,                               ~10 cycles (   5.3 -  3.0 ns )
local  L3 CACHE hit, line unshared                 ~40 cycles (  21.4 - 12.0 ns )
local  L3 CACHE hit, shared line in another core   ~65 cycles (  34.8 - 19.5 ns )
local  L3 CACHE hit, modified in another core      ~75 cycles (  40.2 - 22.5 ns )

remote L3 CACHE (Ref: Fig.1 [Pg. 5])         ~100-300 cycles ( 160.7 - 30.0 ns )

local  DRAM                                                    ~60 ns
remote DRAM                                                   ~100 ns
```

more about latency



Latency Numbers Every Programmer Should Know