Junyi Wu

Permanent Resident Status

junyiwu2003@tamu.edu | (832)792-9723

EDUCATION

Texas A&M University, College of Engineering — College Station, TX

Bachelor of Science in Computer Engineering, Minors in Mathematics — Aug. 2022 - May 2026

GPA: 3.906

- Dean's Honor Roll
- Relevant Coursework: DSA, Digital Systems Design, Electric Circuit, CompArch, Signals and Systems, Computer Systems, **Digital IC Design**, Nand2Tetris, **Microprocessor Systems Design, Advanced CompArch, Fourier Transform**

TECHNICAL SKILLS

Language: C/C++, Python, Verilog, ARMv8 Assembly, Javascript,

Tools/Softwares: Cadence, Arduino, Raspberry Pi, LTSpice, VS Code, Xilinx Vivado, Oscilloscope

EXPERIENCE

Undergraduate Peer Teacher — *Aug. 23-Present*

College of Engineering, *ENGR102, ENGR 216*

- Instruct as a Peer Teacher for Python Coding Classes of 100+ students
- Effectively grade class quizzes and exams, as well as hold weekly office hours for students
- Lead bi-weekly Engineering Physics Mechanics Labs classes of 30+ students
- Supervise mechanics labs and teach students foundational physics concepts

Undergraduate Researcher | *Arduino, Raspberry Pi, Tkinter* — *May. 24-Sep.24*

Research Project - Breathe

- Working with other engineers in designing an Energy-Saving and Air Enhancing System
- Using Arduino and DHT22 sensors to measure outdoor climate and control indoor climates. Returns data to Raspberry Pi for processing and displaying information to users
- Using Tkinter to create an interface for the users to view and adjust climate settings

PROJECTS

8 Bit Pipelined Adder | *Cadence Virtuoso* — *Aug. 24 - Nov.24*

- Designed cmos-level schematics and layouts for an 8-bit pipelined adder using Cadence Virtuoso.
- Performing LVS, DRC, waveform analysis in Cadence and Spectre to optimize capacitance values, improve system throughput and reduce critical path delays, and ensure overall system functionality

6502 Processor Emulation | *C++* — *Dec. 24 - Present*

- Building a cycle-accurate 8-bit CPU emulator in C++, reproducing the 6502 CISC architecture with comprehensive support for registers, flags, and memory management across a 64 KB address space.
- Designing and verifying memory and arithmetic instructions using written testbenches to ensure accurate emulation.

Single Cycle Processor and Control Unit Design| *Verilog* — *Oct.24 - Nov.24*

- Designed and implemented critical components of an ARMv8 single-cycle processor in Verilog, including a 64-bit ALU, control unit, register file, sign extender, and data memory, while supporting instructions.
- Verified functionality through pre-written instruction testbenches, ensuring correct operation of the fetch-execute cycle, and integrated all components into a complete microarchitecture.

Nand2Tetris | *Hack HDL, Hack Assembly* — *Jul. 24*

- Engineered core logic gates and both combinational and sequential circuits—including ALUs, registers, RAM, and a program counter—in Hack HDL.
- Implemented bit manipulation for conditional program counter jumps and ALU operations.
- Integrated all components, including keyboard, screen together to create a 16 bit Computer in Hack HDL

Simple Digital Combination Lock | *Vivado, Verilog, FPGA* — *Apr. 24*

- Designed and implemented a digital combination lock using a Moore FSM on the ZYBO Z7-10 FPGA, with Verilog code to handle a 4-digit binary input sequence.
- Simulated in Vivado, validated functionality with test benches and waveform analysis, and deployed on ZYBO board.