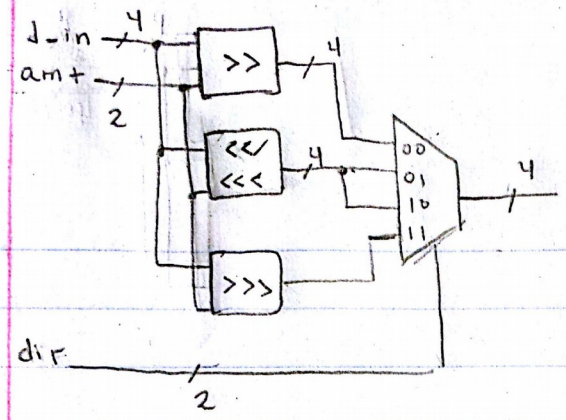


ex)

d_in	d_in >> 2	din << 2	d_in >>> 2	d_in <<< 2
1001	0010	0100	1110	0100
1101	0011	0100	1111	0100
	Logical Right	Logical Left	Arith. Right	Arithmetic Left

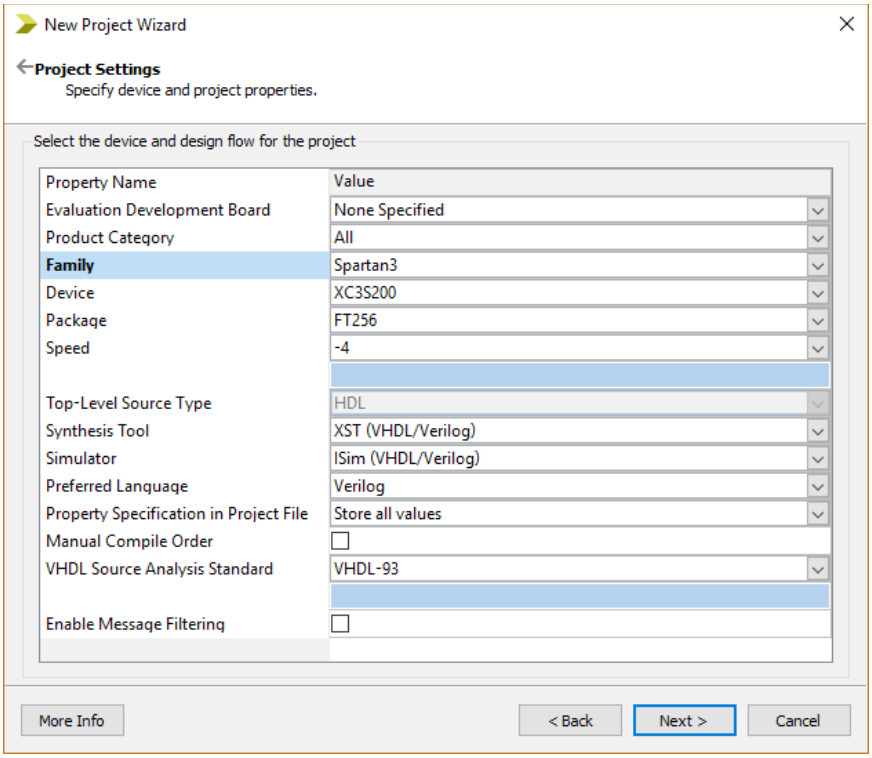
3 2 1 0

[1 0 0 1] Little Endian Notation

amt	shift by
00	1
01	2
10	3
11	4

sel	
00	logic_right
01	left
11	left
10	arith_right

Default Settings



Implementation

4. Implment Verilog on FPGA Spartan3.

4a. On top of the design panel, switch the view to "Implementation".

4b. Double click "Synthesize -XST". If green check shows, the process succeeds and move to next step; otherwise read the error message and revise your design modules.

4b. Double click "Implement Design". If green check shows, the process succeeds and move to next step;

otherwise read the error message and revise your design modules or your ucf file. If this process succeeds, a .bit file will be generated successfully.

STOP HERE AT HOME)

4c. Before proceeding to "Configure Target Device", connect your FPGA board to the computer through JTAG programming cable. Then double click "Configure Target Device"

4d. In the new pop up window, double click on "“ Boundary Scan" on the top left corner.

4e. In the white area to the right, right-click and choose “Initialize chain”

4f. In the dialog “Assign new configuration file” choose your .bit file, and then choose “Bypass” from

next dialog.