

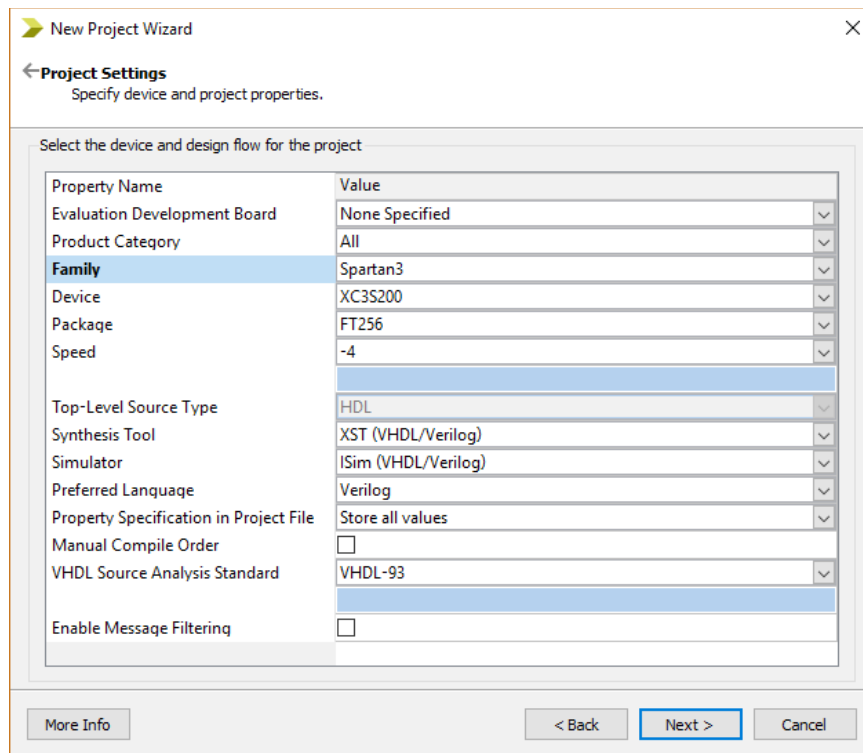
ex)	d-in	d-in >> 2	d-in << 2	d-in >>> 2	d-in <<< 2
	1001	0010	0100	1110	0100
	1101	0011	0100	1111	0100
		Logical Right	Logical Left	Arith. Right	Arithmetic Left

PIC 16C44 3 2 1 0

Little Endian [1 0 0 1] Little Endian Notation

amt	shift by	sel	
00	1	00	logic-right
01	2	01	left
10	3	11	left
11	4	10	arith-right

Default Settings



The image shows the 'New Project Wizard' dialog box, specifically the 'Project Settings' step. The title bar says 'New Project Wizard' with a close button. Below the title bar, there's a back arrow and the text 'Project Settings' and 'Specify device and project properties.' The main area is titled 'Select the device and design flow for the project'. It contains a table with two columns: 'Property Name' and 'Value'. The properties are: Evaluation Development Board (None Specified), Product Category (All), Family (Spartan3), Device (XC3S200), Package (FT256), Speed (-4), Top-Level Source Type (HDL), Synthesis Tool (XST (VHDL/Verilog)), Simulator (ISim (VHDL/Verilog)), Preferred Language (Verilog), Property Specification in Project File (Store all values), Manual Compile Order (checkbox), VHDL Source Analysis Standard (VHDL-93), and Enable Message Filtering (checkbox). At the bottom, there are three buttons: 'More Info', '< Back', and 'Next >', and a 'Cancel' button.

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3
Device	XC3S200
Package	FT256
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

More Info < Back Next > Cancel

Implementation

4. Implement Verilog on FPGA Spartan3.

4a. On top of the design panel, switch the view to "Implementation".

4b. Double click "Synthesize -XST". If green check shows, the process succeeds and move to next step; otherwise read the error message and revise your design modules.

4b. Double click "Implement Design". If green check shows, the process succeeds and move to next step;

otherwise read the error message and revise your design modules or your ucf file. If this process succeeds, a .bit file will be generated successfully.

STOP HERE AT HOME)

4c. Before proceeding to "Configure Target Device", connect your FPGA board to the computer through JTAG programming cable. Then double click "Configure Target Device"

4d. In the new pop up window, double click on "" Boundary Scan" on the top left corner.

4e. In the white area to the right, right-click and choose "Initialize chain"

4f. In the dialog "Assign new configuration file" choose your .bit file, and then choose "Bypass" from next dialog.