Due: Nov 7^{th} 2024

You must show all your work! Answers without supporting work will not be given credit.

All problems are inspired by our Introduction to Logic Design 3rd Edition text.

Only neatly hand-written or typed work will be accepted.

Homework must be in PDF format and should be scanned using, at minimum, a phone camera scanning app.

This homework is worth 10 points.

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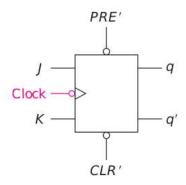
1. Draw both the state diagram and complete the timing sequence as x changes until you have no distinct state information remaining. (1 Point)

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		A B C D	A C A C	В В D В	0 0 0 1	
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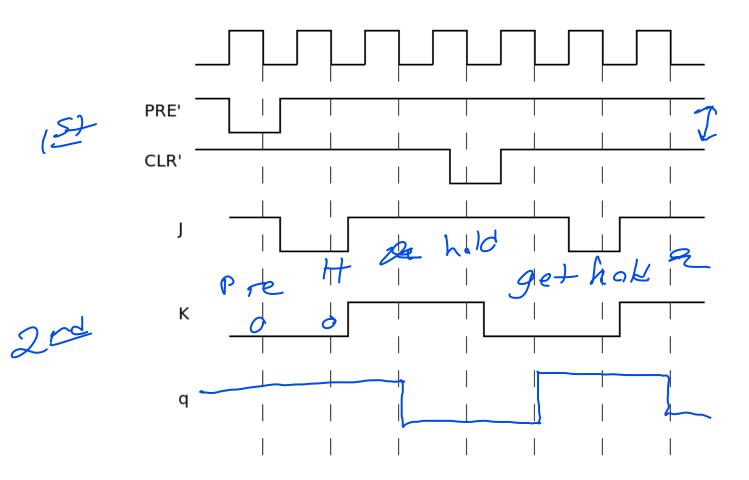
2. Draw both the state diagram and complete the timing sequence as x changes until you have no distinct state information remaining. (1 Point)

	q	x=0	x=1	x = 0	x = 1	
	A B C D	A C A C	B D B D	1 0 0 1	0 0 0	
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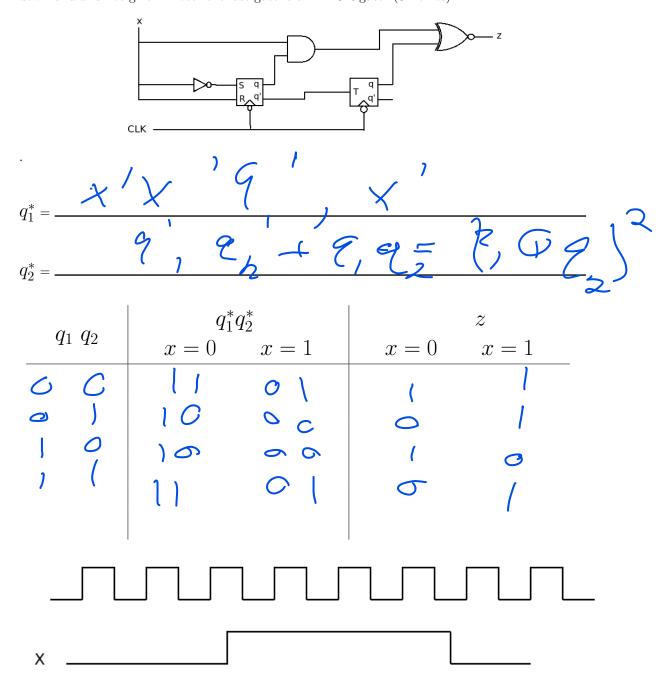
3. Given the following JK flip-flop,



Complete the timing diagram; show the states of \mathbf{q} in a timing diagram. Remember to take the CLR' signal into consideration. Number the clock edges (starting from 1 and then 2, 3, ...) and state the JK's action (HOLD, RESET, SET, or TOGGLE) at each clock edge. (2 Points)



4. Given the following sequential circuit, give the equations for q_1^* and q_2^* (give the unsimplified SoP version for your answer, simplify for yourself as needed), construct the state tables, and use the graphic to complete a timing trace; notice, these are trailing edge flip flops. Assume the circuit begins in $q_1q_2 = 00$ and continue your trace as long as the clock is shown, i.e. you will have one "?" as the clock ticks down and x is not given. Note: the last gate is an XNOR gate. (3 Points)



q2

q1

5. Given the following sequential circuit, provide equations for A^* and B^* (give the unsimplified SoP version for your answer, simplify for yourself as needed), construct a state table, and complete the timing trace until no state information remains. (3 Points)

