EXPT NO. 10 :

STUDY OF J-K FLIP FLOP

Objective :

To study the J-K flip flop.

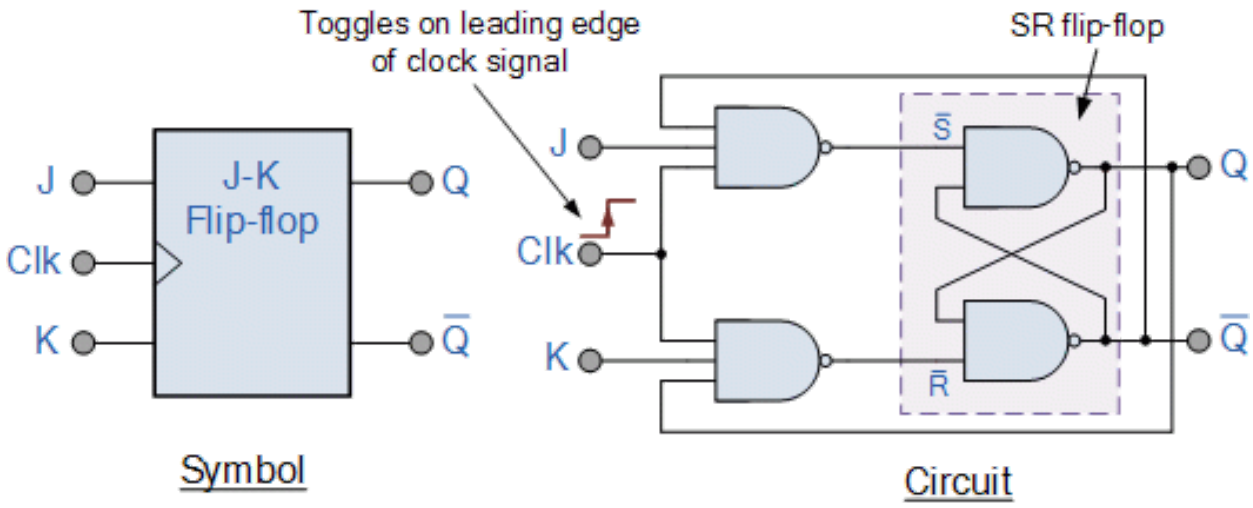
Equipments :

Logic Circuit Simulator Pro.

Theory :

J-K Flip Flop :

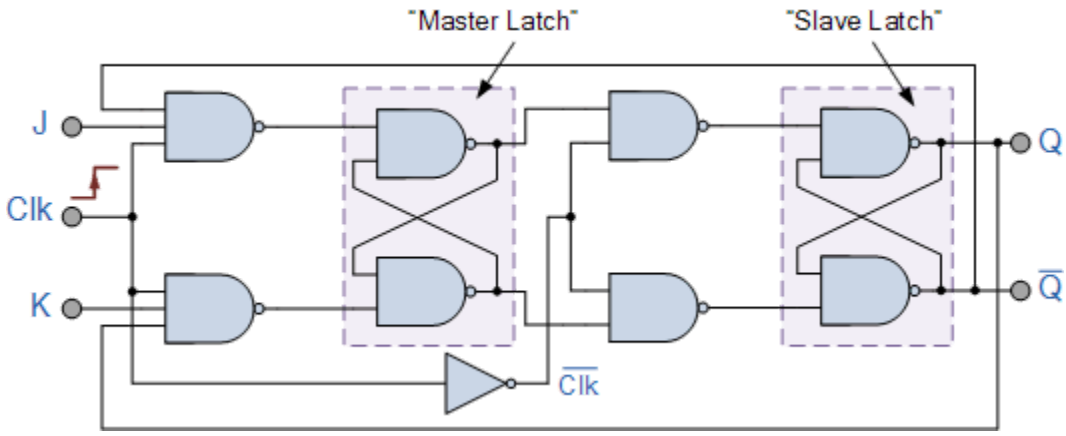
Fig 7(a) shows the clocked J-K flip-flop with clear (CR) and preset (PR) inputs. The small circle (inversion symbols) on these inputs indicates that logic '0' is required to clear or set the flip-flop. Thus the '0' applied to the clear input will reset the flip-flop to Q= 'O', and a 'o applied to the Preset input will set the flip-flop to Q J-K input. I.e. a 'o' applied to the clear input will reset the flip-flop regardless of the values of 1'. These inputs override the clock & J-K, and the clock. Under normal conditions, a 'O' should not be applied simultaneously to clear and preset. When the clear and preset inputs are both held at logic '1', the J, K and clock inputs operate in the normal manner.



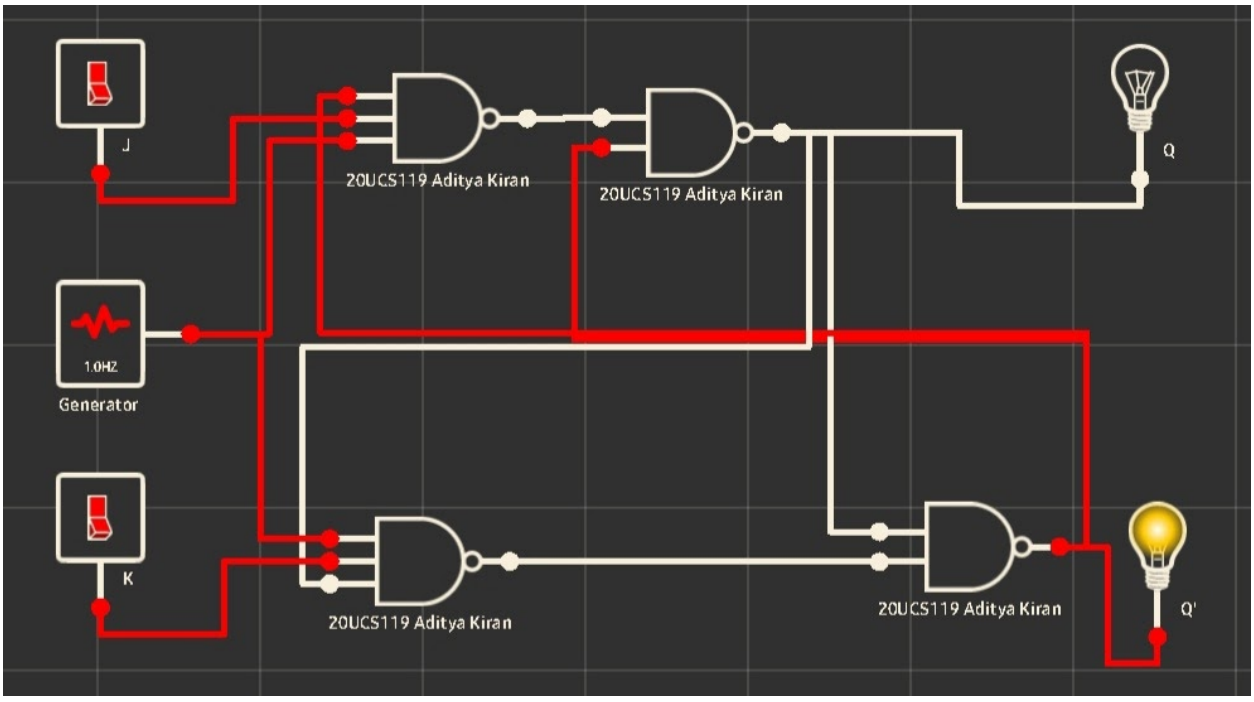
Procedure :

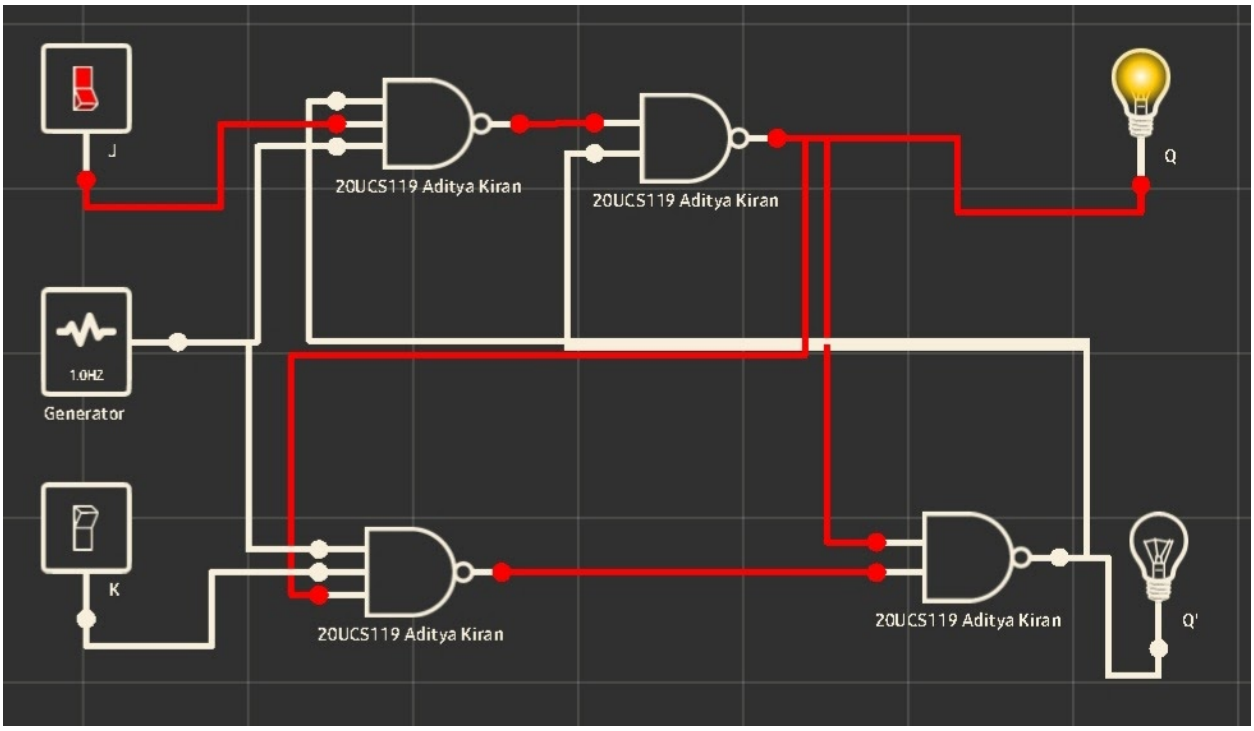
- Do the connection as per block diagram shown below and switch ON the power supply.
- Apply proper logic inputs to the J-K flip flop and observe the output on LEDs.
- Verify the function table of J-K Flip flop.

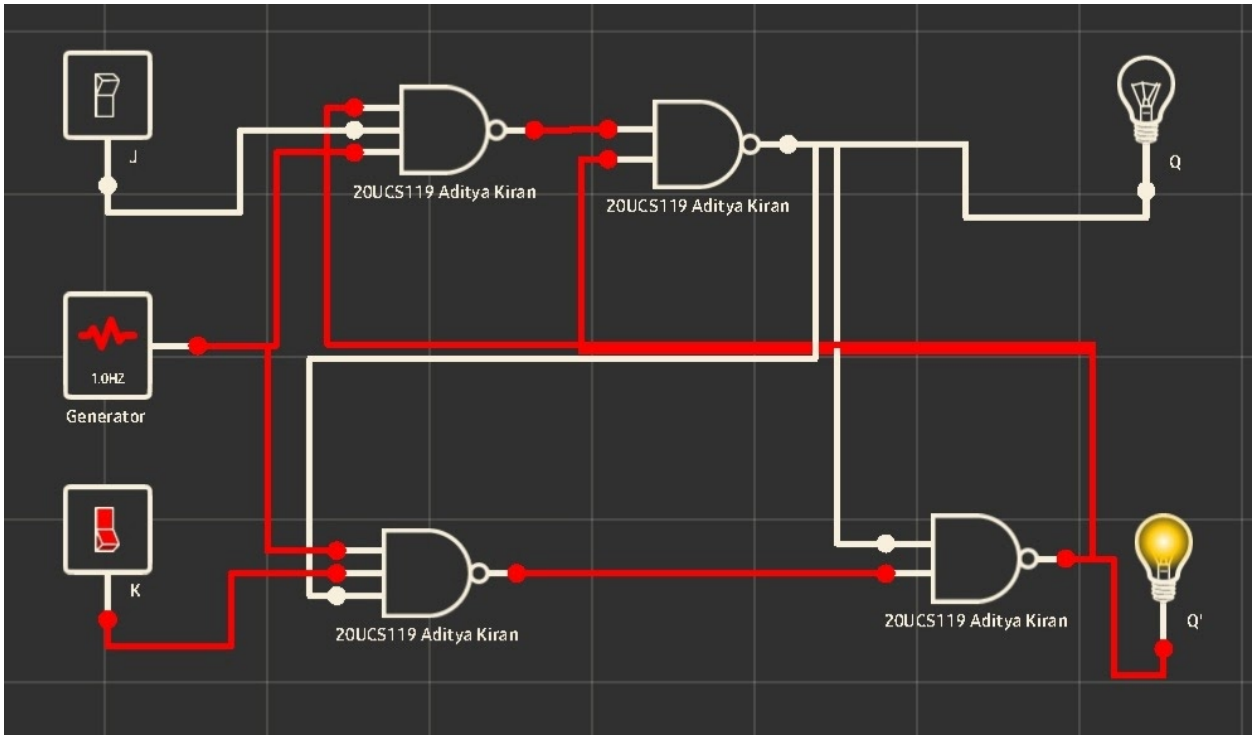
Logic Diagram :



Circuit Diagram :




J
20UCS119 Aditya Kiran
20UCS119 Aditya Kiran
Q
1.0HZ
Generator
K
20UCS119 Aditya Kiran
20UCS119 Aditya Kiran
Q'


J
20UCS119 Aditya Kiran
20UCS119 Aditya Kiran
Q
1.0HZ
Generator
K
20UCS119 Aditya Kiran
20UCS119 Aditya Kiran
Q'

Truth Table :

PR	CL	CLK	J	K	Q	Q'
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	-	-
1	1	1	0	0	Q_0	Q_0'
1	1	1	1	0	1	0
1	1	1	0	1	0	1
1	1	1	1	1	Toggle	
1	1	0	X	X	Q_0	Q_0'

Conclusion :

From the above experiment, we verified the characteristics of J-K flip flop.