B.tech DCLD Lab MCQ test

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DCLD Lab MCQ test

The inputs of a NAND gate are connected together. The resulting circuit is

- ○ OR gate
- ○ AND gate
- ◉ NOT gate
- ○ None of the above

Clear selection

2's complement of binary number 0101 is .....

- ◉ 1011
- ○ 1111
- ○ 1101
- ○ 1110

Clear selection

An AND gate will function as OR if

- ○ All the inputs are ‘0’
- ○ All the inputs to the gates are “1”
- ○ Either of the inputs is “1”
- ◉ All the inputs and outputs are complemente'

Clear selection

Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?

- ◉ Two 2 input AND gates
- ○ b) Two 3 input AND gates
- ○ c) Two 2 input OR gates
- ○ d) Two 3 input OR gates

Clear selection

NAND. gates are preferred over others because these

- ○ have lower fabrication area
- ◉ can be used to make any gate
- ○ consume least electronic power
- ○ provide maximum density in a chip.

Clear selection

What must be used along with synchronous control inputs to trigger a change in the flip flop?

- a) 0
- b) 1
- c) Clock
- d) Previous output

Clear selection

What will be the output from a D flip – flop if the clock is low and D = 0?

- 0
- 1
- No change
- Toggle between 0 and 1

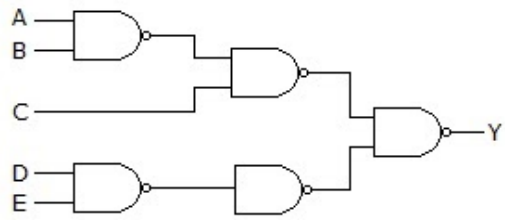
Clear selection

What kind of operation occurs in a J – K flip flop when both inputs J and K are equal to 1?

- a) Preset operation
- b) Reset operation
- c) Clear operation
- d) Toggle operation

Clear selection

Q30. The circuit of the given figure realizes the function .....



1. $Y = (\overline{A} + \overline{B})\,C + \overline{DE}$

2. $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$

- (●) Option 1
- ( ) Option 2
- ( ) AB+C+DE
- ( ) AB+C(D+E)

Clear selection

The basic storage element in a digital system is .....

- (●) flipflop
- ( ) counter
- ( ) multiplexer
- ( ) encoder

Clear selection

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