# Virtual Memory: Just an Illusion

Hung-Wei Tseng

#### Let's dig into this code

```
int main(int argc, char *argv[])
    int i,j;
    double **a;
    double sum=0, average;
    int dim=32768;
    if(argc < 2)
        fprintf(stderr, "Usage: %s dimension\n", argv[0]);
        exit(1);
    dim = atoi(argv[1]);
    a = (double **)malloc(sizeof(double *)*dim);
    for(i = 0 ; i < dim; i++)
        a[i] = (double *)malloc(sizeof(double)*dim);
    for(i = 0 ; i < dim; i++)
        for(j = 0 ; j < dim; j++)
            a[i][j] = rand();
    for(i = 0 ; i < dim; i++)
        for(j = 0 ; j < dim; j++)
            sum+=a[i][i];
    average = sum/(dim*dim);
    fprintf(stderr, "average: %lf\n", average);
    for(i = 0 ; i < dim; i++)
        free(a[i]);
    free(a);
    return 0;
```



#### What will happen?

- If we execute the code on the right-hand side code on a machine with only 16 GB of physical memory installed and the dim is "48000" (requires 48000\*48000\*8 bytes ~ 18 GB memory at least), What will happen?
  - A. The program will crash in one of the malloc function call
  - B. The program will crash due to a "segmentation fault" that caused by accessing NULL pointer
  - C. The program will be killed automatically by the OS as it uses more than installed physical main memory
  - D. The program will finish without any issue

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#### Let's dig into this code

```
#define GNU SOURCE
#include <unistd.h>
#include <stdio.h>
#include <stdlib.h>
#include <assert.h>
#include <sched.h>
#include <sys/syscall.h>
#include <time.h>
double a;
int main(int argc, char *argv[])
    int i, number_of_total_processes=4;
    number of total processes = atoi(argv[1]);
    // Create processes
    for(i = 0; i< number_of_total_processes-1 && fork(); i++);</pre>
    // Generate rand seed
    srand((int)time(NULL)+(int)getpid());
    a = rand();
    fprintf(stderr, "\nProcess %d. Value of a is %lf and address of a is %p\n",getpid(), a, &a);
    sleep(10);
    fprintf(stderr, "\nProcess %d. Value of a is %lf and address of a is %p\n",getpid(), a, &a);
    return 0;
```



# Consider the following code ...

- Consider the case when we run 4 instances of the given program at the same time on modern machines, which pair of statements is correct?
  - ① The printed "address of a" is the same for every#include <sys/syscall.h> running instances
  - ② The printed "address of a" is different for each instance
  - ③ All running instances will print the same value of a
  - Some instances will print the same value of a
  - ⑤ Each instance will print a different value of a
  - A. (1) & (3)
  - B. (1) & (4)
  - C. (1) & (5)
  - D. (2) & (3)
  - E. (2) & (4)

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#include <time.h>
double a;
int main(int argc, char *argv[])
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    number_of_total_processes = atoi(argv[1]);
    for(i = 0; i< number_of_total_processes-1 && fork(); i++);</pre>
    srand((int)time(NULL)+(int)getpid());
    fprintf(stderr, "\nProcess %d. Value of a is %lf and address
of a is %p\n",getpid(), a, &a);
    sleep(10);
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```

#### Consider the following code ...

- Consider the case when we run 4 instances of the given program at the same time on modern machines, which pair of statements is correct?
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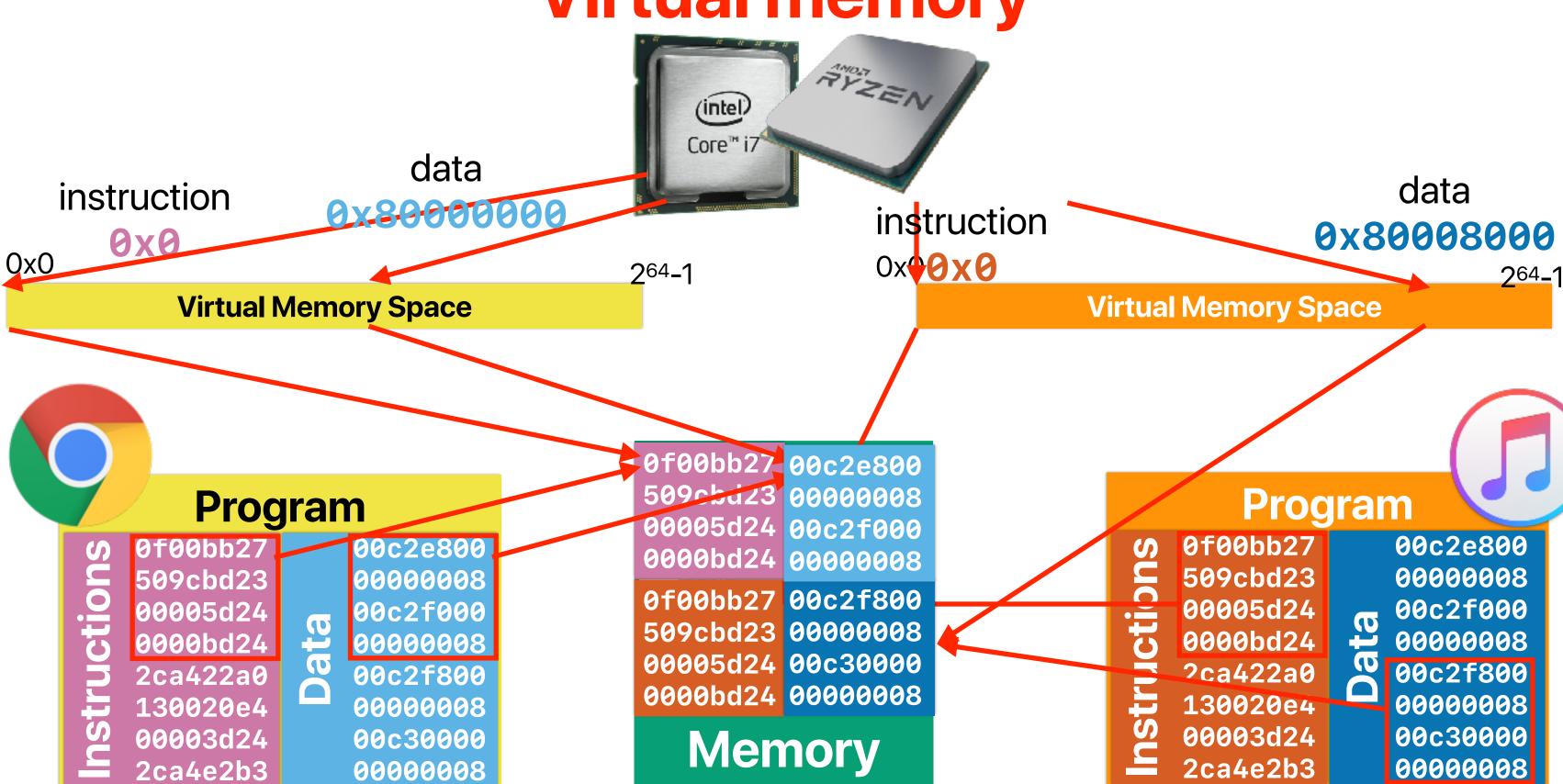
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#### **Outline**

- Virtual memory
- Architectural support for virtual memory

# Virtual Memory

# Virtual memory



#### Virtual memory

- An abstraction of memory space available for programs/ software/programmer
- Programs execute using virtual memory address
- The operating system and hardware work together to handle the mapping between virtual memory addresses and real/ physical memory addresses
- Virtual memory organizes memory locations into "pages"

Processor Core

Registers

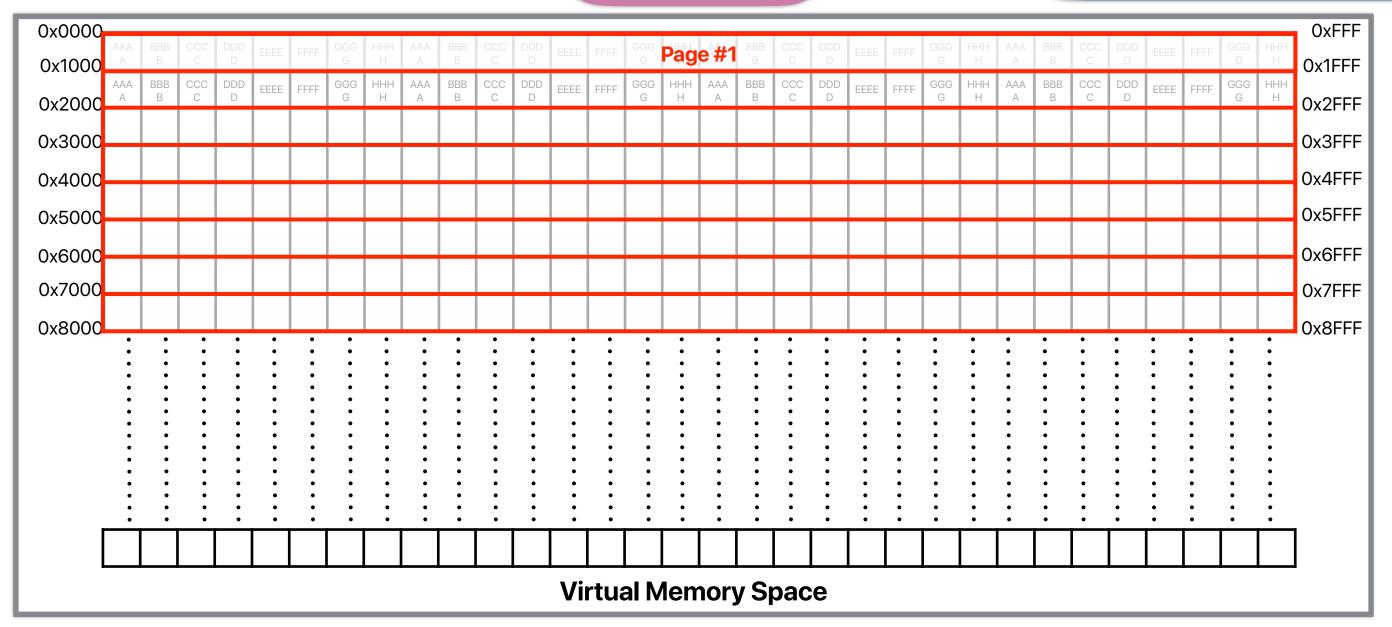
The virtual memory abstraction

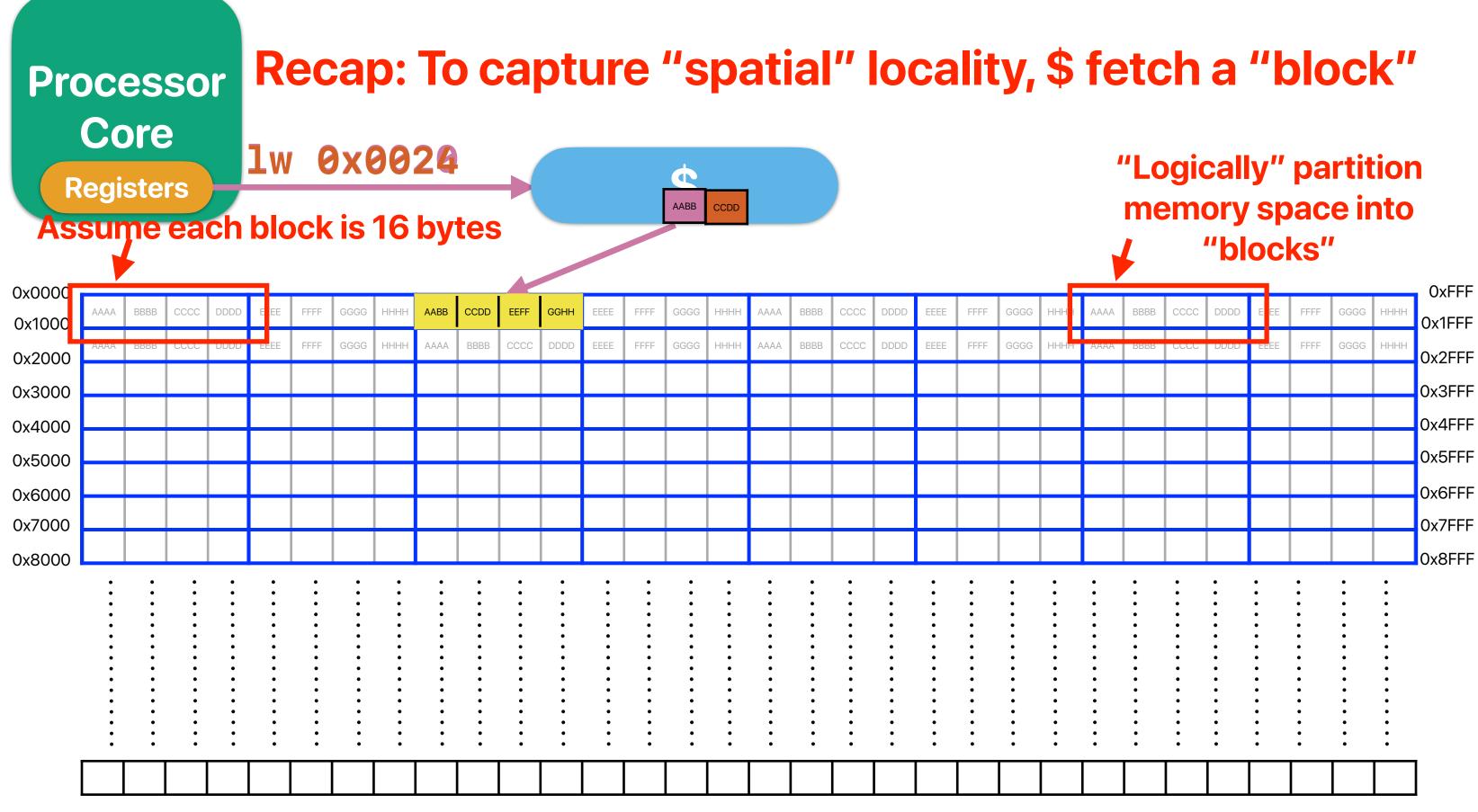
load 0x0009

Page table

MaiPage#hory

(DRAM)

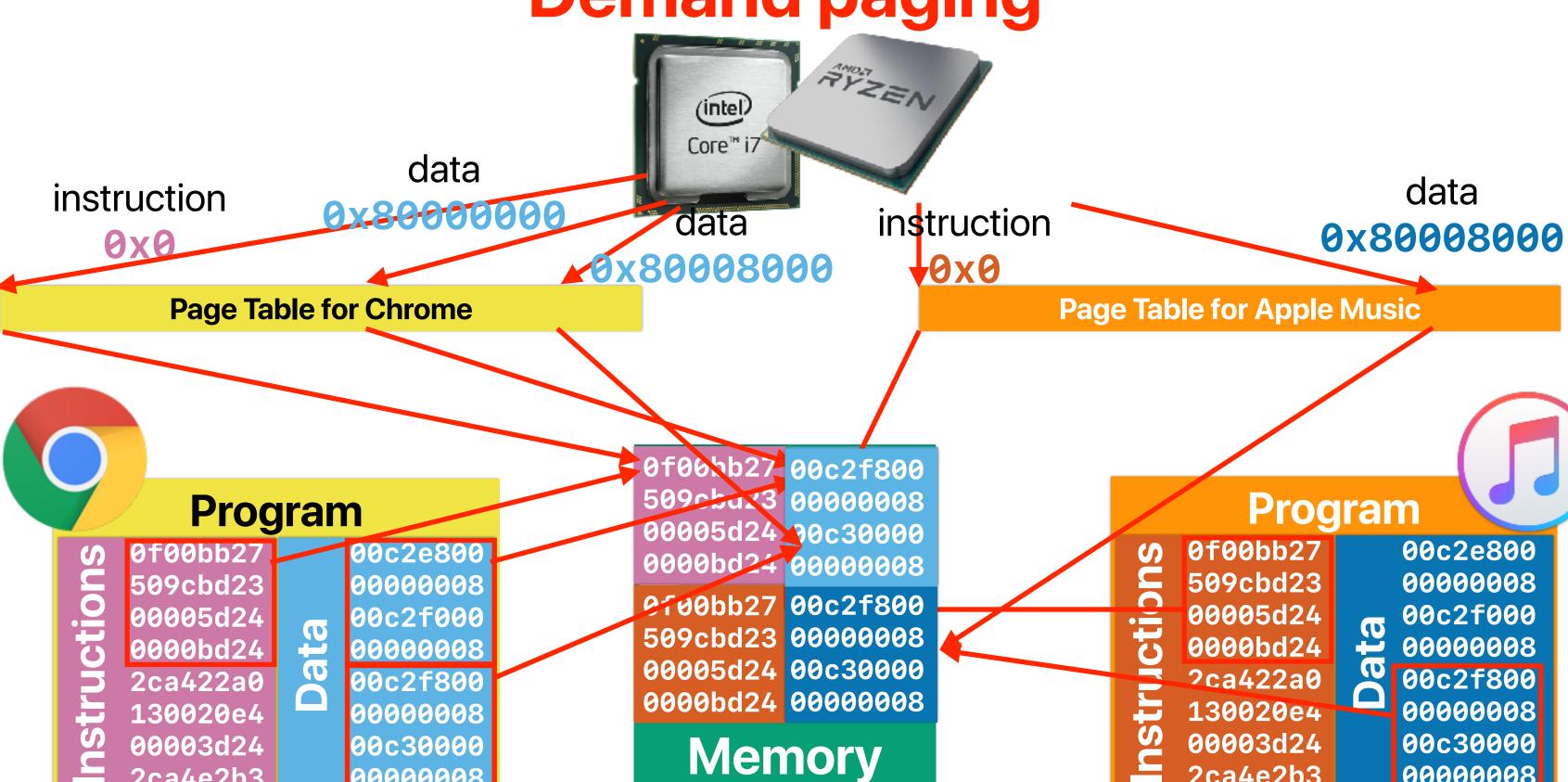




#### Why Virtual memory?

- Allowing multiple applications to share physical main memory
  - Memory protection/isolation among programs/processes is automatically achieved
- Allowing applications to work even the installed physical memory or available physical memory is smaller than the working set of the application
  - Programmer does not need to worry about the physical memory capacity of different machines — make compiled program compatible
  - Multiple programs can work concurrently even through their total memory demand is larger than the installed physical memory

# Demand paging



2ca4e2b3

00000008

00000008

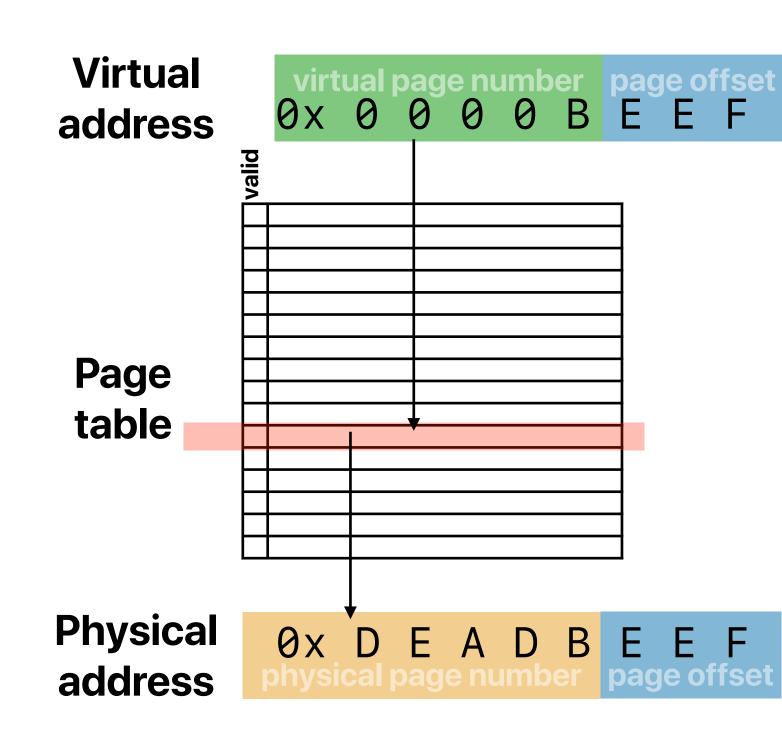
2ca4e2b3

#### **Demand paging**

- Treating physical main memory as a "cache" of virtual memory
- The block size is the "page size"
- The page table is the "tag array"
- It's a "fully-associate" cache a virtual page can go anywhere in the physical main memory

#### **Address translation**

- Processor receives virtual addresses from the running code, main memory uses physical memory addresses
- Virtual address space is organized into "pages"
- The system references the page table to translate addresses
  - Each process has its own page table
  - The page table content is maintained by OS





#### Size of page table

- Assume that we have 64-bit virtual address space, each page is 4KB, each page table entry is 8 Bytes, what magnitude in size is the page table for a process?
  - A. MB 2<sup>20</sup> Bytes
  - B. GB 2<sup>30</sup> Bytes
  - C. TB 2<sup>40</sup> Bytes
  - D. PB 2<sup>50</sup> Bytes
  - E. EB 2<sup>60</sup> Bytes



# Size of page table

 Assume that we have 64-bit virtual address space, each page is 4KB, each page table entry is 8 Bytes, what magnitude in size is the page table for a process?

$$\frac{2^{64} \ Bytes}{4 \ KB} \times 8 \ Bytes = 2^{55} \ Bytes = 32 \ PB$$

If you still don't know why — you need to take CS202

#### Conventional page table

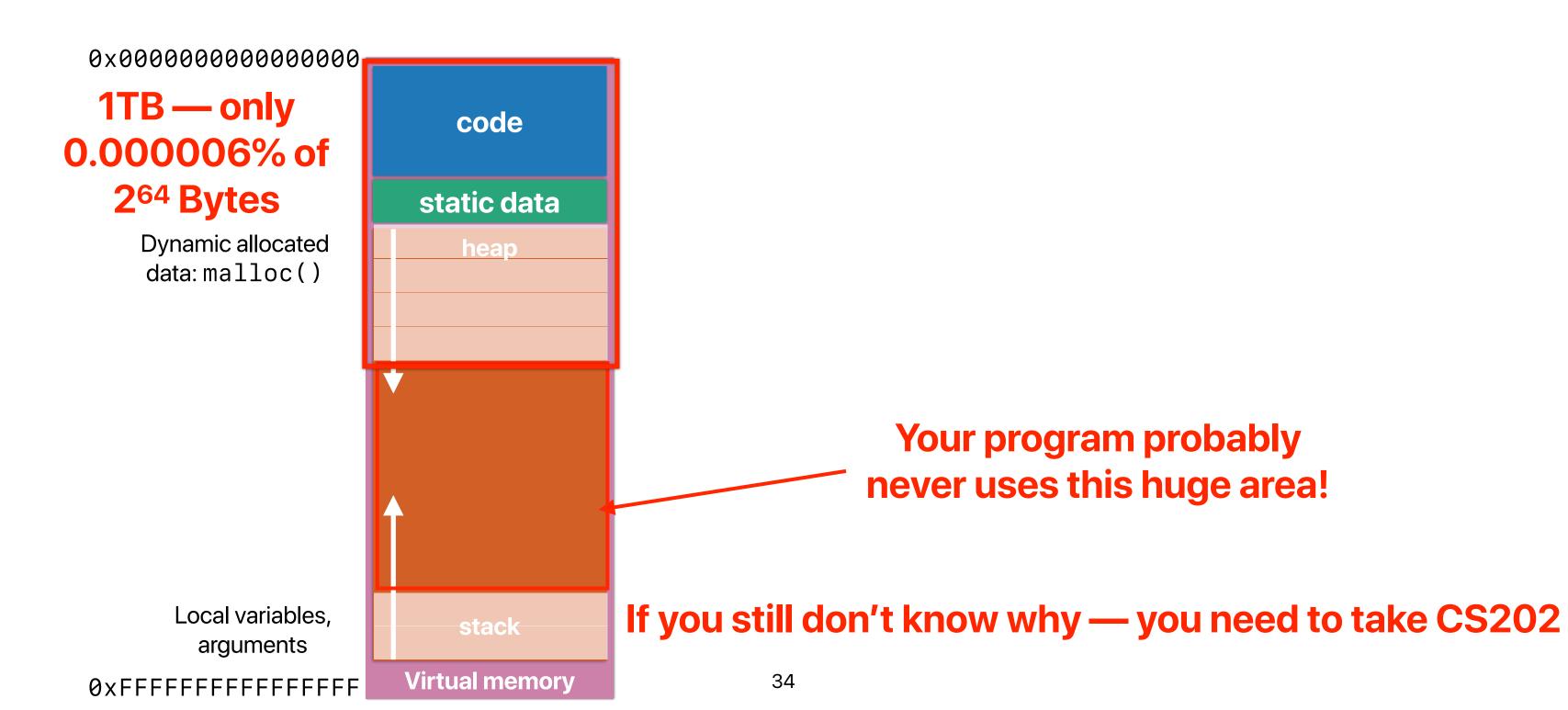
0xfffffffffffffff

#### **Virtual Address Space**

- must be consecutive in the physical memory
- need a big segment! difficult to find a spot
- simply too big to fit in memory if address space is large!

$$\frac{2^{64} B}{2^{12} B}$$
 page table entries/leaf nodes -

### Do we really need a large table?



# "Paged" page table

0xfffffffffffffff

Code Data Heap Virtual Address Space Stack

Break up entries into pages!

Each of these occupies exactly a page

$$-\frac{2^{12} B}{2^{3} P} = 2^{9}$$
 PTEs per node

0x0

**Question:** 

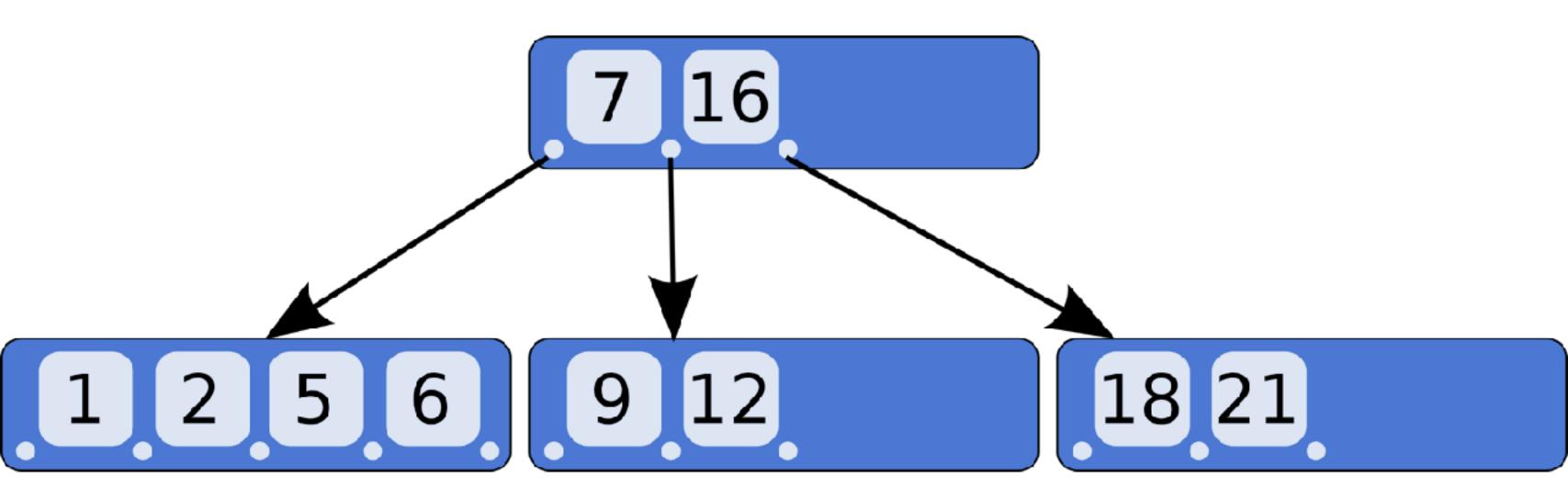
These nodes are spread out, how to locate them in the memory?

Otherwise, you always need to find more than one consecutive pages — difficult!

These are nodes are not presented if they are not referenced at all — save space

Allocate page table entry nodes "on demand"

#### **B-tree**

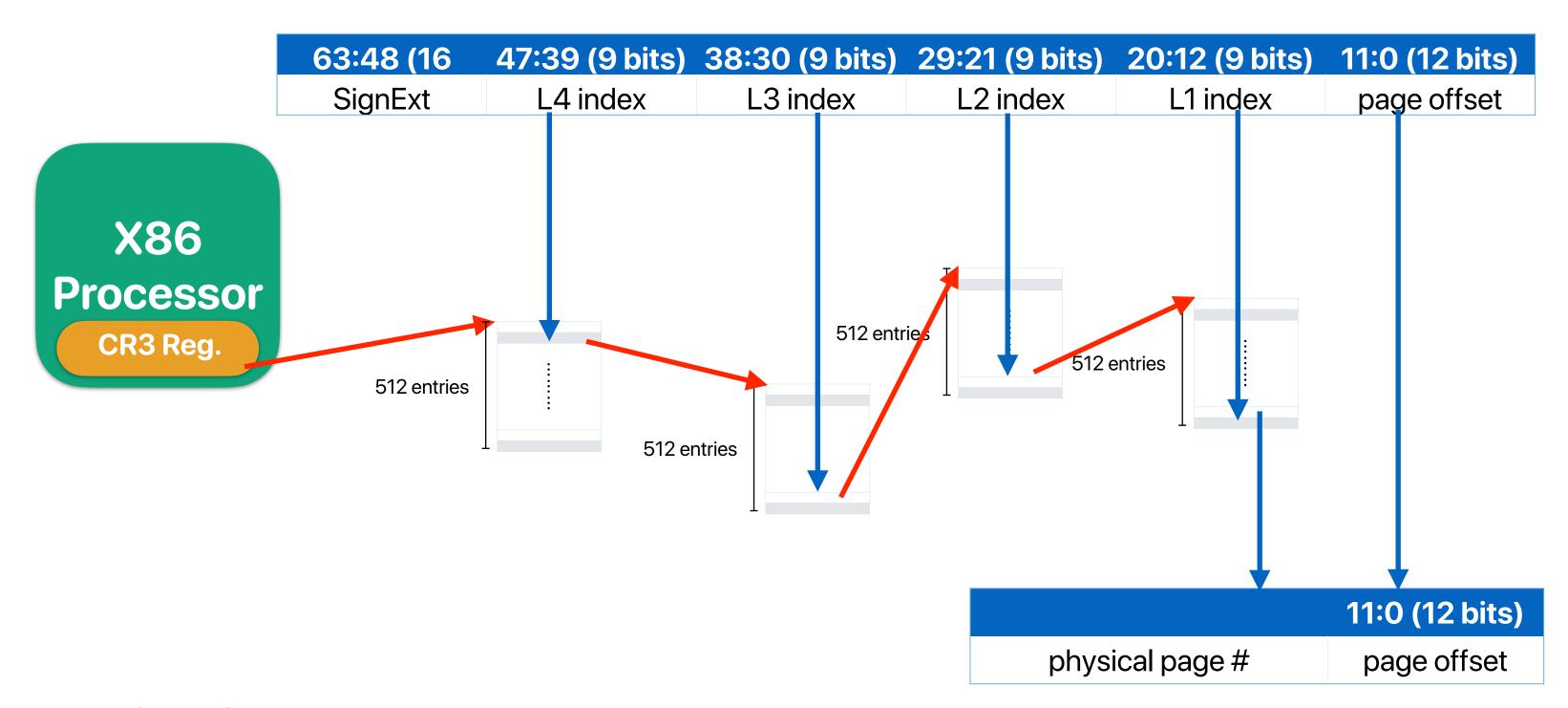


https://en.wikipedia.org/wiki/B-tree#/media/File:B-tree.svg

# **Hierarchical Page Table**

0x0 0xffffffffffffff Code Data Heap **Virtual Address Space** Stack  $\lceil log_{2^9} \frac{2^{64} B}{2^{12} B} \rceil = \lceil log_{2^9} 2^{52} \rceil = 6 \text{ levels}$ These are nodes are not presented as they are not referenced at all.  $\frac{2}{2^{12}}$  page table entries/leaf nodes (worst case)

#### Address translation in x86-64



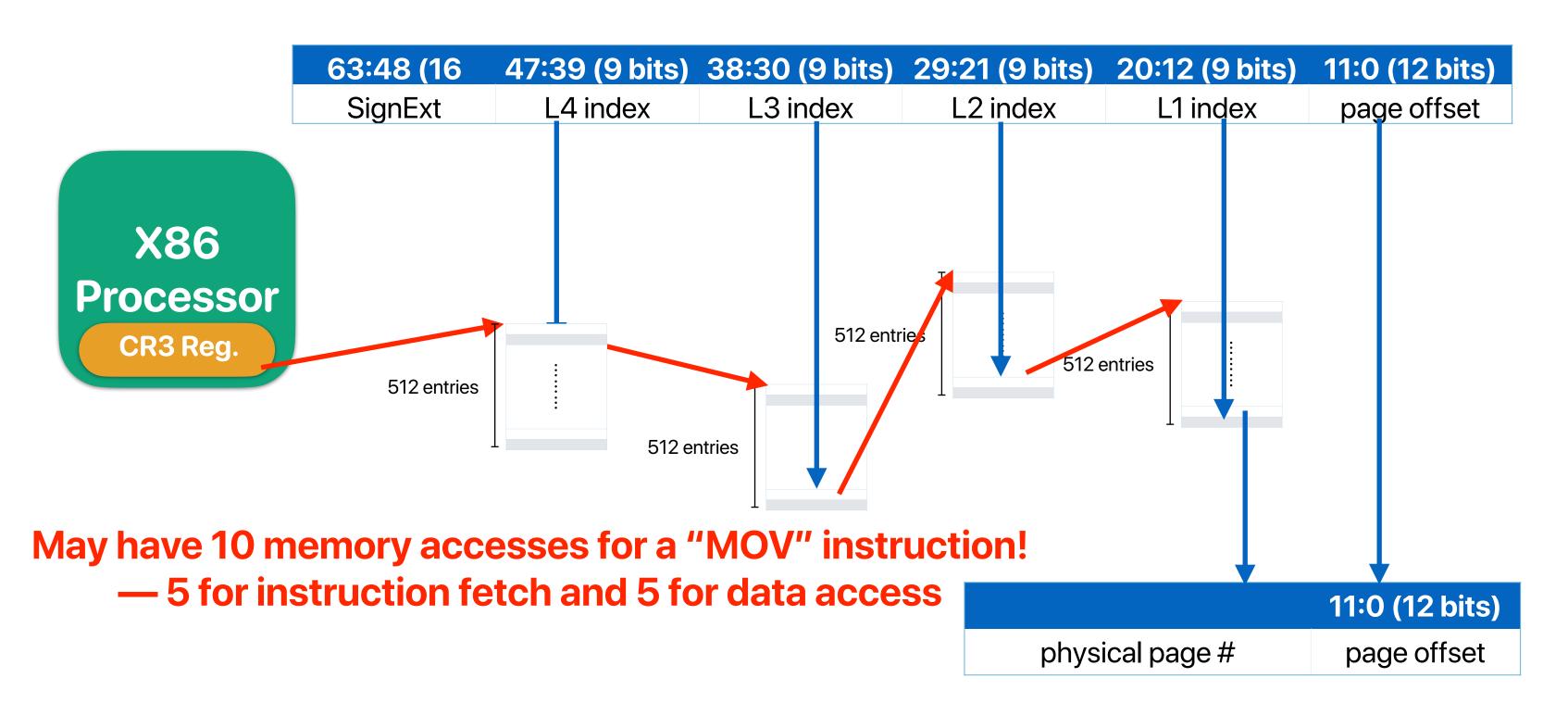


#### When we have virtual memory...

- If an x86 processor supports virtual memory through the basic format of the page table as shown in the previous slide, how many memory accesses can a mov instruction that access data memory once incur?
  - A. 2
  - B. 4
  - C. 6
  - D. 8
  - E. 10



#### Address translation in x86-64



#### When we have virtual memory...

 If an x86 processor supports virtual memory through the basic format of the page table as shown in the previous slide, how many memory accesses can a mov instruction that access data memory once incur?

A. 2

B. 4

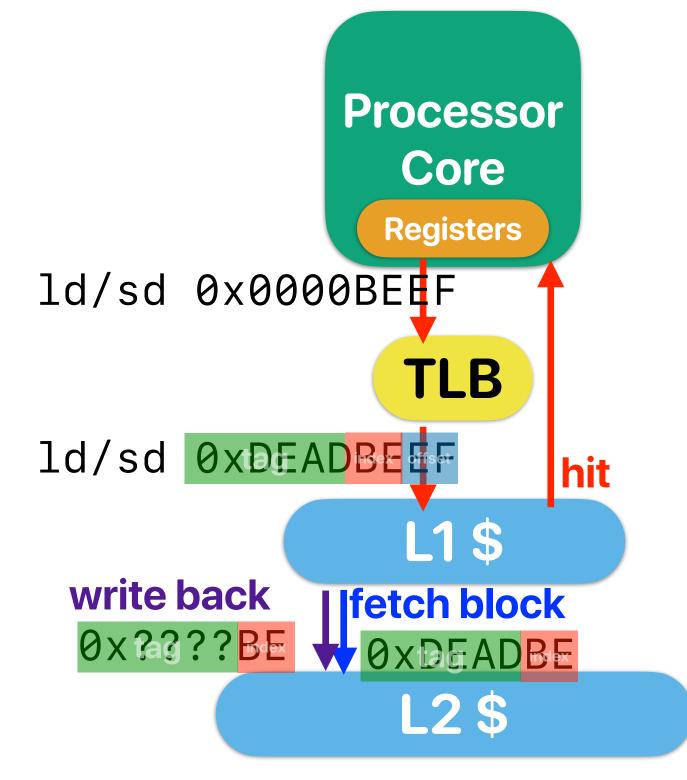
C. 6

D. 8

E. 10

# Avoiding the address translation overhead

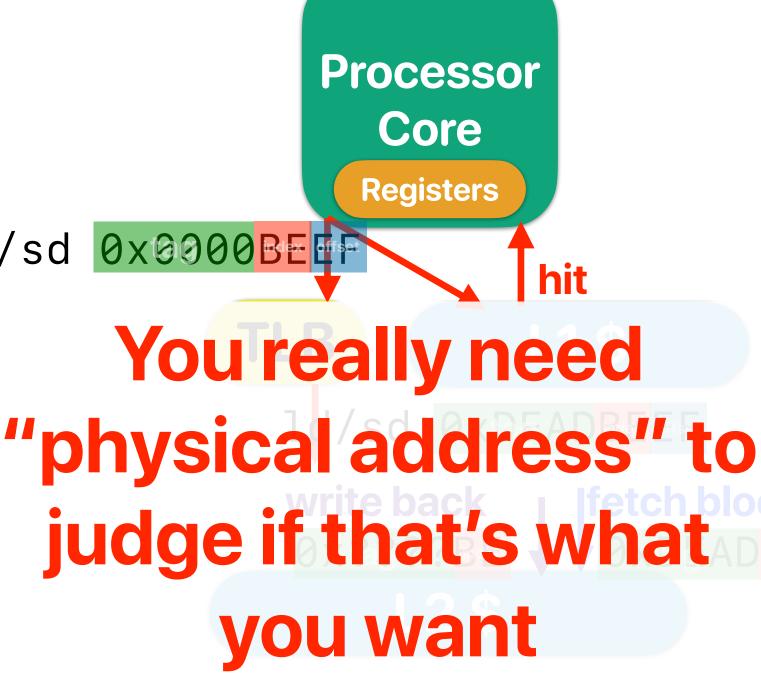
#### **TLB: Translation Look-aside Buffer**



- TLB a small SRAM stores frequently used page table entries
- Good A lot faster than having everything going to the DRAM
- Bad Still on the critical path

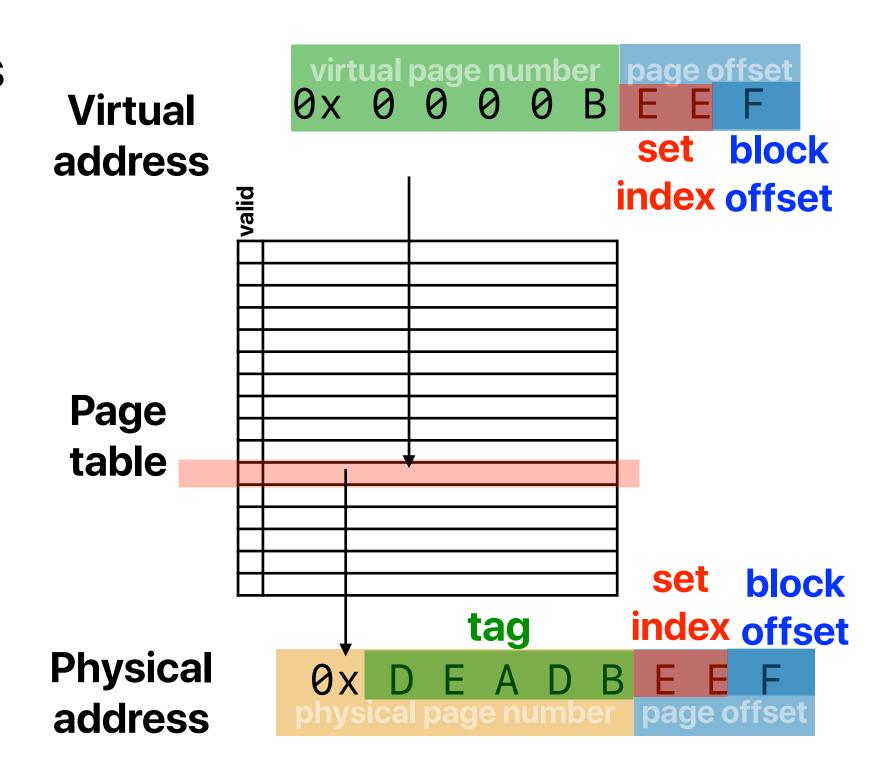
#### TLB + Virtual cache

- L1 \$ accepts virtual address you don't need to translate
- Good you can access both TLB and L1-\$ at the same time and physical address is only needed if L1-\$ missed d/sd
- Bad it doesn't work in practice
  - Many applications have the same virtual address but should be pointing different physical addresses
  - An application can have "aliasing virtual addresses" pointing to the same physical address

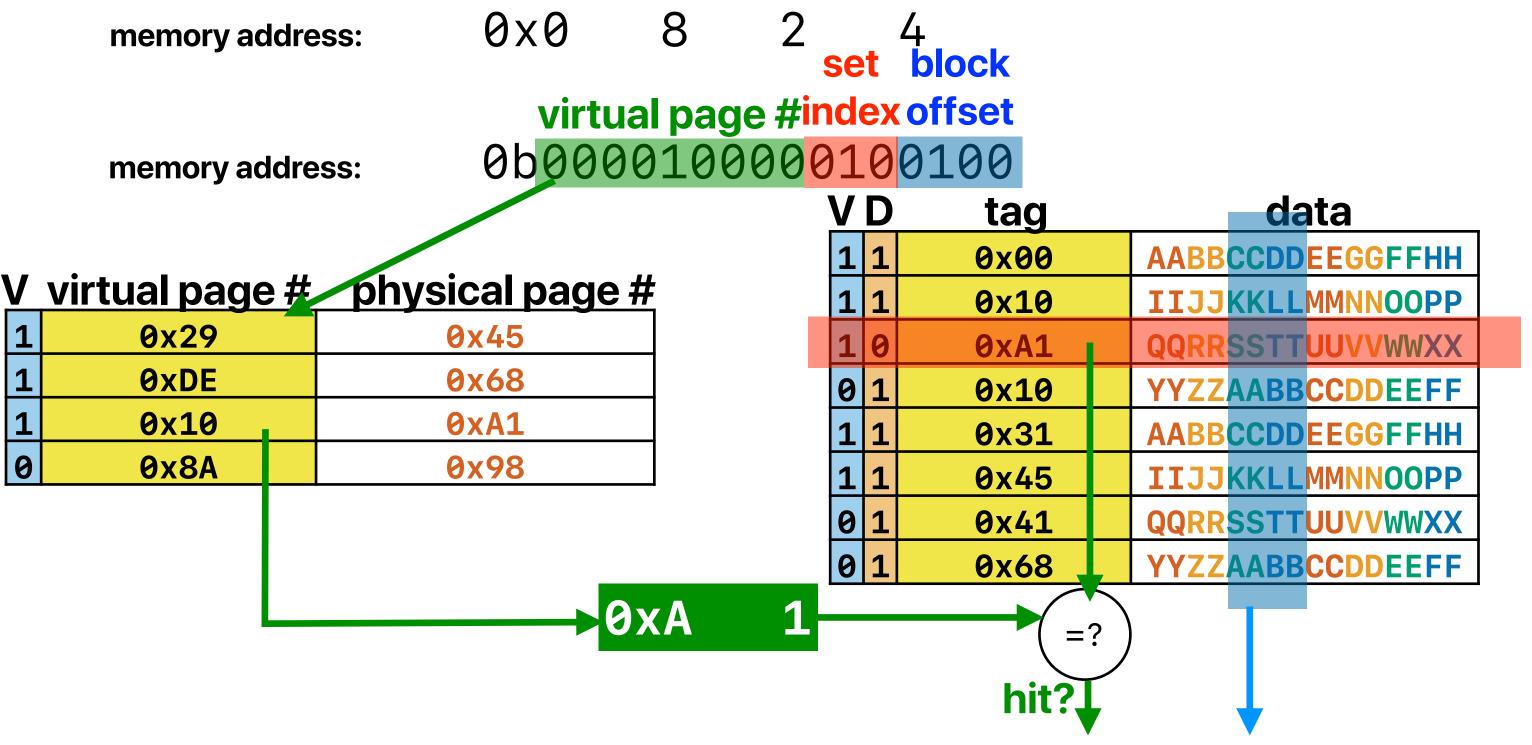


# Virtually indexed, physically tagged cache

- Can we find physical address directly in the virtual address
  - Not everything but the page offset isn't changing!
- Can we indexing the cache using the "partial physical address"?
  - Yes Just make set index + block set to be exactly the page offset



# Virtually indexed, physically tagged cache



# Virtually indexed, physically tagged cache

If page size is 4KB —

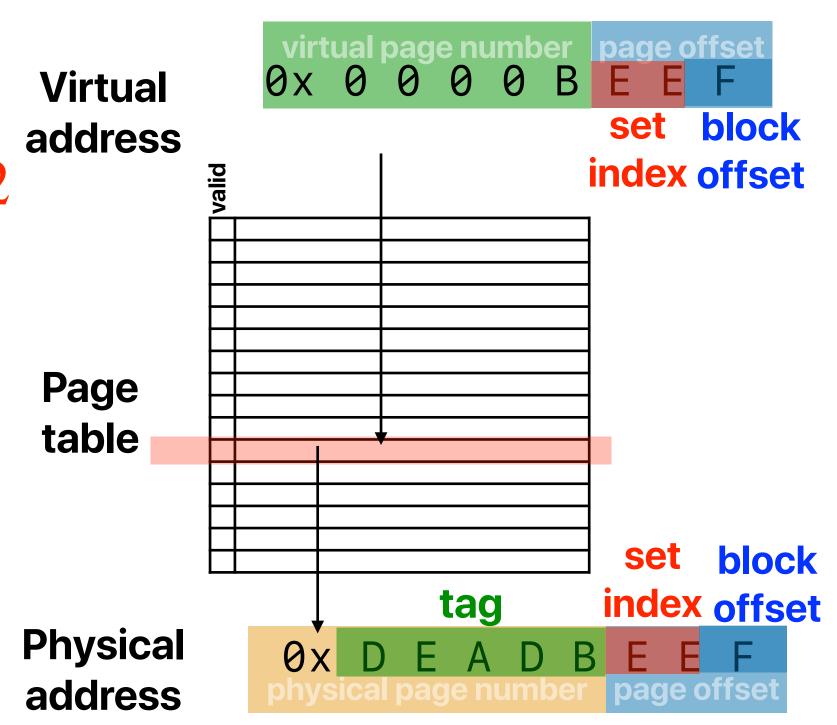
$$lg(B) + lg(S) = lg(4096) = 12$$

$$C = ABS$$

$$C = A \times 2^{12}$$

$$if A = 1$$

$$C = 4KB$$





#### Virtual indexed, physical tagged cache limits the cache size

- If you want to build a virtual indexed, physical tagged cache with 32KB capacity, which of the following configuration is possible? Assume the operating system use 4K pages.
  - A. 32B blocks, 2-way
  - B. 32B blocks, 4-way
  - C. 64B blocks, 4-way
  - D. 64B blocks, 8-way



#### Virtual indexed, physical tagged cache limits the cache size

 If you want to build a virtual indexed, physical tagged cache with 32KB capacity, which of the following configuration is possible? Assume the operating system use 4K pages.

Exactly how Core i7 9th generation configures its own cache

$$lg(B) + lg(S) = lg(4096) = 12$$

$$C = ABS$$

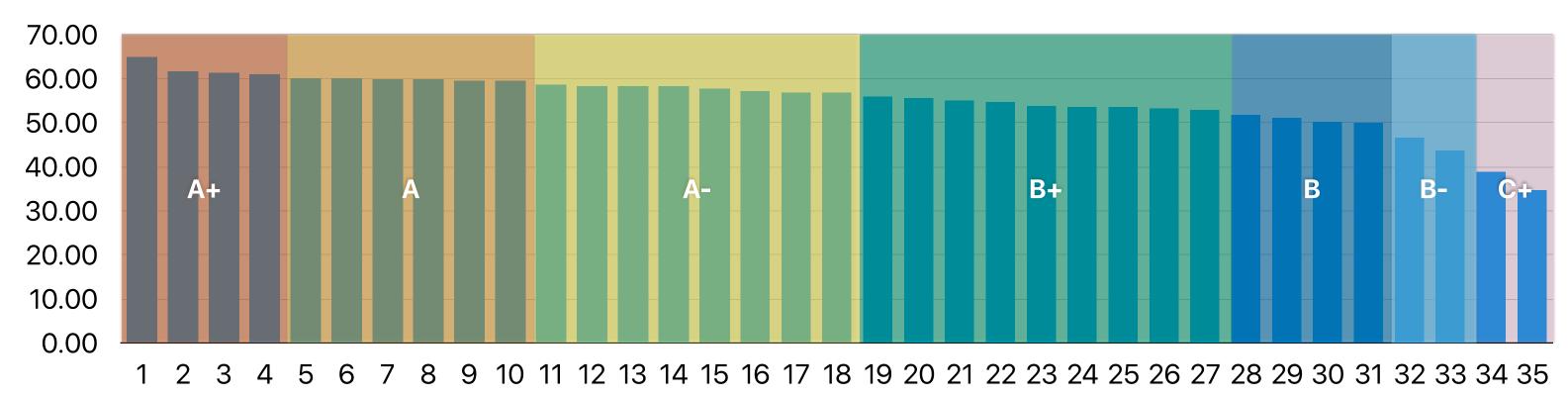
$$32KB = A \times 2^{12}$$

$$A = 8$$

#### **Announcements**

- Reading quiz due tomorrow
- Assignment 3 released
- Your overall grade and your ranking in the class decides your final letter grade, not just the midterm.
  - The bar chart below shows the current "total" and the "projected" letter grades
  - The curve is flexible we don't mind to give more As, but depending on how good is the class overall
  - Midterm is only 25% max 100, mean 74.
  - Final exam is 35%

#### **Current "Total" and "Projected" Letter Grades**



# Computer Science & Engineering

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