# 2022 Digital IC Design Homework 3

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|---|---|
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**Simulation Result**

| Functional simulation | Pass/ Fail (encoder) | Pass/ Fail (decoder) | Gate-level simulation | Pass/ Fail (encoder) | Pass/ Fail (decoder) |
|---|---|---|---|---|---|

(your pre-sim result) encoder/decoder img0

```
# cycle 03a12, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 03a26, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 03a3a, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 03a4e, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 03a62, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 03a7d, expect(7,6,$) , get(7,6,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Encoder.sv(250)
#    Time: 449400 ns  Iteration: 1  Instance: /testfixture_encoder
# cycle 007ff, expect 0, get 0 >> Pass
# cycle 00800, expect 8, get 8 >> Pass
# cycle 00801, expect 0, get 0 >> Pass
# cycle 00802, expect 8, get 8 >> Pass
# cycle 00803, expect 0, get 0 >> Pass
# cycle 00804, expect 8, get 8 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Decoder.sv(228)
#    Time: 61590 ns  Iteration: 1  Instance: /testfixture_decoder
```

(your post-sim result) encoder/decoder img0

```
# cycle 03a26, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 03a3a, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 03a4e, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 03a62, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 03a7d, expect(7,6,$) , get(7,6,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Encoder.sv(250)
#    Time: 449400 ns  Iteration: 1  Instance: /testfixture_encoder

#   == Decoding string "080808"
# cycle 007ff, expect 0, get 0 >> Pass
# cycle 00800, expect 8, get 8 >> Pass
# cycle 00801, expect 0, get 0 >> Pass
# cycle 00802, expect 8, get 8 >> Pass
# cycle 00803, expect 0, get 0 >> Pass
# cycle 00804, expect 8, get 8 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Decoder.sv(228)
#    Time: 61590 ns  Iteration: 1  Instance: /testfixture_decoder
```

(your pre-sim result) encoder/decoder img1

```
# cycle 03d63, expect(5,1,4) , get(5,1,4) >> Pass
# cycle 03d73, expect(5,1,8) , get(5,1,8) >> Pass
# cycle 03d83, expect(3,2,f) , get(3,2,f) >> Pass
# cycle 03d89, expect(0,0,6) , get(0,0,6) >> Pass
# cycle 03d8d, expect(0,0,$) , get(0,0,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Encoder.sv(250)
#    Time: 472740 ns  Iteration: 1  Instance: /testfixture_encoder


#   == Decoding string "f4f"
# cycle 00801, expect f, get f >> Pass
# cycle 00802, expect 4, get 4 >> Pass
# cycle 00803, expect f, get f >> Pass
#   == Decoding string "6"
# cycle 00804, expect 6, get 6 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Decoder.sv(228)
#    Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder
```

(your post-sim result) encoder/decoder img1

```
# cycle 03d63, expect(5,1,4) , get(5,1,4) >> Pass
# cycle 03d73, expect(5,1,8) , get(5,1,8) >> Pass
# cycle 03d83, expect(3,2,f) , get(3,2,f) >> Pass
# cycle 03d89, expect(0,0,6) , get(0,0,6) >> Pass
# cycle 03d8d, expect(0,0,$) , get(0,0,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Encoder.sv(250)
#    Time: 472740 ns  Iteration: 1  Instance: /testfixture_encoder

# cycle 00803, expect f, get f >> Pass
#   == Decoding string "6"
# cycle 00804, expect 6, get 6 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Decoder.sv(228)
#    Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder
```

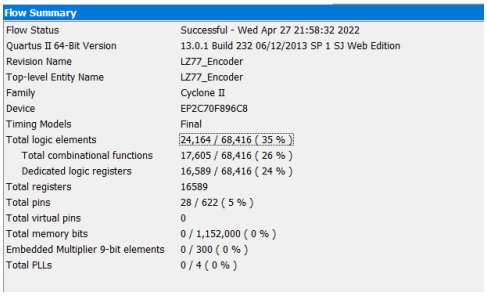
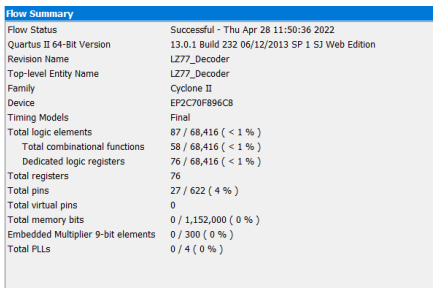
(your pre-sim result) encoder/decoder img2

```
# cycle 025c4, expect(7,7,7) , get(7,7,7) >> Pass
# cycle 025dd, expect(1,3,6) , get(1,3,6) >> Pass
# cycle 025f7, expect(5,5,7) , get(5,5,7) >> Pass
# cycle 0260c, expect(5,7,6) , get(5,7,6) >> Pass
# cycle 02620, expect(7,7,7) , get(7,7,7) >> Pass
# cycle 0263b, expect(7,6,4) , get(7,6,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Encoder.sv(250)
#    Time: 293820 ns  Iteration: 1  Instance: /testfixture_encoder


#   == Decoding string "d7d7d7"
# cycle 007ff, expect d, get d >> Pass
# cycle 00800, expect 7, get 7 >> Pass
# cycle 00801, expect d, get d >> Pass
# cycle 00802, expect 7, get 7 >> Pass
# cycle 00803, expect d, get d >> Pass
# cycle 00804, expect 7, get 7 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Decoder.sv(228)
#    Time: 61590 ns  Iteration: 1  Instance: /testfixture_decoder
```

(your post-sim result) encoder/decoder img2

```
# cycle 025f7, expect(5,5,7) , get(5,5,7) >> Pass
# cycle 0260c, expect(5,7,6) , get(5,7,6) >> Pass
# cycle 02620, expect(7,7,7) , get(7,7,7) >> Pass
# cycle 0263b, expect(7,6,$) , get(7,6,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Encoder.sv(250)
#    Time: 293820 ns  Iteration: 1  Instance: /testfixture_encoder

#   == Decoding string "d7d7d7"
# cycle 007ff, expect d, get d >> Pass
# cycle 00800, expect 7, get 7 >> Pass
# cycle 00801, expect d, get d >> Pass
# cycle 00802, expect 7, get 7 >> Pass
# cycle 00803, expect d, get d >> Pass
# cycle 00804, expect 7, get 7 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW3/tb_Decoder.sv(228)
#    Time: 61590 ns  Iteration: 1  Instance: /testfixture_decoder
```

| Synthesis Result | encoder | decoder |
|---|---|---|
| Total logic elements | 24164 | 87 |

| | | |
|---|---|---|
| Total memory bit | 0 | 0 |
| Embedded multiplier 9-bit element | 0 | 0 |
| Simulation time img0 | 449400 (ns) | 61590 (ns) |
| Simulation time img1 | 472740 (ns) | 61620 (ns) |
| Simulation time img2 | 293820 (ns) | 61590 (ns) |
| (your flow summary) encoder<br>  | (your flow summary) decoder<br>  | |

| Flow Summary | |
|---|---|
| Flow Status | Successful - Wed Apr 27 21:58:32 2022 |
| Quartus II 64-Bit Version | 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition |
| Revision Name | LZ77_Encoder |
| Top-level Entity Name | LZ77_Encoder |
| Family | Cyclone II |
| Device | EP2C70F896C8 |
| Timing Models | Final |
| Total logic elements | 24,164 / 68,416 ( 35 % ) |
| Total combinational functions | 17,605 / 68,416 ( 26 % ) |
| Dedicated logic registers | 16,589 / 68,416 ( 24 % ) |
| Total registers | 16589 |
| Total pins | 28 / 622 ( 5 % ) |
| Total virtual pins | 0 |
| Total memory bits | 0 / 1,152,000 ( 0 % ) |
| Embedded Multiplier 9-bit elements | 0 / 300 ( 0 % ) |
| Total PLLs | 0 / 4 ( 0 % ) |

| Flow Summary | |
|---|---|
| Flow Status | Successful - Thu Apr 28 11:50:36 2022 |
| Quartus II 64-Bit Version | 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition |
| Revision Name | LZ77_Decoder |
| Top-level Entity Name | LZ77_Decoder |
| Family | Cyclone II |
| Device | EP2C70F896C8 |
| Timing Models | Final |
| Total logic elements | 87 / 68,416 ( < 1 % ) |
| Total combinational functions | 58 / 68,416 ( < 1 % ) |
| Dedicated logic registers | 76 / 68,416 ( < 1 % ) |
| Total registers | 76 |
| Total pins | 27 / 622 ( 4 % ) |
| Total virtual pins | 0 |
| Total memory bits | 0 / 1,152,000 ( 0 % ) |
| Embedded Multiplier 9-bit elements | 0 / 300 ( 0 % ) |
| Total PLLs | 0 / 4 ( 0 % ) |

**Description of your design**

Encoder 的部分會先將 2049 個 input 存在一個 str_buf 中，並像文件上的一樣，使用 search buffer 和 lookahead buffer 來進行 encoder。分成兩種情況，一種是在 search buffer 內就已經完成 encoder，另一種是會從 search buffer 跨到 lookahead buffer，此兩種情況都利用如同 C code 的雙重迴圈從 search buffer[8]~[0]來一一比對是否與 lookahead buffer[7]的字元相同，不是的話就減 1 往前，當比對完成後，會將 search、lookahead buffer 根據 matchlen 來從 str_buf 內抓取出接下來要 encode 的字元。

Decoder 的部分會將各個解碼步驟一一寫入 search buffer 中，並將 search buffer[0]的位置 assign 為 char_nxt，接著平移 buffer，如此一來就可以把解碼的字元一個個輸出。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element)*