2022 Digital IC Design
Homework 4: Edge-Based Line Average interpolation

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Clock width	18 (ns)	Gate-level simulation time	52226(ns)

your pre-sim result of test patterns

```
# ----------------------------------------------------------------
#
#    START!!! Simulation Start .....
#
# ----------------------------------------------------------------
#
#
#
# ------------------------S U M M A R Y----------------------------
#
#    Congratulations!
#
#    Result image data are generated successfully!
#
#    The result is PASS!!!
#
# ----------------------------------------------------------------
#
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW4/file/testfixture.v(176)
#    Time: 52218 ns  Iteration: 0  Instance: /TB_ELA
```

your post-sim result of test patterns

```
# ----------------------------------------------------------------
#
#    START!!! Simulation Start .....
#
# ----------------------------------------------------------------
#
#
#
# ------------------------S U M M A R Y----------------------------
#
#    Congratulations!
#
#    Result image data are generated successfully!
#
#    The result is PASS!!!
#
# ----------------------------------------------------------------
#
# ** Note: $finish    : C:/Users/User/Desktop/IC HW/HW4/file/testfixture.v(176)
#    Time: 52226601 ps  Iteration: 0  Instance: /TB_ELA
```

Synthesis Result

Total logic elements	350
Total memory bit	0
Embedded multiplier 9-bit element	0

your flow summary

Flow Summary

Flow Status	Successful - Wed May 25 15:03:59 2022
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	ELA
Top-level Entity Name	ELA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	350 / 68,416 (< 1 %)
Total combinational functions	348 / 68,416 (< 1 %)
Dedicated logic registers	101 / 68,416 (< 1 %)
Total registers	101
Total pins	39 / 622 (6 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

先從測資將 Odd part 讀入並直接寫入 Result Image Memory，再來從最左邊一次從 Odd part 讀上下共 6 個值存入暫存器來計算 Even part(邊緣讀兩個就直接算)，每移動一個單位，這六個暫存器就會向左平移，所以讀好六個值後，之後每次要讀兩個做平移，再利用 3 個 assign 來計算三個 min 值，再從那六個暫存器找最小位置的兩個出來除 2。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*