Deerwalk Institute of Technology

Subject: CSC-151: Digital Logic

Level: Freshman Year / Second Semester

Nature of course: Theory (3 Hrs) + Lab (3 Hrs)

Full Marks: 60 (Board) + 20 (Internal) + 20 (Practical)

Pass Marks: 24 (Board) + 8 (Internal) + 8 (Practical)

Name of Instructor (Theory): Sanjeeb Prasad Panday (Ph.D.)

Evaluation Criteria: Internal

Total Marks: - 20

Class Test: 8

Assignments: 2

Attendance: 8

Presentation: 2

Course Synopsis: General concepts to be used in the design and analysis of digital systems and introduces the principles of digital computer organization and design.

Goals:
• Introduce fundamental digital logics and switching networks. Exposure of Boolean algebra and its application for circuit analysis.
• Introduction to multilevel gates networks, flip-lops, counters and logic devices.

Course Contents:

Unit 1: Binary Systems (7 Hrs → Week 1, 2 and 3)
Digital Systems, Binary numbers, Number base conversion, Octal and hexadecimal numbers, Binary Systems, Integrated Circuits

Unit 2: Boolean algebra and Logic Gates (6 Hrs → Week 3, 4 and 5)
Basic definitions of Boolean algebra, basic Theory of Boolean Algebra, Boolean Function, Logic Operations, Logic Gates, IC Digital Logic Families

Unit 3: Simplification of Boolean Functions (6 Hrs → Week 5, 6 and 7)
K-map, Two and Three variable maps, Four variable maps, product of sums, sum of

product simplification, NAND and NOR implementation

Unit 4: Combinational Logic (6 Hrs → Week 7, 8 and 9)
Design Procedure, Adders, Subtractors, Code Conversions, Analysis Procedure, NAND Circuits, NOR Circuits, Exclusive –OR Circuits

(1st Class Test → Week 9) Time 1 Hour

Unit 5: Combinational Logic with MSI and LSI (6 Hrs → Week 10, 11 and 12)
Binary Parallel Adder, Decimal Adder, Magnitude Comparator, Decoders, Multiplexers, Read-only-Memory (ROM), Programmable Logic Array (PLA)

Unit 6: Sequential Logic (8 Hrs → Week 12, 13 and 14)
Flip-Flops, Triggering of flip-flops, Design procedure, Design with state equations and state reduction table

(2nd Class Test → Week 15) Time 1 Hour

Unit 7: Registers and Counters (6 Hrs → Week 15-16)
Registers, Shift registers, Ripple Counters, Synchronous Counters, Timing Sequences, the memory Unit

Text/ Reference book

M.Morris Mano, "Logic & Computer Design Fundamentals", Pearson Education.

Note:
The above-mentioned timetable is only the estimated one and is subject to change in case the students are not able to grasp any lecture in the allocated time.