The 80386 Microprocessors

INTRODUCTION

The 80386 microprocessor is a full 32-bit version of the earlier 8086 80286 l6-bit microprocessors, and represents a major advancement in the architecture switch from l6-bit architecture to 32-bit architecture. Along with this larger word size are many improvements and additional features.

The 80386 microprocessor features multitasking, memory management, virtual memory (with or without paging), software protection, and a large memory system. All software written for the early 8086 8088 and the 80286 are upward-compatible to the 80386 microprocessor. The amount of memory addressable by the 80386 is increased from the 1M byte found in the 8086 8088 and the 16M bytes found in the 80286, to 4G bytes in the 80386.

The 80386 can switch between protected mode and real mode without resetting the microprocessor. Switching from protected mode to real mode was a problem on the 80286 microprocessor because it required a hardware reset

The 80386DX is packaged in a 132-pin PGA (pin grid array).two versions of the 80386 are commonly available, the 386DX which is illustrated and the other is the 80386SX which is a reduced bus version of the 80386. A new version of the 80386-the 80386EX incorporates the AT bus system, dynamic RAM controller. programmable chip selection logic, 2 address pins, 16 data pins, and 24 .*IO* pins

The 80386DX addresses 4G bytes of memory through its 32-bit data bus and 32address. The 80386SX, was developed after the 80386DX for application that didn't require the full 32-bit bus version. The 80386SX was found in many early personal computers that used the same basic motherboard design as the 80286. At the time that t 80386SX was popular, most applications, including Windows 3.11, required fewer than 16 bytes of memory, so the 80386SX is a popular version of the 80386 microprocessor. Even though the 80486 has become a less expensive upgrade path for newer system the 80386 still can be used for many applications. For example. the 80386EX does not appear computer systems, but it is becoming very popular in embedded applications.

As with earlier versions of the Intel family of microprocessors, the 80386 requires a sin +5.0 V power supply for operation. The power supply current averages 550 mA for the 25 MHz version of the 80386, 500mA for the 20 MHz version. and 450 mA forth16 MHz version. Also available is a 33 MHz version that requires

600 mA of power supply current. The power sup current for the 80386EX is 320 mA when operated at 33 MHz Note that during some modes.

Pin Connection

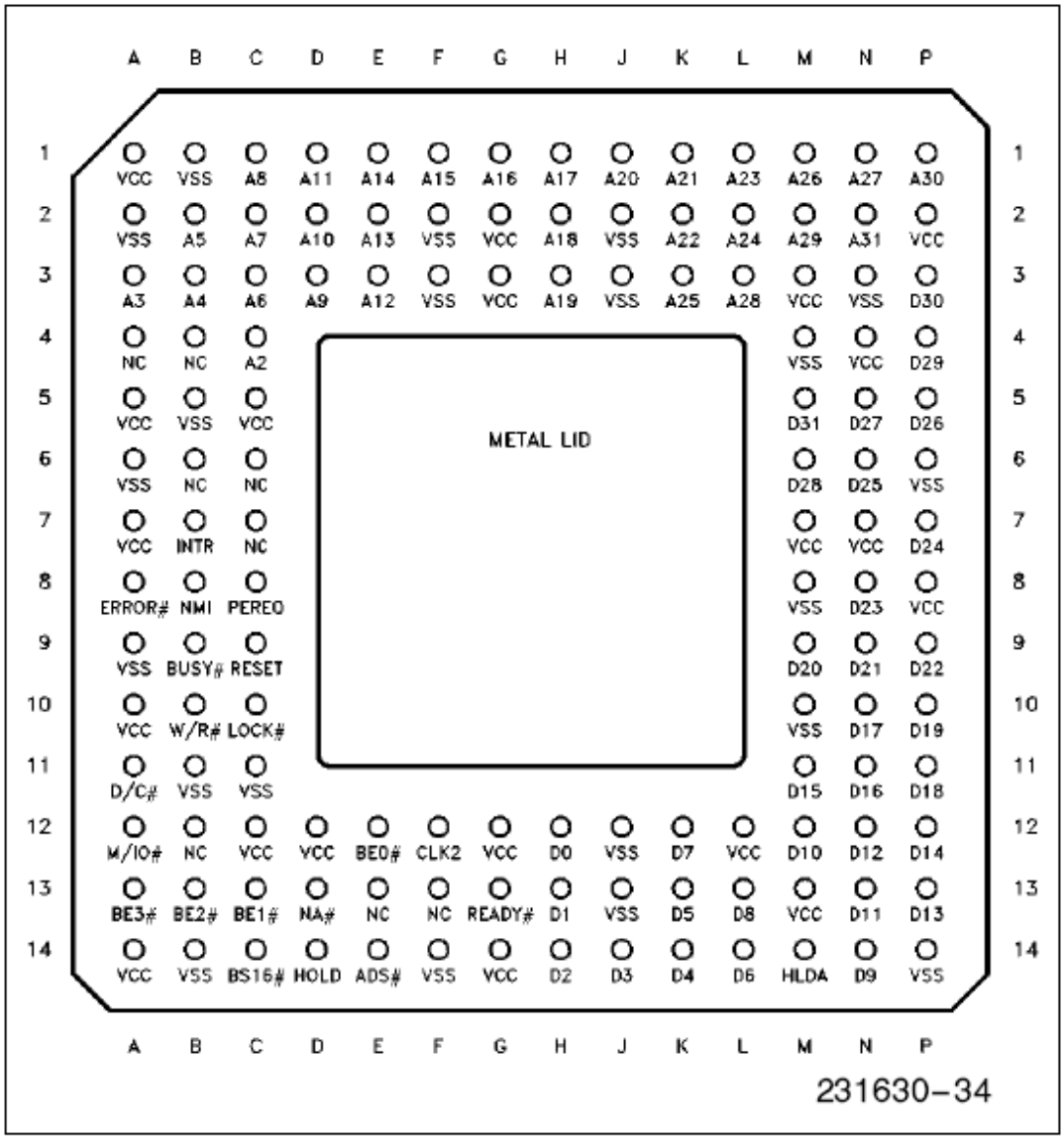


Figure 1-2. Intel386™ DX PGA Pinout—View from Pin Side

Table 1-1. Intel386™ DX PGA Pinout—Functional Grouping

Signal/Pin		Signal/Pin		Signal/Pin		Signal/Pin		Signal/Pin		Signal/Pin	
A2	C4	A24	L2	D6	L14	D28	M6	V_{CC}	C12	V_{SS}	F2
A3	A3	A25	K3	D7	K12	D29	P4		D12		F3
A4	B3	A26	M1	D8	L13	D30	P3		G2		F14
A5	B2	A27	N1	D9	N14	D31	M5		G3		J2
A6	C3	A28	L3	D10	M12	D/C#	A11		G12		J3
A7	C2	A29	M2	D11	N13	ERROR#	A8		G14		J12
A8	C1	A30	P1	D12	N12	HLDA	M14		L12		J13
A9	D3	A31	N2	D13	P13	HOLD	D14		M3		M4
A10	D2	ADS#	E14	D14	P12	INTR	B7		M7		M8
A11	D1	BE0#	E12	D15	M11	LOCK#	C10		M13		M10
A12	E3	BE1#	C13	D16	N11	M/IO#	A12		N4		N3
A13	E2	BE2#	B13	D17	N10	NA#	D13		N7		P6
A14	E1	BE3#	A13	D18	P11	NMI	B8		P2		P14
A15	F1	BS16#	C14	D19	P10	PEREQ	C8		P8	W/R#	B10
A16	G1	BUSY#	B9	D20	M9	READY#	G13	V_{SS}	A2	N.C.	A4
A17	H1	CLK2	F12	D21	N9	RESET	C9		A6		B4
A18	H2	D0	H12	D22	P9	V_{CC}	A1		A9		B6
A19	H3	D1	H13	D23	N8		A5		B1		B12
A20	J1	D2	H14	D24	P7		A7		B5		C6
A21	K1	D3	J14	D25	N6		A10		B11		C7
A22	K2	D4	K14	D26	P5		A14		B14		E13
A23	L1	D5	K13	D27	N5		C5		C11		F13

Data bus(D0-D31) Data bus connections transfer data between the microprocessor and its memory and I/O system.

Bank enable(be0,be1,be2,be3) signals select the access of a byte, word, or double word of data. These signals are generated internally by the microprocessor from address bits A1 and A0.

Memory\IO (M/IO') selects a memory device when a logic I or an I/O device when a logic O. During the I/O operation, the address bus contains a 16-bit I/O address on address connections AI5-A2'

Write/Read(W/R') indicates that the current bus cycle is a write when a logic I or a read when a logic 0.

The address data strobe (ADS') becomes active whenever the 80386 has issued a valid memory or I/O address. This signal is combined with the W/R signal to generate the separate read and write signals present in the earlier

8086-80286 microprocessor-based systems.

Reset initializes the_80386, causing it to begin executing software at memory location **0xFFFFFFF0** The 80386 is reset to the real mode, and the leftmost 12 address connections remain logic Is (FFFH) until a far jump or far call is executed. This allows compatibility with earlier microprocessors.

Clock times 2(CLK2) is driven by a clock signal that is twice the operating frequency of the 80386. For example, to operate the 80386 at 16 MHz, apply a 32 MHz clock to this pin.

Ready controls (READY') the number of wait states inserted into the timing to lengthen memory accesses.

Lock (LOCK') becomes logic 0 whenever an instruction is prefixed with the LOCK: prefix. This is used most often during DMA accesses.

Data/control (D/C') indicates that the data bus contains data for or from memory or I/O when a logic I. If D/C is a logic 0, the microprocessor is halted or execute an interrupt acknowledge.

Bus size 16 (BS16') selects either a 32-bit data bus (BS16 = 1) or a 16-bit data bus (BS16 = 0). In most cases, if an 80386DX is operated on a 16-bit data bus, we use the 80386SX that has a 16-bit data bus. On the 80386EX, the BS8 pin selects an 8-bit data bus.

Next address (NA') causes the 80386 to output the address of the next instruction data in the current bus cycle. This pin is often used for pipelining the address.

Hold requests (HOLD) a DMA action.

Hold acknowledge (DLDA) indicates that the 80386 is currently in a hold condition.
Busy is an input used by the WAIT or FWAIT instruction that waits for the coprocessor to become available. This is also a direct connection to the 80387 from the 80386.
Error (ERROR') indicates to the microprocessor that an error is detected by the coprocessor.
An interrupt request (INTR) is used by external circuitry to request an interrupt.
Nun-maskable interrupt (NMI)A non-maskable interrupt requests a non-maskable interrupt as it did on the earlier versions of the microprocessor.

The Memory System

The memory is divided into four 8-bit-wide memory banks.
of memory. This 32-bit-wide memory organization allows bytes. or double words of memory data to be accessed directly. The 80386DX transfer up to a 32-bit-wide number in a single memory cycle. whereas the early 8088 requires four cycles to accomplish the same transfer. and the 80286 and 80386SX require two cycles. Today. the data is important. especially with single-precision floating-point number that are 32 bits wide. High-level software normally uses floating-point number for data storage, so 32-bit memory locations speed the execution of high-level software when it is written to take

advantage of this wider memory.

Each memory byte is numbered in hexadecimal as they were in prior versions of the family. The difference is that the 80386DX uses a 32-bit-wide memory address, with memory bytes numbered from location 00000000H to FFFFFFFFH

The two memory banks in the 8086, 80286. and 803S6SX system are accessed via BLE (on the 8086 and 80286) and BHE. In the 80386DX. the memory banks are accessed via four bank enable signals, BE3-BE0. It also allows a word to be addressed when two bank enable signals are activated. In most system. a word is addressed in banks 0 and 1, or in banks 2 and 3. Memory location 00000000H is in bank 0. location 00000001H is in bank I, location 00000002H is in bank 2, and location 00000003H is in bank 3. The 80386DX does not contain address connections A0 and A1 because these have been encoded as the bank enable signals. Likewise, the 80386SX does not contain the A0 address pin because it is encoded in the BLE and BHE signals. The 80386EX addresses data either in two banks for a 16-bit-wide memory system if BS8 = 1 or as an 8-bit system if BS8 = 0.

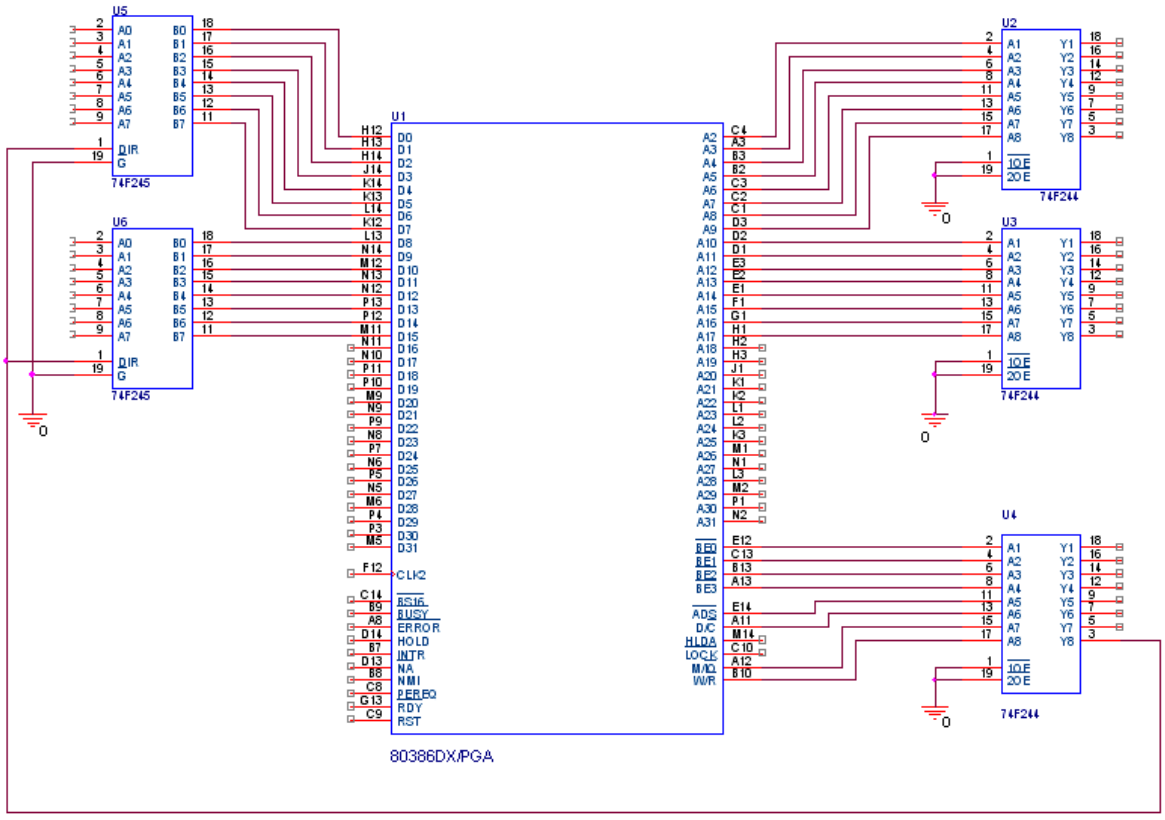
Table 5-6. Generating A0–A31 from BE0#–BE3# and A2–A31

Intel386™ DX Address Signals								
A31 ..... A2					BE3#	BE2#	BE1#	BE0#
A31	Physical Base Address	A2	A1	A0				
A31	.....	A2	0	0	X	X	X	Low
A31	.....	A2	0	1	X	X	Low	High
A31	.....	A2	1	0	X	Low	High	High
A31	.....	A2	1	1	Low	High	High	High

Buffering System.

80386DX connected to buffers that increase fan-out from its address, Data, and control connections. This microprocessor is operated at 12.5 MHz using a 25 MHz clock input signal that is generated by an integrated oscillator module.

We used 74f244 for buffering all output signals like Address bus, be0-be3, ads, d/c', m/io', and w/r'And by-directional try-state buffers 74f245 for buffering data bus. The (W/R') is used to control direction of data on Data bus.



The Input/output System

The 80386 input/output system is the same as that found in any Intel 8086 family microprocessor-based system. There are 64K different bytes of I/O space available if isolated I/O is implemented. With isolated I/O, the IN and OUT instructions are used to transfer I/O data between the microprocessor and I/O devices. The I/O port address appears on address bus connections AI5-A2, with BE3-BEO used to select a byte, word, or double word of I/O data. If memory-mapped I/O is implemented, then the number of I/O locations can be any amount up to 4G bytes. With memory-mapped I/O, any instruction that transfers data between the microprocessor and memory system can be used for I/O transfers because the I/O device is treated as a memory device. Almost all 80386 systems use isolated I/O because of the I/O protection scheme provided by the 80386 in protected mode operation.

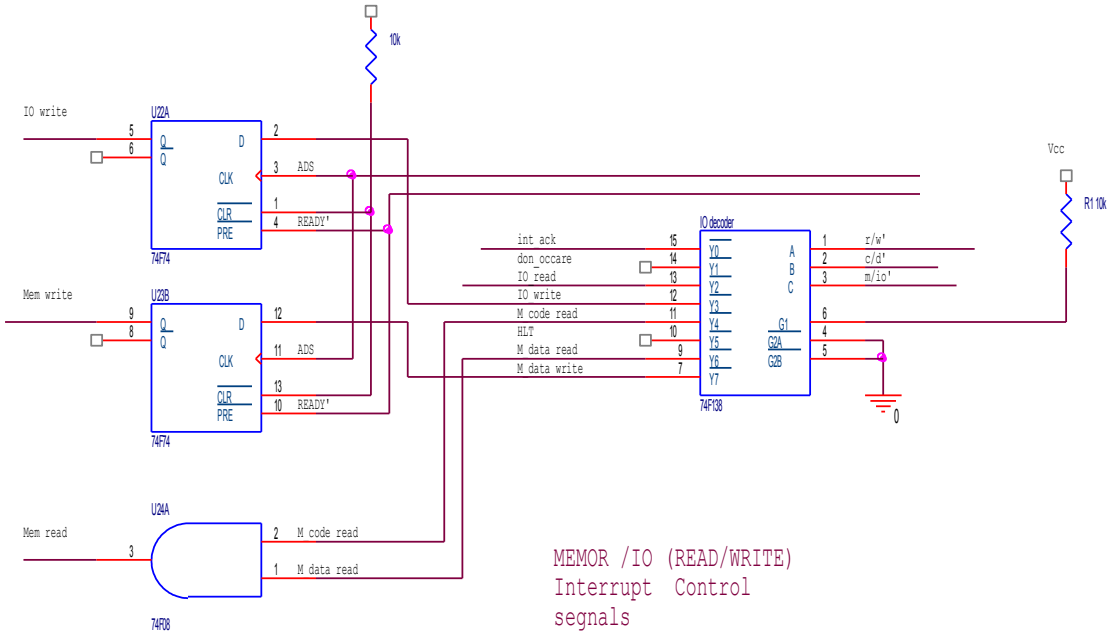
Unlike the I/O map of earlier Intel microprocessors, which were 16 bits wide. the 80386 uses a full 32-bit-wide I/O system divided into four banks. This is identical to the memory system, which is also divided into four banks. Most I/O transfers are 8 bits wide because we often use ASCII code (a seven-bit code) for transferring alphanumeric data between the microprocessor and printers and keyboards. This may change if Unicode, a 16-bit alphanumeric code, becomes

common and replaces ASCII code. Recently, I/O devices that are 16 and even 32 bits wide have appeared for systems such as disk

Memory and I/O Control Signals

The memory and I/O are controlled with separate signals. The M/IO' signal indicates whether the data transfer is between the microprocessor and the memory (M/IO' = I) or I/O (M/IO' = 0). In addition to M/IO', the memory and I/O systems must read or write data. The W/R signal is logic 0 for a read operation and logic 1 for a write operation. The ADS' signal is used to qualify the M/IO' and W/R' control signals.

This is a slight deviation from earlier Intel microprocessors, which didn't use ADS' for qualification. Notice that two control signals are developed for memory control (MRDC' and MWTC') and two (or I/0 controls (IORC' and IOWE'). These signals are consistent with the memory and I/O control signals generated for use in earlier versions of the Intel microprocessor.



Timing

Tuning is important for understanding how to interface memory and I/O to the 80386 microprocessor. Note that the timing is referenced to the CLK2 input signal and that a bus cycle consists of four clocking periods.

Each bus cycle contains two clocking states with each state (T1 and T2) containing two clocking periods time for the two states equal 4/CLK2. The 12.5 MHz version allows memory access time of time(T0,T1)-47ns which is equal 160ns-47ns=113ns before wait states are inserted

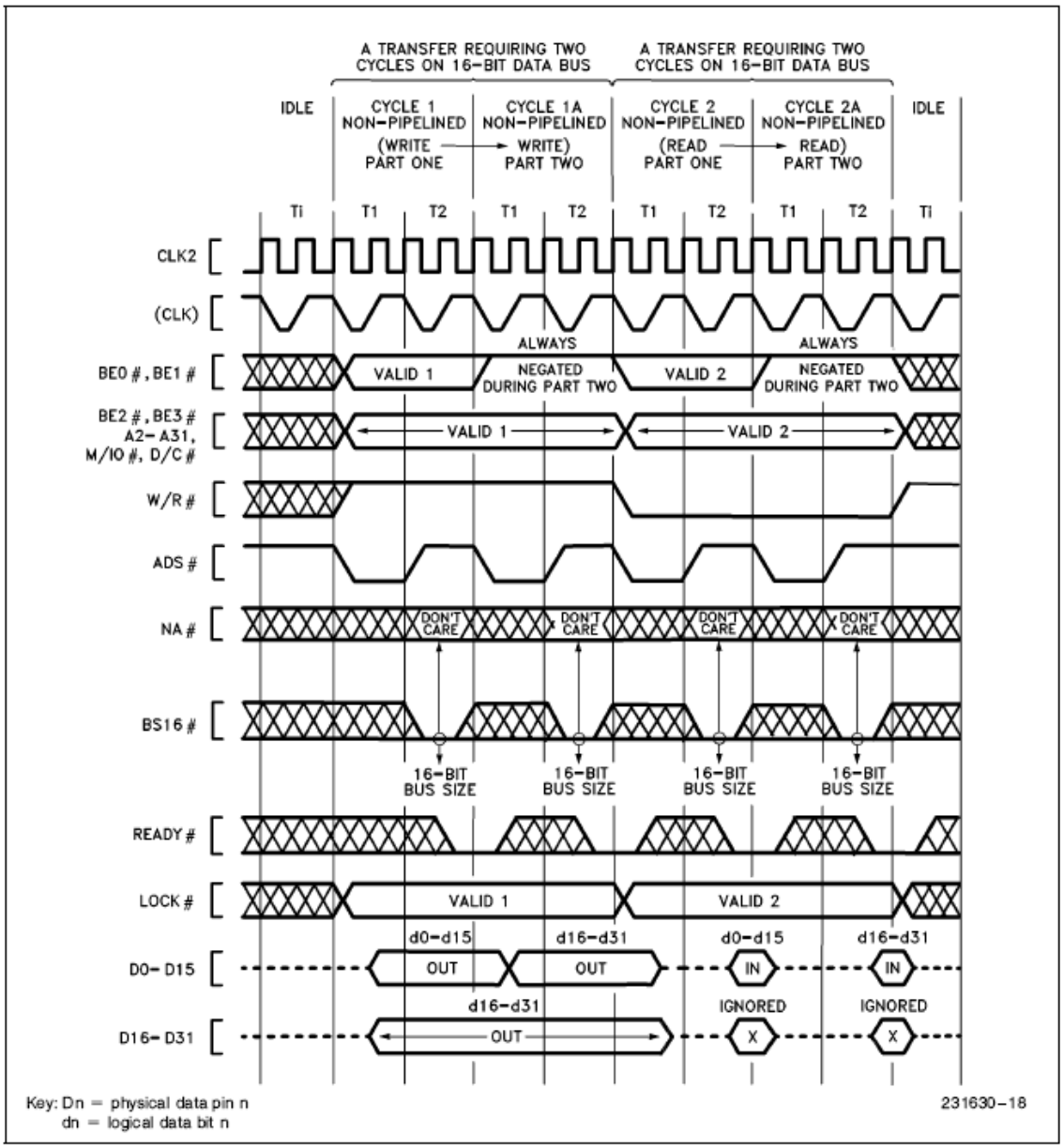


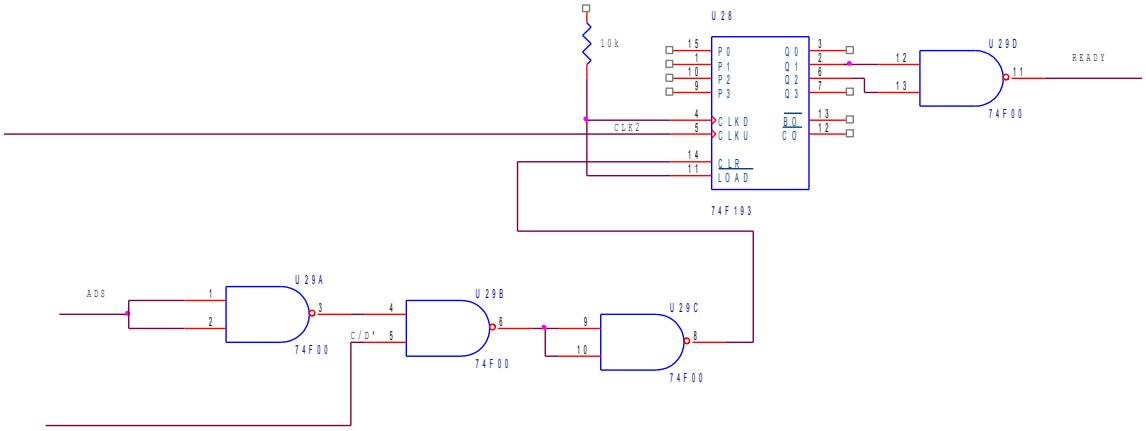
Figure 5-14. Asserting BS16# (zero wait states, non-pipelined address)

Wait States

Wait states are needed if memory access times are long compared with the time allow 80386 for memory access. In a no pipelined 12.5 MHz system, only a few DRAM memories exist that have an access time of 113 ns. This mean, often wait states must be introduced to

access the DRAM (one wait for 120 ns DRAM) ,EPROM that has an access time of 150 ns (one waits).
Each wait state added increase access time with 80ns,to ensure compatibility with IO devices we added 3 hardwired wait states for each read or writ access, whether it's an IO access or memory access.

The READY input controls whether or not wait states are inserted into the timing READY input on the 80386 is a dynamic input that must be activated during each bus.to generate three wait states we used the following circuit:-



CLK2 input increase the counter value by one, if the counter value reached 0110(count to 6) the ready output is asserted (which cause the microprocessor to end the current read or write cycle) when a new read or write cycle begins (ADS=0, C/D'=1) the counter CLR' input is

asserted to clear the counter.

Timing with Wait states

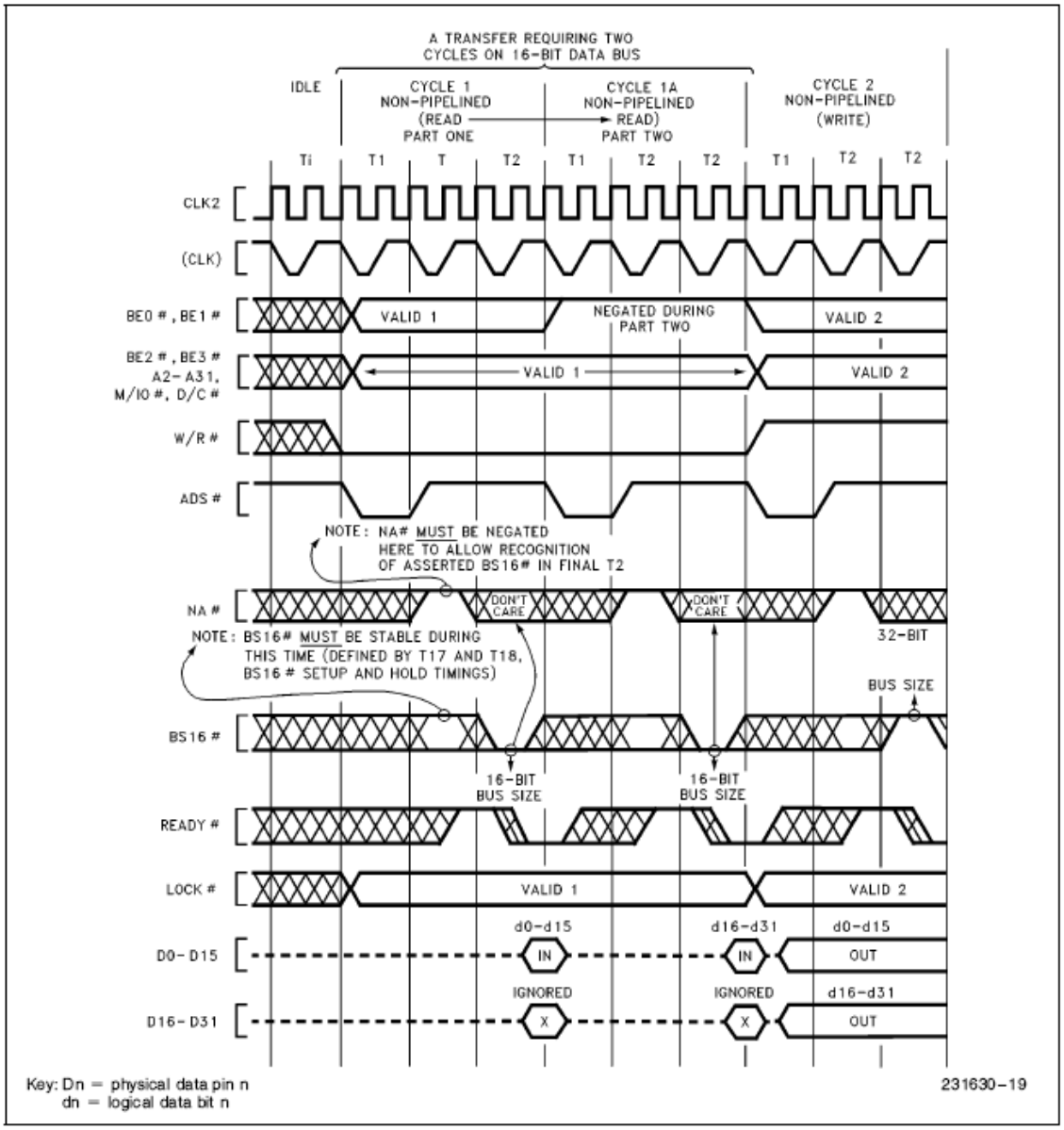


Figure 5-15. Asserting BS16 # (one wait state, non-pipelined address)

The physical data bus width for any non-pipelined bus cycle can be either 32-bits or 16-bits. At the beginning of the bus cycle, the processor behaves as if

the data bus is 32-bits wide. When the bus cycle is acknowledged, by asserting READY' at the end of a T2 state, the most recent sampling of BS16' determines the data bus size for the cycle being acknowledged. If BS16' was most recently negated, the physical data bus size is defined as 32 bits. If BS16Ý was most recently asserted, the size is defined as 16 bits.

When BS16' is asserted and two 16-bit bus cycles are required to complete the transfer, BS16' must be asserted during the second cycle; 16-bit bus size is not assumed. Like any bus cycle, the second 16-bit cycle must be acknowledged by asserting READY'.

When a second 16-bit bus cycle is required to complete the transfer over a 16-bit bus, the addresses generated for the two 16-bit bus cycles are closely related to each other. The addresses are the same except BE0' and BE1' are always negated for the second cycle. This is because data on D0-D15 was already transferred during the first 16-bit cycle.

A0, A1, BLE, and BHE generating

In 32-bit-wide physical memories each physical Dword begins at a byte address that is a multiple of 4. A2-A31 are directly used as a Dword select and

BE0'-BE3' as byte selects. BS16' is negated for all bus cycles involving the 32-bit array.

When 16-bit-wide physical arrays are included in the system, each 16-bit physical word begins at an address that is a multiple of 2.

Note the address is decoded, to assert BS16' only during bus cycles involving the 16-bit array.

IO Peripherals

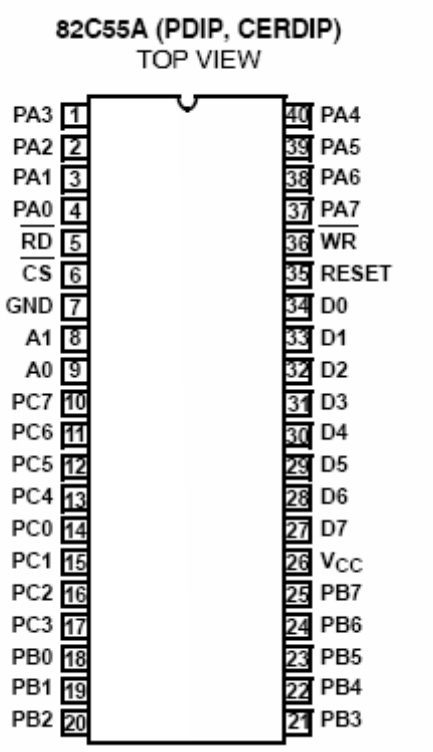
-Parallel Peripheral interface8255

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B One 8-bit data input/output latch/buffer and one 8-bit



data input buffer. **Port C** One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into

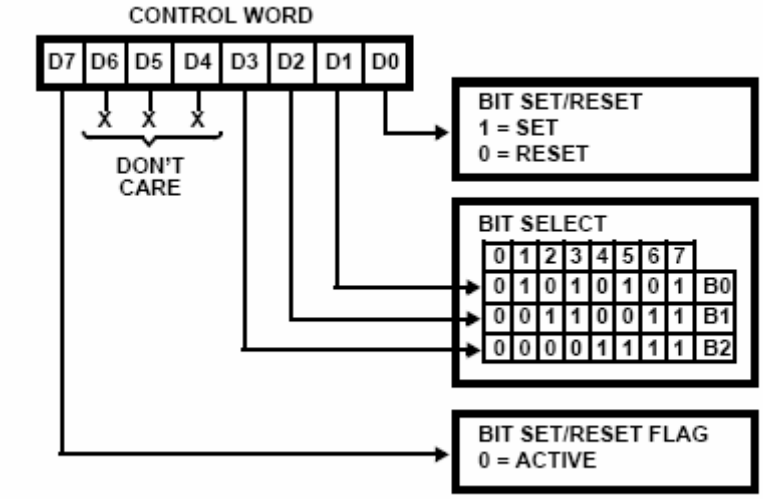


FIGURE 5. BIT SET/RESET FORMAT

MODE 0 PORT DEFINITION

A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (Upper)	#	PORT B	PORT C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Interrupt Controller 8259

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus, limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

Programming the 82C59A

The 82C59A accepts two types of command words generated by the CPU:

1. **Initialization Command Words (ICWs):** Before normal operation can begin, each 82C59A in the system must be brought to a starting point - by a sequence of 2 to 4 bytes timed by WR pulses.

2. **Operation Command Words (OCWs):** These are the command words which command the 82C59A to operate in various interrupt modes. Among these modes are:

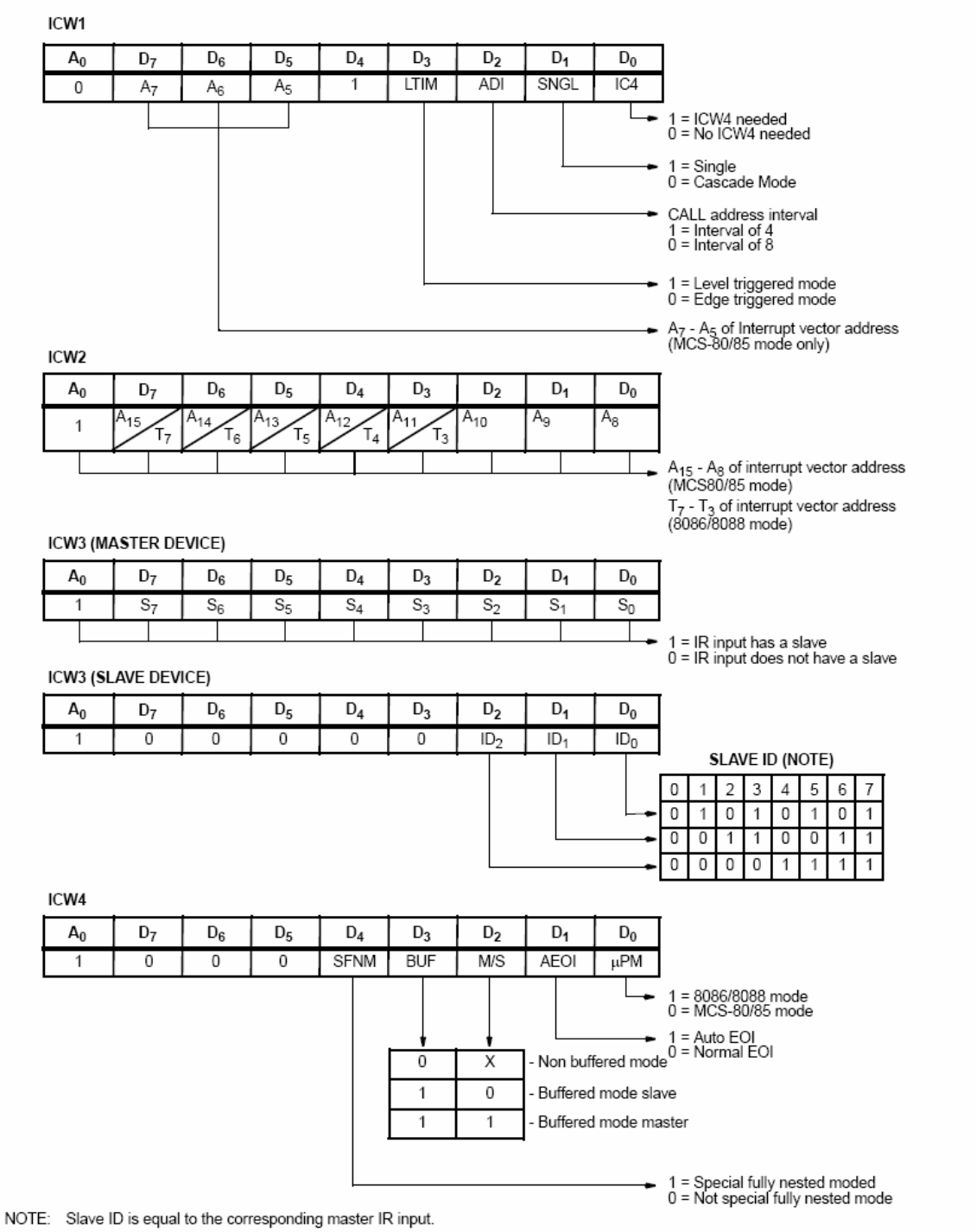
a. Fully nested mode.

b. Rotating priority mode.

c. Special mask mode.

d. Polled mode.

The OCWs can be written into the 82C59A anytime after initialization.

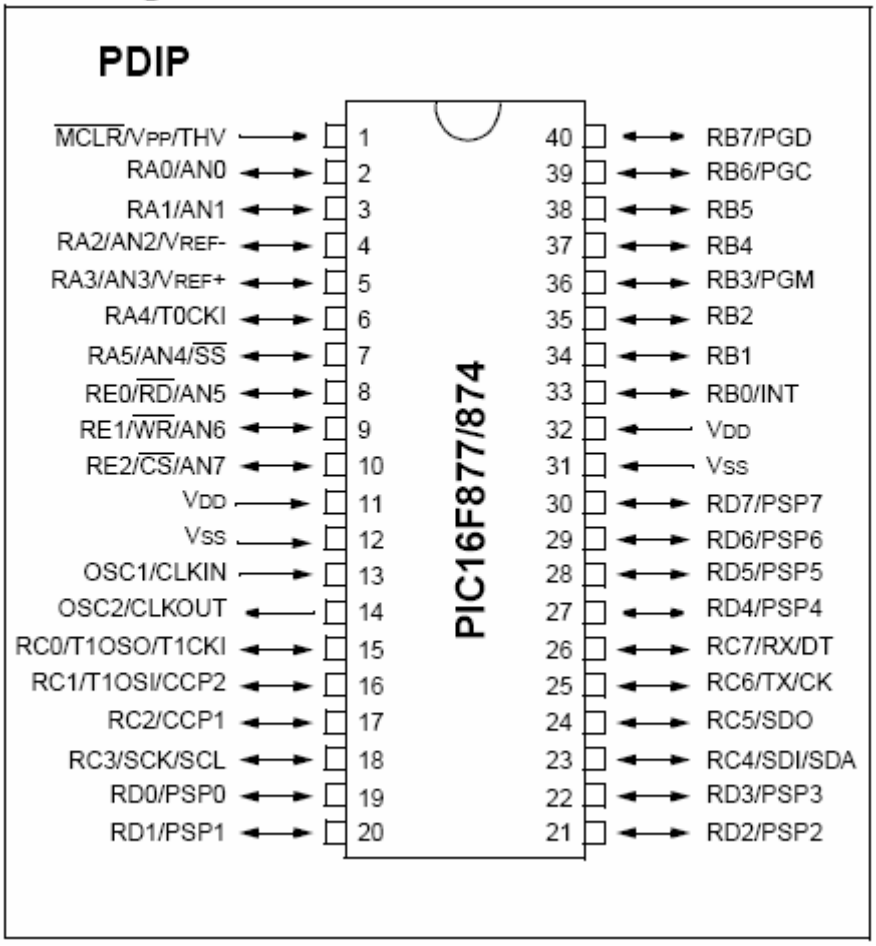


NOTE: Slave ID is equal to the corresponding master IR input.

FIGURE 7. 82C59A INITIALIZATION COMMAND WORD FORMAT

-PIC 16F877 Microcontroller

Pin Diagram



Used to interface microprocessor with PS-2 keyboard, Graphical LCD, and Serial Communication with PC.

Using PSP we achieved handshaking between micro processor and PIC, the microprocessor commands the PIC to execute one of the following commands:-

1. Write data to GLCD and increment writing pointer(ASCII).
2. Write data to GLCD specific Address.
3. Write command to GLCD.

4	Clear the GLCD and initialize writing Pointer
5	Display Main menu.
6	Write command to PS-2 keyboard
7	Read character (ASCII) from keyboard.
8	Send data Serially to other devices
9	Resave data from other serial devices.

Each command word (8 bit) is divided into to parts
*Command type (most significant 4 bits).
*Data count (number of data bytes following the command used to complete execution of the command).

Timing of Parallel Slave Port (PSP):-

PIC in the default Case (no commands to execute) is idle waiting for PSP interrupt .

When processor sends command to PIC (write Operation relative to PIC), PSP interrupt is occur and PIC execute that Command putting the result value on PSP register, data now is available to Processor to read.

During execution of command the PIC_ready output become Logic 0 to tell Processor that the PIC is not ready to receive other commands. After execution complication PIC_ready output become Logic 1(PIC is ready now).

FIGURE 3-10: PARALLEL SLAVE PORT WRITE WAVEFORMS

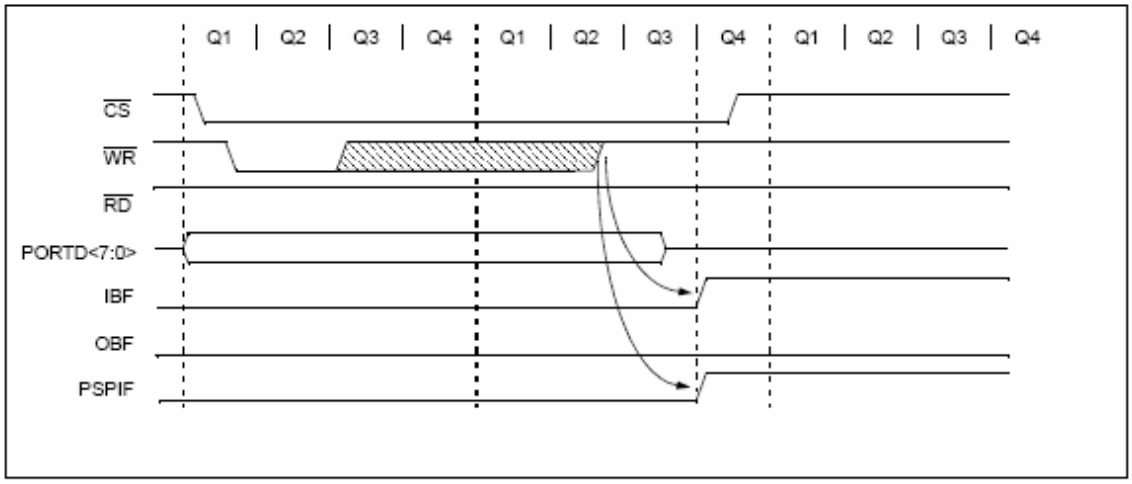
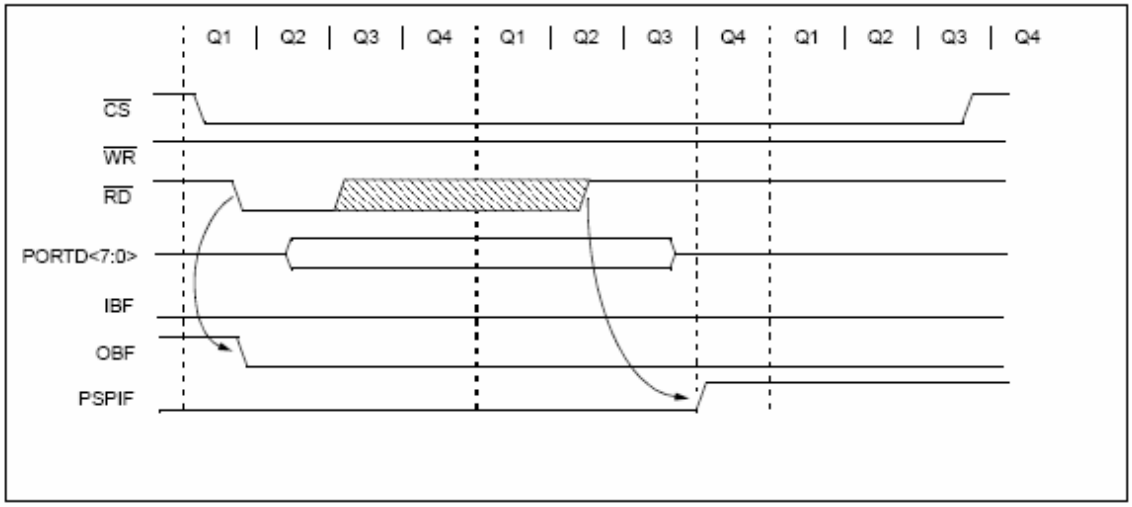


FIGURE 3-11: PARALLEL SLAVE PORT READ WAVEFORMS



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80386-DX Computer (KIT)

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