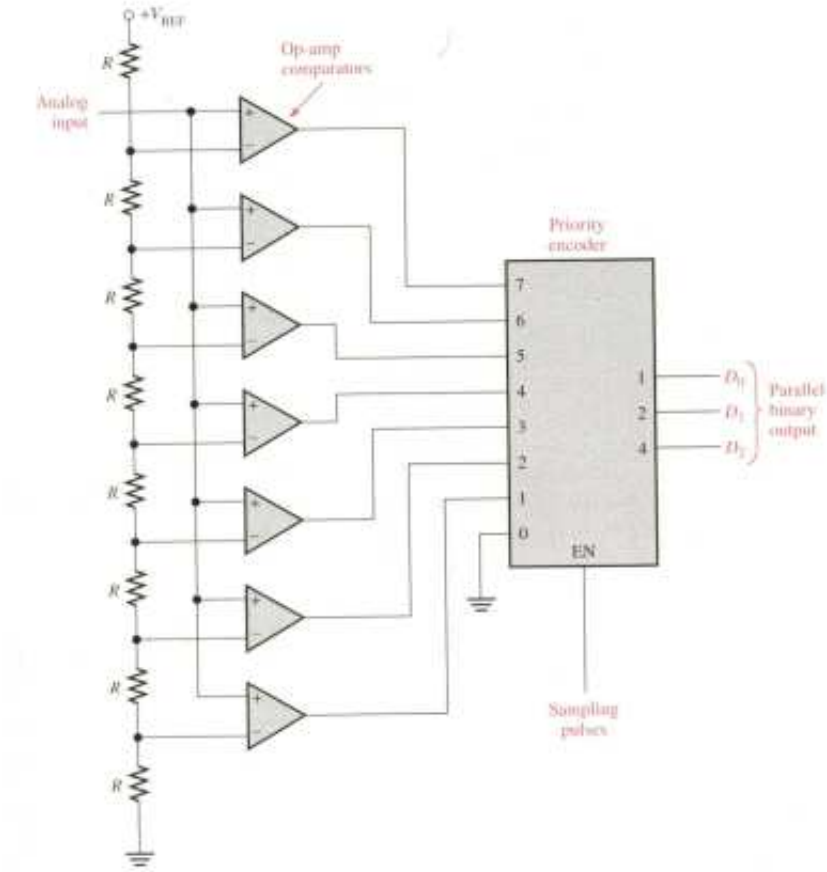
Analogue to Digital Converters (ADC)

Flash (Simultaneous) ADC

The flash ADC uses comparators that compare reference voltages with the analogue input voltage. When the analogue voltage exceeds the reference voltage for a given comparator, a High is generated. In general (2^n -1) comparators are required. So for an 8-bit conversion 255 comparators are required. However the flash ADC provides a fast conversion time because of the parallel process.



3-Bit Flash Analogue to Digital Converter (ADC)

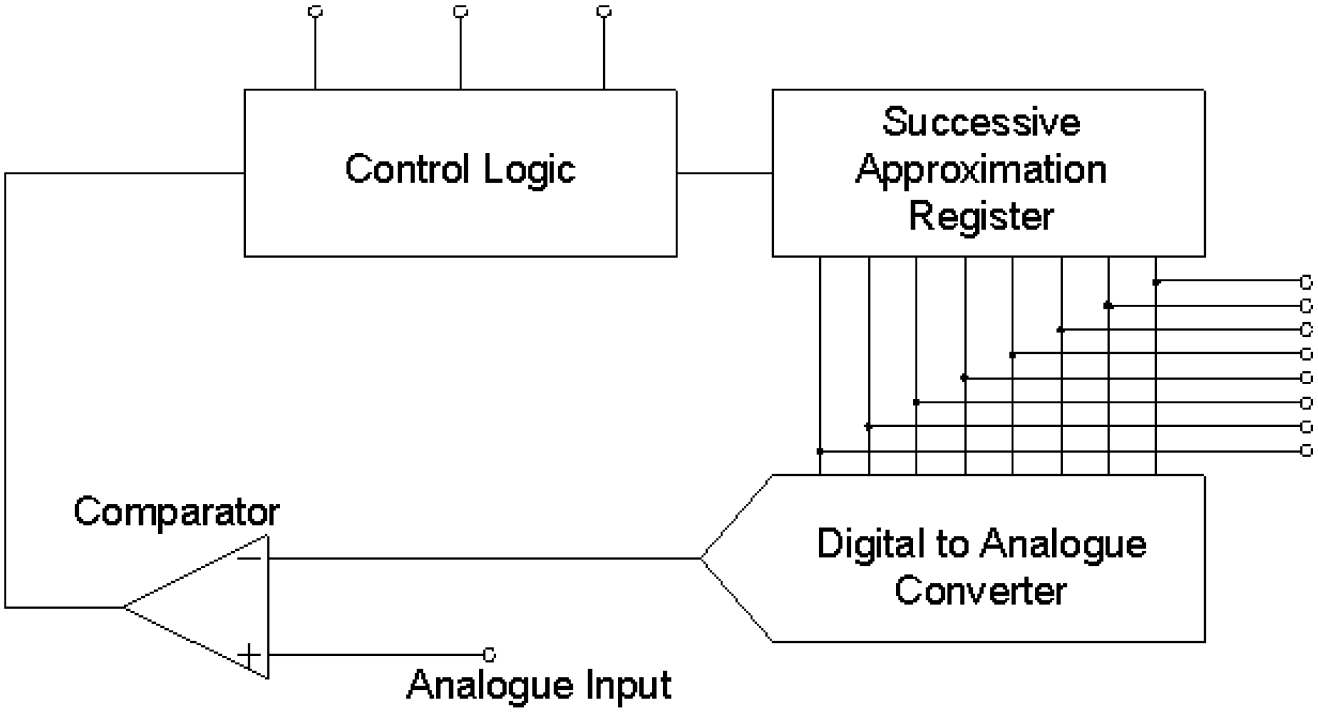
The reference voltage for each comparator is set by the resistive voltage divider network. The output of each comparator is connected to an input of the priority encoder. The encoder is sampled by a pulse on the Enable input and a 3-bit binary code representing the analogue input appears on the encoder output. The binary code is determined by the highest order input having a High level.

Principle of Operation:

- The flash ADC comprises an array of comparators.
- Each comparator is connected to a resistive voltage divider and to the analogue input voltage.
- The resistive voltage divider consists of equal valued resistors connected in series with the reference voltage V_{REF}.
- Thus each comparator compares the analogue input voltage with a slightly different voltage from the divider.
- Those comparators which are connected to divider resistors where the divider voltage

is lower than the analogue input voltage will give a high output
- The other comparators will produce a low output.
- Larger analogue input voltages will result in more comparator high outputs.
- The pattern of comparator high/low outputs is applied to encoder circuits which convert the data into a binary output number which is proportional to the ratio of the analogue input voltage to the reference voltage.

Successive Approximation ADC



- The ADC is interfaced to a controller - usually a microprocessor.
- The controller decides when a conversion is to be performed and initiates the conversion by asserting the **Start Convert** signal line into the control logic.
- The Control Logic monitors the input to determine whether the present contents of the register represent a value which is below or above the analogue input voltage.
- Each bit is set in turn starting with the MSB and working down to the LSB.
- The effect of setting each bit is noted by the control logic and
  - if setting a particular bit results in a DAC output in excess of the analogue input voltage, the bit is cleared before moving on to the next bit
  - otherwise the bit is left set.

- At the end of the process, the LSB is adjusted and the conversion is complete.
- The control logic signals this to the controller/microprocessor by asserting the End of Conversion line and the digital output is taken from the register output.

The main advantages of the flash type of ADC over the successive approximation ADC:

- The successive approximation type of ADC includes in its circuits a binary counter that is clocked by a gated clock oscillator.
- The clock is gated on so long as the counter output is lower than the binary equivalent of the analogue input voltage.
- Once the counter output exceeds the analogue output binary equivalent the oscillator is gated off and the counter output is taken to be the binary equivalent of the analogue input.
- On average, the ramp conversion of ADC requires of the order of $(2^n - 1)$ clock cycles for each conversion where n is the bit length of the ADC output. Thus, a 16-bit converter will need 65535 clock pulses for each conversion.
- This limits the maximum frequency that can be handled by such ADCs to perhaps 100 kHz maximum.
- The flash converter is capable of performing conversions in a time interval related to the slew rate of the comparators and the propagation delay of the encoder circuits.
- Thus typical flash ADCs can perform conversions fast enough to work on real time video data - i.e. data conversion at frequencies of tens of MHz.